

# HDL Coder™

## User's Guide

**R2012b**

**MATLAB®**

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*HDL Coder™ User's Guide*

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# HDL Code Generation from MATLAB

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- Chapter 2, “Code Generation”
- Chapter 3, “Code Generation”
- Chapter 4, “Optimization”
- Chapter 5, “Speed and Area Optimization”
- Chapter 6, “HDL Workflow Advisor Reference”



# MATLAB Algorithm Design

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- “MATLAB Test Bench Requirements and Best Practices” on page 1-62

# Operators

## Arithmetic Operators

HDL Coder™ supports the arithmetic operators (and equivalent MATLAB® functions) listed in the following table.

Operation	Operator Syntax	Equivalent Function	Restrictions
Binary addition	A+B	plus(A,B)	Neither A nor B can be data type logical.
Matrix multiplication	A*B	mtimes(A,B)	
Arraywise multiplication	A.*B	times(A,B)	Neither A nor B can be data type logical.
Matrix power	A^B	mpower(A,B)	A and B must be scalar, and B must be an integer.
Arraywise power	A.^B	power(A,B)	A and B must be scalar, and B must be an integer.
Complex transpose	A'	ctranspose(A)	
Matrix transpose	A.'	transpose(A)	
Matrix concat	[A B]	None	
Matrix index	A(r c)	None	Before you use a variable, you must fully define it.

## Relational Operators

HDL Coder supports the relational operators (and equivalent MATLAB functions) listed in the following table.

Relation	Operator Syntax	Equivalent Function
Less than	$A < B$	<code>lt(A,B)</code>
Less than or equal to	$A \leq B$	<code>le(A,B)</code>
Greater than or equal to	$A \geq B$	<code>ge(A,B)</code>
Greater than	$A > B$	<code>gt(A,B)</code>
Equal	$A == B$	<code>eq(A,B)</code>
Not equal	$A \neq B$	<code>ne(A,B)</code>

## Logical Operators

HDL Coder supports the logical operators (and equivalent MATLAB functions) listed in the following table.

Relation	Operator Syntax	M Function Equivalent	Notes
Logical And	$A \& B$	<code>and(A,B)</code>	
Logical Or	$A   B$	<code>or(A,B)</code>	
Logical Xor	$A \text{ xor } B$	<code>xor(A,B)</code>	
Logical And (short circuiting)	$A \&\& B$	N/A	Use short circuiting logical operators within conditionals. See also “Control Flow Statements” on page 17-62.

<b>Relation</b>	<b>Operator Syntax</b>	<b>M Function Equivalent</b>	<b>Notes</b>
Logical Or (short circuiting)	A   B	N/A	Use short circuiting logical operators within conditionals. See also “Control Flow Statements” on page 17-62.
Element complement	~A	not(A)	



## Control Flow Statements

HDL Coder supports the following control flow statements and constructs with restrictions.

Control Flow Statement	Restrictions
for	<p>Do not use for loops without static bounds.</p> <p>Do not use the &amp; and   operators within conditions of a for statement. Instead, use the &amp;&amp; and    operators.</p> <p>HDL Coder does not support nonscalar expressions in the conditions of for statements. Instead, use the all or any functions to collapse logical vectors into scalars.</p>
if	<p>Do not use the &amp; and   operators within conditions of an if statement. Instead, use the &amp;&amp; and    operators.</p> <p>HDL Coder does not support nonscalar expressions in the conditions of if statements. Instead, use the all or any functions to collapse logical vectors into scalars.</p>
switch	<p>The conditional expression in a switch or case statement must use only:</p> <ul style="list-style-type: none"> <li>• uint8, uint16, uint32, int8, int16, or int32 data types</li> <li>• Scalar data</li> </ul> <p>If multiple case statements make assignments to the same variable, the numeric type and fimath specification for that variable must be the same in every case statement.</p>

The following control flow statements are not supported:

- while
- break
- continue

- return

## **Vector Function Limitations Related to Control Statements**

Avoid using the following vector functions, as they may generate loops containing break statements:

- isequal
- bitrevorder

## Persistent Variables

Persistent variables enable you to model registers. If you need to preserve state between invocations of your MATLAB algorithm, use persistent variables.

Before you use a persistent variable, you must initialize it with a statement specifying its size and type. You can initialize a persistent variable with either a constant value or a variable, as in the following examples:

```
% Initialize with a constant
persistent p;
if isempty(p)
    p = fi(0,0,8,0);
end
```

```
% Initialize with a variable
initval = fi(0,0,8,0);
```

```
persistent p;
if isempty(p)
    p = initval;
end
```

Use a logical expression that evaluates to a constant to test whether a persistent variable has been initialized, as in the preceding examples. Using a logical expression that evaluates to a constant ensures that the generated HDL code for the test is executed only once, as part of the reset process.

You can initialize multiple variables within a single logical expression, as in the following example:

```
% Initialize with variables
initval1 = fi(0,0,8,0);
initval2 = fi(0,0,7,0);
```

```
persistent p;
if isempty(p)
    x = initval1;
    y = initval2;
```

end

---

**Note** If persistent variables are not initialized as described above, extra sentinel variables can appear in the generated code. These sentinel variables can translate to inefficient hardware.

---

## Persistent Array Variables

Persistent array variables enable you to model RAM.

By default, the coder optimizes the area of your design by mapping persistent array variables to RAM. If persistent array variables are not mapped to RAM, they map to registers. RAM mapping can therefore reduce the area of your design in the target hardware.

To learn how persistent array variables map to RAM, see “Map Persistent Arrays and `dsp.Delay` to RAM” on page 4-3.

## Data Types for Variables and Constants

### Supported Data Types

HDL Coder supports the following subset of MATLAB data types.

Types	Supported Data Types	Restrictions
Integer	<ul style="list-style-type: none"> <li>uint8, uint16, uint32,</li> <li>int8, int16, int32</li> </ul>	
Real	<ul style="list-style-type: none"> <li>double</li> <li>single</li> </ul>	HDL code generated with double or single data types can be used for simulation, but is not synthesizable.
Character	char	
Logical	logical	
Fixed point	<ul style="list-style-type: none"> <li>Scaled (binary point only) fixed-point numbers</li> <li>Custom integers (zero binary point)</li> </ul>	<p>Fixed-point numbers with slope (not equal to 1.0) and bias (not equal to 0.0) are not supported.</p> <p>Maximum word size for fixed-point numbers is 128 bits.</p>
Vectors	<ul style="list-style-type: none"> <li>unordered {N}</li> <li>row {1, N}</li> <li>column {N, 1}</li> </ul>	<p>The maximum number of vector elements allowed is <math>2^{32}</math>.</p> <p>Before a variable is subscripted, it must be fully defined.</p>

<b>Types</b>	<b>Supported Data Types</b>	<b>Restrictions</b>
Matrices	{N, M}	Matrices are supported in the body of the design algorithm, but are not supported as inputs to the top-level design function.  Do not use matrices in the testbench.
Structures	struct	Structures are supported in the body of the design algorithm, but are not supported as inputs to the top-level design function.  Do not use structures in the testbench.

## Unsupported Data Types

In the current release, the following data types are not supported:

- Cell array
- Enumeration

## System Objects

In this section...
“Why Use System Objects?” on page 1-12
“System Objects Supported for HDL Code Generation from MATLAB” on page 1-12
“Limitations of HDL Code Generation from System Objects” on page 1-13

### Why Use System Objects?

System objects provide a design advantage because:

- You can save time during design and testing by using existing System object™ components.
- HDL code that you generate from System object is modular and therefore more readable.

### System Objects Supported for HDL Code Generation from MATLAB

The coder supports the following Fixed-Point Toolbox™ System object for HDL code generation:

- `hdlram`

The coder supports the following Communications System Toolbox™ System objects for HDL code generation:

- `comm.BPSKModulator`, `comm.BPSKDemodulator`
- `comm.PSKModulator`, `comm.PSKDemodulator`
- `comm.QPSKModulator`, `comm.QPSKDemodulator`
- `comm.RectangularQAMModulator`, `comm.RectangularQAMDemodulator`
- `comm.ConvolutionalInterleaver`, `comm.ConvolutionalDeinterleaver`
- `comm.ViterbiDecoder`



The coder supports the following DSP System Toolbox™ System objects for HDL code generation:

- `dsp.Delay`
- `dsp.Maximum`
- `dsp.Minimum`
- `dsp.BiquadFilter`

## **Limitations of HDL Code Generation from System Objects**

The following limitations apply to HDL code generation from System objects:

- `step` is the only method supported for HDL code generation.
- Your design can call the `step` method only once per System object.
- `step` must not be inside a loop or a conditional statement.
- System objects must be declared persistent.
- You can use the `dsp.Delay` System object only in feed-forward delay modeling.

## Model and Generate RAM with hdlram

You can model RAM behavior and generate RAM from your MATLAB code using the `hdlram` System object.

To learn how RAM generated from `hdlram` differs from other MATLAB code that can map to RAM, see “RAM Mapping Comparison for MATLAB Code” on page 4-7.

### hdlram Restrictions for Code Generation

Code generation from `hdlram` has the same restrictions as code generation from other System objects. For details, see “Limitations of HDL Code Generation from System Objects” on page 1-13.

### Ring Buffer Implementation using hdlram

This example shows how to implement a ring buffer using `hdlram`. In the RAM, data is written in one position and read from another position. The write data is read back after a specific number of cycles.

A counter generates the RAM write address, and the read address is generated by adding a constant  $K$  to the write address. If the memory size is  $M$ , the input is read  $M-K$  clock cycles after it is written to the memory. This implements  $M-K$  word shift behavior.

```
##codegen
function data_out = mlhdlc_line_delay(data_in)

persistent hRam;
if isempty(hRam)
    hRam = hdlram('RAMType', 'Dual Port');
end

% RAM size 512
ram_addr_type = numerictype(0,9,0);
fm = hdlfimath;

% read address counter
persistent rdAddrCtr;
```

```
if isempty(rdAddrCtr)
    rdAddrCtr = fi(0, ram_addr_type, hdlfimath);
end

% ring counter length
ringCtrLength = 10;
ramWriteAddr = fi(rdAddrCtr + ringCtrLength, ram_addr_type, fm);

ramWriteData = data_in;
ramWriteEnable = true;

ramReadAddr = rdAddrCtr;

% execute single step of RAM
[~, ramRdDout] = step(hRam, ramWriteData, ramWriteAddr,
                    ramWriteEnable, ramReadAddr);

rdAddrCtr(:) = rdAddrCtr + 1;

data_out = ramRdDout;
```

To see an example of a MATLAB design and test bench that use hdlram, enter the following at the command line:

```
edit mlhdlc_hdlram.m; edit mlhdlc_hdlram_tb.m
```

## HDL Code Generation from Viterbi Decoder System object

This example shows how to check, generate and verify HDL code from MATLAB code that instantiates a Viterbi Decoder System object.

### MATLAB Design

The MATLAB code used in this example is a Viterbi Decoder used in hard decision convolutional decoding, implemented as a System object. This example also shows a MATLAB test bench that exercises the filter.

```
design_name = 'mlhdlc_sysobj_viterbi.m';
testbench_name = 'mlhdlc_sysobj_viterbi_tb.m';
```

Let us take a look at the MATLAB design.

```
type(design_name);
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% MATLAB design: FIR Filter
%
% Key Design pattern covered in this example:
% (1) Using comm system toolbox ViterbiDecoder function
% (2) The 'step' method can be called only per system object in a design it
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

function decodedBits = mlhdlc_sysobj_viterbi(inputSymbol)

persistent hVitDec;

if isempty(hVitDec)
    hVitDec = comm.ViterbiDecoder('InputFormat','Hard', 'OutputDataType', 'int8');
end

decodedBits = step(hVitDec, inputSymbol);

type(testbench_name);
```

```

% Viterbi_tb - testbench for Viterbi_dut

numErrors = 0;
% rand stream
original_rs = RandStream.getGlobalStream;
rs = RandStream.create('mrg32k3a', 'seed', 25);
%RandStream.getGlobalStream(rs);
rs.reset;
% convolutional encoder
hConvEnc = comm.ConvolutionalEncoder;
% BER
hBER = comm.ErrorRate;
hBER.ReceiveDelay = 34;
reset(hBER);

% clear persistent variables in the design between runs of the testbench
clear mlhdlc_msysobj_viterbi;

for numSymbols = 1:10000
    % generate a random bit
    inputBit = logical(randi([0 1], 1, 1));

    % encode it with the Convolutional Encoder - rate 1/2
    encodedSymbol = step(hConvEnc, inputBit);

    % optional - add noise

    %%%%%%%%%%%
    % call Viterbi Decoder DUT to decode the symbol
    %%%%%%%%%%%
    vitdecOut = mlhdlc_msysobj_viterbi(encodedSymbol);

    ber = step(hBER, inputBit, vitdecOut);
end

fprintf('%s\n', repmat('%', 1, 38));
fprintf('%%%%%%%%%% %s %%%%%%%%%%%\n', 'Viterbi Decoder Output');
fprintf('%s\n', repmat('%', 1, 38));
fprintf('Number of bits %d, BER %g\n', numSymbols, ber(1));

```

```
fprintf('%s\n', repmat('%', 1, 38));

% EOF
```

### Create a New Folder and Copy Relevant Files

Execute the following lines of code to copy the necessary example files into a temporary folder.

```
mlhdlc_demo_dir = fullfile(matlabroot, 'toolbox', 'hdlcoder', 'hdlcoderdemo');
mlhdlc_temp_dir = [tempdir 'mlhdlc_so_viterbi'];

% Create a temporary folder and copy the MATLAB files.
cd(tempdir);
[~, ~, ~] = rmdir(mlhdlc_temp_dir, 's');
mkdir(mlhdlc_temp_dir);
cd(mlhdlc_temp_dir);

copyfile(fullfile(mlhdlc_demo_dir, design_name), mlhdlc_temp_dir);
copyfile(fullfile(mlhdlc_demo_dir, testbench_name), mlhdlc_temp_dir);
```

### Simulate the Design

Simulate the design with the testbench prior to code generation to make sure there are no runtime errors.

```
mlhdlc_sysobj_viterbi_tb

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%% Viterbi Decoder Output %%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Number of bits 10000, BER 0
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

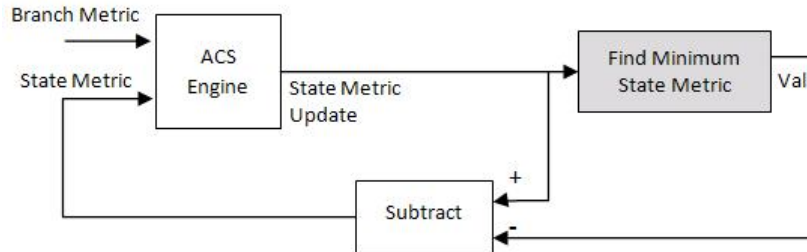
### Hardware Implementation of Viterbi Decoding Algorithm

There are three main components in the Viterbi decoding algorithm. They are the branch metric computation (BMC), add-compare-select (ACS), and traceback decoding. The following diagram illustrates the three units in the Viterbi decoding algorithm.



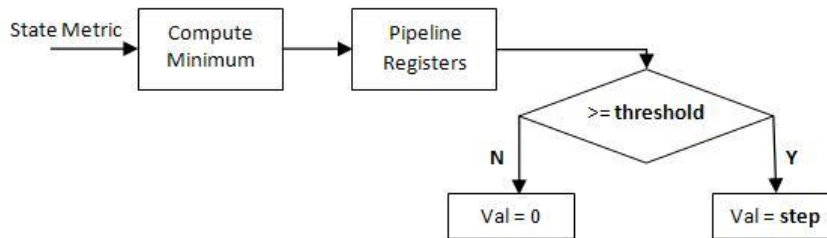
### The Renormalization Method

The Viterbi decoder prevents the overflow of the state metrics in the ACS component by subtracting the minimum value of the state metrics at each time step, as shown in the following figure.



Obtaining the minimum value of all the state metric elements in one clock cycle results in a poor clock frequency for the circuit. The performance of the circuit may be improved by adding pipeline registers. However, simply subtracting the minimum value delayed by pipeline registers from the state metrics may still lead to overflow.

The hardware architecture modifies the renormalization method and avoids the state metric overflow in three steps. First, the architecture calculates values for the threshold and step parameters, based on the trellis structure and the number of soft decision bits. Second, the delayed minimum value is compared to the threshold. Last, if the minimum value is greater than or equal to the threshold value, the implementation subtracts the step value from the state metric; otherwise no adjustment is performed. The following figure illustrates the modified renormalization method.



### Create a New HDL Coder Project

To create a new project, enter the following command:

```
coder -hdlcoder -new mlhdlc_viterbi
```

Next, add the file 'mlhdlc\_sysobj\_viterbi.m' to the project as the MATLAB function and 'mlhdlc\_sysobj\_viterbi\_tb.m' as the MATLAB test bench.

You can refer to the Getting Started with MATLAB to HDL Workflow tutorial for a more complete tutorial on creating and populating MATLAB HDL Coder projects.

### Run Fixed-Point Conversion and HDL Code Generation

Launch the Workflow Advisor. In the Workflow Advisor, right-click the 'Code Generation' step and choose the option 'Run to selected task' to run all the steps from the beginning through HDL code generation.

Examine the generated HDL code by clicking the links in the log window.

### Supported System objects

Refer to the documentation for a list of System objects supported for HDL code generation.

### Clean up the Generated Files

Run the following commands to clean up the temporary project folder.

```
mlhdlc_demo_dir = fullfile(matlabroot, 'toolbox', 'hdlcoder', 'hdlcoderdem
```



```
mlhdlc_temp_dir = [tempdir 'mlhdlc_so_viterbi'];  
clear mex;  
cd (mlhdlc_demo_dir);  
rmdir(mlhdlc_temp_dir, 's');
```

## HDL Code Generation from System Objects

This example shows how to generate HDL code from MATLAB code that contains System objects.

### MATLAB Design

The MATLAB code used in this example implements a simple symmetric FIR filter and uses the `dsp.Delay` System object to model state. This example also shows a MATLAB test bench that exercises the filter.

```
design_name = 'mlhdlc_sysobj_ex.m';
testbench_name = 'mlhdlc_sysobj_ex_tb.m';
```

Let us take a look at the MATLAB design.

```
type(design_name);
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% MATLAB design: Symmetric FIR Filter
%
% Design pattern covered in this example:
% Filter states modeled using DSP System object (dsp.Delay)
% Filter coefficients passed in as parameters to the design
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%#codegen
function [y_out, delayed_xout] = mlhdlc_sysobj_ex(x_in, h_in1, h_in2, h_in3)
% Symmetric FIR Filter

persistent h1 h2 h3 h4 h5 h6 h7 h8;
if isempty(h1)
    h1 = dsp.Delay('FrameBasedProcessing', false);
    h2 = dsp.Delay('FrameBasedProcessing', false);
    h3 = dsp.Delay('FrameBasedProcessing', false);
    h4 = dsp.Delay('FrameBasedProcessing', false);
    h5 = dsp.Delay('FrameBasedProcessing', false);
    h6 = dsp.Delay('FrameBasedProcessing', false);
    h7 = dsp.Delay('FrameBasedProcessing', false);
```

```
        h8 = dsp.Delay('FrameBasedProcessing', false);
    end

    h1p = step(h1, x_in);
    h2p = step(h2, h1p);
    h3p = step(h3, h2p);
    h4p = step(h4, h3p);
    h5p = step(h5, h4p);
    h6p = step(h6, h5p);
    h7p = step(h7, h6p);
    h8p = step(h8, h7p);

    a1 = h1p + h8p;
    a2 = h2p + h7p;
    a3 = h3p + h6p;
    a4 = h4p + h5p;

    m1 = h_in1 * a1;
    m2 = h_in2 * a2;
    m3 = h_in3 * a3;
    m4 = h_in4 * a4;

    a5 = m1 + m2;
    a6 = m3 + m4;

    % filtered output
    y_out = a5 + a6;
    % delayout input signal
    delayed_xout = h8p;

end

type(testbench_name);
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% MATLAB test bench for the FIR filter
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
clear mlhdlc_sysobj_ex;

x_in = cos(2.*pi.*(0:0.001:2).*(1+(0:0.001:2).*75)).';

h1 = -0.1339;
h2 = -0.0838;
h3 = 0.2026;
h4 = 0.4064;

len = length(x_in);
y_out_sysobj = zeros(1,len);
x_out_sysobj = zeros(1,len);
a = 10;

for ii=1:len
    data = x_in(ii);
    % call to the design 'sfir' that is targeted for hardware
    [y_out_sysobj(ii), x_out_sysobj(ii)] = mlhdlc_sysobj_ex(data, h1, h2, h3, h4, a);
end

figure('Name', [mfilename, '_plot']);
subplot(2,1,1);
plot(1:len,x_in); title('Input signal with noise');
subplot(2,1,2);
plot(1:len,y_out_sysobj); title('Filtered output signal');
```

### **Create a New Folder and Copy Relevant Files**

Execute the following lines of code to copy the necessary example files into a temporary folder.

```
mlhdlc_demo_dir = fullfile(matlabroot, 'toolbox', 'hdlcoder', 'hdlcoderdemo');
mlhdlc_temp_dir = [tempdir 'mlhdlc_sysobj_intro'];

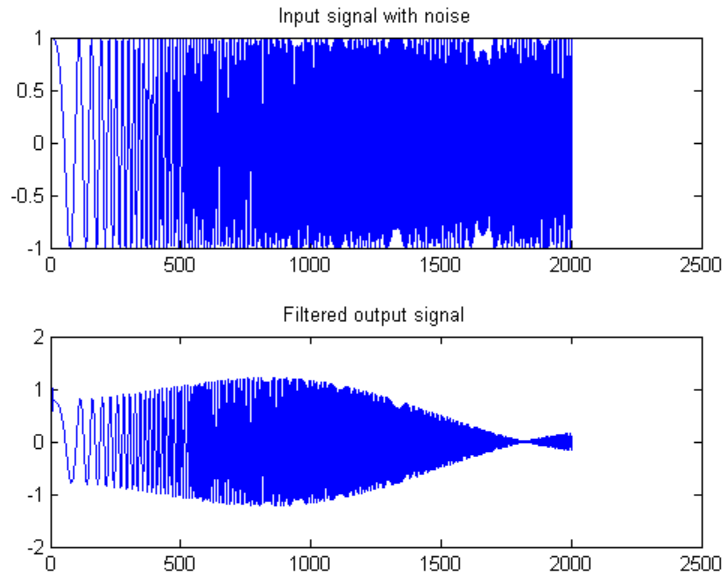
% Create a temporary folder and copy the MATLAB files.
cd(tempdir);
[~, ~, ~] = rmdir(mlhdlc_temp_dir, 's');
```

```
mkdir(mlhdlc_temp_dir);  
cd(mlhdlc_temp_dir);  
  
copyfile(fullfile(mlhdlc_demo_dir, design_name), mlhdlc_temp_dir);  
copyfile(fullfile(mlhdlc_demo_dir, testbench_name), mlhdlc_temp_dir);
```

### Simulate the Design

Simulate the design with the test bench prior to code generation to make sure there are no runtime errors.

```
mlhdlc_sysobj_ex_tb
```



### Create a New HDL Coder™ Project

To create a new project, enter the following command:

```
coder -hdlcoder -new mlhdlc_sysobj_prj
```

Next, add the file 'mlhdlc\_sysobj\_ex.m' to the project as the MATLAB Function and 'mlhdlc\_sysobj\_ex\_tb.m' as the MATLAB Test Bench.

You can refer to the Getting Started with MATLAB to HDL Workflow tutorial for a more complete tutorial on creating and populating MATLAB HDL Coder projects.

### **Run Fixed-Point Conversion and HDL Code Generation**

Launch the Workflow Advisor. In the Workflow Advisor, right-click the 'Code Generation' step. Choose the option 'Run to selected task' to run all the steps from the beginning through HDL code generation.

Examine the generated HDL code by clicking the links in the log window.

### **Supported System objects**

Refer to the documentation for a list of System objects supported for HDL code generation.

### **Clean up the Generated Files**

Run the following commands to clean up the temporary project folder.

```
mlhdlc_demo_dir = fullfile(matlabroot, 'toolbox', 'hdlcoder', 'hdlcoderdemo');
mlhdlc_temp_dir = [tempdir 'mlhdlc_sysobj_intro'];
clear mex;
cd (mlhdlc_demo_dir);
rmdir(mlhdlc_temp_dir, 's');
```

## Fixed-Point Bitwise Functions

### In this section...

“Overview” on page 17-69

“Bitwise Functions Supported for HDL Code Generation” on page 17-69

### Overview

HDL Coder supports many bitwise functions that operate on fixed-point integers of arbitrary length. For more information about these bitwise functions, see “Bitwise Operations” in the Fixed-Point Toolbox documentation.

This section describes HDL code generation support for these functions. “Bitwise Functions Supported for HDL Code Generation” on page 17-69 summarizes the supported functions, with notes that describe considerations specific to HDL code generation. “Bit Slicing and Bit Concatenation” on page 1-46 and “Shift and Rotate Without Saturation Or Rounding Logic” on page 1-43 provide usage examples, with corresponding MATLAB and generated HDL code.

### Bitwise Functions Supported for HDL Code Generation

The following table summarizes MATLAB bitwise functions that are supported for HDL code generation. The Description column notes considerations that are specific to HDL. The following conventions are used in the table:

- *a, b*: Denote fixed-point integer operands.
- *idx*: Denotes an index to a bit within an operand. Indexes can be scalar or vector, depending on the function.

MATLAB code uses 1-based indexing conventions. In generated HDL code, such indexes are converted to zero-based indexing conventions.

- *lidx*, *ridx*: denote indexes to the left and right boundaries delimiting bit fields. Indexes can be scalar or vector, depending on the function.
- *val*: Denotes a Boolean value.

**Note** Indexes, operands, and values passed as arguments bitwise functions can be scalar or vector, depending on the function. For information on the individual functions, see “Bitwise Operations” in the Fixed-Point Toolbox documentation.

<b>MATLAB Syntax</b>	<b>Description</b>	<b>See Also</b>
<code>bitand(a, b)</code>	Bitwise AND	<code>bitand</code>
<code>bitandreduce(a, lidx, ridx)</code>	<p>Bitwise AND of a field of consecutive bits within <code>a</code>. The field is delimited by <code>lidx</code>, <code>ridx</code>.</p> <p>Output data type: <code>ufix1</code></p> <p>For VHDL®, generates the bitwise AND operator operating on a set of individual slices</p> <p>For Verilog®, generates the reduce operator:</p> <p><code>&amp;a[lidx:ridx]</code></p>	<code>bitandreduce</code>
<code>bitcmp(a)</code>	Bitwise complement	<code>bitcmp</code>
<code>bitconcat(a, b)</code> <code>bitconcat([a_vector])</code> <code>bitconcat(a, b,c,d,...)</code>	<p>Concatenate fixed-point operands. Operands can be of different signs.</p> <p>Output data type: <code>ufixN</code>, where <code>N</code> is the sum of the word lengths of <code>a</code> and <code>b</code>.</p> <p>For VHDL, generates the concatenation operator: <code>(a &amp; b)</code></p> <p>For Verilog, generates the concatenation operator: <code>{a , b}</code></p>	<code>bitconcat</code>



<b>MATLAB Syntax</b>	<b>Description</b>	<b>See Also</b>
<code>bitget(a,idx)</code>	<p>Access a bit at position <code>idx</code>.</p> <p>For VHDL, generates the slice operator: <code>a(idx)</code></p> <p>For Verilog, generates the slice operator: <code>a[idx]</code></p>	<code>bitget</code>
<code>bitor(a, b)</code>	Bitwise OR	<code>bitor</code>
<code>bitorreduce(a, lidx, ridx)</code>	<p>Bitwise OR of a field of consecutive bits within <code>a</code>. The field is delimited by <code>lidx</code> and <code>ridx</code>.</p> <p>Output data type: <code>ufix1</code></p> <p>For VHDL, generates the bitwise OR operator operating on a set of individual slices.</p> <p>For Verilog, generates the reduce operator:</p> <p><code> a[lidx:ridx]</code></p>	<code>bitorreduce</code>
<code>bitset(a, idx, val)</code>	<p>Set or clear bit(s) at position <code>idx</code>.</p> <p>If <code>val = 0</code>, clears the indicated bit(s). Otherwise, sets the indicated bits.</p>	<code>bitset</code>
<code>bitreplicate(a, n)</code>	Concatenate bits of <code>fi</code> object <code>a</code> <code>n</code> times	<code>bitreplicate</code>

MATLAB Syntax	Description	See Also
<code>bitrol(a, idx)</code>	<p>Rotate left.</p> <p><code>idx</code> must be a positive integer. The value of <code>idx</code> can be greater than the word length of <code>a</code>. <code>idx</code> is normalized to <code>mod(idx, wlen)</code>. <code>wlen</code> is the word length of <code>a</code>.</p> <p>For VHDL, generates the <code>rol</code> operator.</p> <p>For Verilog, generates the following expression (where <code>wl</code> is the word length of <code>a</code>):</p> $a \ll idx \    \ a \gg wl - idx$	<code>bitrol</code>
<code>bitror(a, idx)</code>	<p>Rotate right.</p> <p><code>idx</code> must be a positive integer. The value of <code>idx</code> can be greater than the word length of <code>a</code>. <code>idx</code> is normalized to <code>mod(idx, wlen)</code>. <code>wlen</code> is the word length of <code>a</code>.</p> <p>For VHDL, generates the <code>ror</code> operator.</p> <p>For Verilog, generates the following expression (where <code>wl</code> is the word length of <code>a</code>):</p> $a \gg idx \    \ a \ll wl - idx$	<code>bitror</code>
<code>bitset(a, idx, val)</code>	<p>Set or clear bit(s) at position <code>idx</code>.</p> <p>If <code>val = 0</code>, clears the indicated bit(s). Otherwise, sets the indicated bits.</p>	<code>bitset</code>

MATLAB Syntax	Description	See Also
bitshift(a, idx)	<p><b>Note:</b> For efficient HDL code generation, use <code>bitsll</code>, <code>bitsrl</code>, or <code>bitsra</code> <i>instead</i> of <code>bitshift</code>.</p> <p>Shift left or right, based on the positive or negative integer value of <code>idx</code>.</p> <p><code>idx</code> must be an integer.</p> <p>For positive values of <code>idx</code>, shift left <code>idx</code> bits.</p> <p>For negative values of <code>idx</code>, shift right <code>idx</code> bits.</p> <p>If <code>idx</code> is a variable, generated code contains logic for both left shift and right shift.</p> <p>Result values saturate if the <code>overflowMode</code> of <code>a</code> is set to <code>saturate</code>.</p>	bitshift
bitsliceget(a, lidx, ridx)	<p>Access consecutive set of bits from <code>lidx</code> to <code>ridx</code>.</p> <p>Output data type: <code>ufixN</code>, where <math>N = \text{ridx} - \text{lidx} + 1</math>.</p>	bitsliceget
bitsll(a, idx)	<p>Shift left logical.</p> <p><code>idx</code> must be a scalar within the range</p> $0 \leq \text{idx} < \text{wl}$ <p><code>wl</code> is the word length of <code>a</code>.</p> <p>Overflow and rounding modes of input operand <code>a</code> are ignored.</p> <p>Generates <code>sll</code> operator in VHDL.</p> <p>Generates <code>&lt;&lt;</code> operator in Verilog.</p>	bitsll

<b>MATLAB Syntax</b>	<b>Description</b>	<b>See Also</b>
<code>bitsra(a, idx)</code>	<p>Shift right arithmetic.</p> <p><code>idx</code> must be a scalar within the range</p> $0 \leq \text{idx} < w1$ <p><code>w1</code> is the word length of <code>a</code>,</p> <p>Overflow and rounding modes of input operand <code>a</code> are ignored.</p> <p>Generates <code>sra</code> operator in VHDL.</p> <p>Generates <code>&gt;&gt;&gt;</code> operator in Verilog.</p>	<code>bitsra</code>
<code>bitsrl(a, idx)</code>	<p>Shift right logical.</p> <p><code>idx</code> must be a scalar within the range</p> $0 \leq \text{idx} < w1$ <p><code>w1</code> is the word length of <code>a</code>.</p> <p>Overflow and rounding modes of input operand <code>a</code> are ignored.</p> <p>Generates <code>srl</code> operator in VHDL.</p> <p>Generates <code>&gt;&gt;</code> operator in Verilog.</p>	<code>bitsrl</code>
<code>bitxor(a, b)</code>	Bitwise XOR	<code>bitxor</code>

<b>MATLAB Syntax</b>	<b>Description</b>	<b>See Also</b>
<code>bitxorreduce(a, lidx, ridx)</code>	<p>Bitwise XOR reduction.</p> <p>Bitwise XOR of a field of consecutive bits within <code>a</code>. The field is delimited by <code>lidx</code> and <code>ridx</code>.</p> <p>Output data type: <code>ufix1</code></p> <p>For VHDL, generates a set of individual slices.</p> <p>For Verilog, generates the reduce operator:</p> <p><code>^a[lidx:ridx]</code></p>	<code>bitxorreduce</code>
<code>getlsb(a)</code>	Return value of LSB.	<code>getlsb</code>
<code>getmsb(a)</code>	Return value of MSB.	<code>getmsb</code>

## Complex Data Type Support

### In this section...

“Declaring Complex Signals” on page 17-50

“Conversion Between Complex and Real Signals” on page 17-51

“Arithmetic Operations on Complex Numbers” on page 17-52

“Support for Vectors of Complex Numbers” on page 17-56

“Other Operations on Complex Numbers” on page 17-57

### Declaring Complex Signals

The following MATLAB code declares several local complex variables.  $x$  and  $y$  are declared by complex constant assignment;  $z$  is created using the using the `complex()` function.

```
function [x,y,z] = fcn

% create 8 bit complex constants
x = uint8(1 + 2i);
y = uint8(3 + 4j);
z = uint8(complex(5, 6));
```

The following code example shows VHDL code generated from the previous MATLAB code.

```
ENTITY complex_decl IS
    PORT (
        clk : IN std_logic;
        clk_enable : IN std_logic;
        reset : IN std_logic;
        x_re : OUT std_logic_vector(7 DOWNTO 0);
        x_im : OUT std_logic_vector(7 DOWNTO 0);
        y_re : OUT std_logic_vector(7 DOWNTO 0);
        y_im : OUT std_logic_vector(7 DOWNTO 0);
        z_re : OUT std_logic_vector(7 DOWNTO 0);
        z_im : OUT std_logic_vector(7 DOWNTO 0));
END complex_decl;
```

```

ARCHITECTURE fsm_SFHDH OF complex_decl IS

BEGIN
    x_re <= std_logic_vector(to_unsigned(1, 8));
    x_im <= std_logic_vector(to_unsigned(2, 8));
    y_re <= std_logic_vector(to_unsigned(3, 8));
    y_im <= std_logic_vector(to_unsigned(4, 8));
    z_re <= std_logic_vector(to_unsigned(5, 8));
    z_im <= std_logic_vector(to_unsigned(6, 8));
END fsm_SFHDH;

```

As shown in the example, complex inputs, outputs and local variables declared in MATLAB code expand into real and imaginary signals. The naming conventions for these derived signals are:

- Real components have the same name as the original complex signal, suffixed with the default string `'_re'` (for example, `x_re`). To specify a different suffix, set the **Complex real part postfix** option (or the corresponding `ComplexRealPostfix` CLI property).
- Imaginary components have the same name as the original complex signal, suffixed with the string `'_im'` (for example, `x_im`). To specify a different suffix, set the **Complex imaginary part postfix** option (or the corresponding `ComplexImagPostfix` CLI property).

A complex variable declared in MATLAB code remains complex during the entire length of the program.

## Conversion Between Complex and Real Signals

The MATLAB code provides access to the fields of a complex signal via the `real()` and `imag()` functions, as shown in the following code.

```

function [Re_part, Im_part]= fcn(c)
% Output real and imaginary parts of complex input signal

Re_part = real(c);
Im_part = imag(c);

```

The coder supports these constructs, accessing the corresponding real and imaginary signal components in generated HDL code. In the following Verilog code example, the MATLAB complex signal variable `c` is flattened into the signals `c_re` and `c_im`. Each of these signals is assigned to the output variables `Re_part` and `Im_part`, respectively.

```
module Complex_To_Real_Imag (clk, clk_enable, reset, c_re, c_im, Re_part, Im_part );

    input clk;
    input clk_enable;
    input reset;
    input [3:0] c_re;
    input [3:0] c_im;
    output [3:0] Re_part;
    output [3:0] Im_part;

    // Output real and imaginary parts of complex input signal
    assign Re_part = c_re;
    assign Im_part = c_im;
```

## Arithmetic Operations on Complex Numbers

When generating HDL code, the coder supports the following arithmetic operators for complex numbers composed of base types (integer, fixed-point, double):

- Addition (+)
- Subtraction (-)
- Multiplication (\*)

The coder supports division only for the Fixed-Point Toolbox `divide` function (see `divide`). The `divide` function is supported only if the base type of both complex operands is fixed-point.

As shown in the following example, the default sum and product mode for fixed-point objects is `FullPrecision`, and the `CastBeforeSum` property defaults to `true`.

```
fm = hdlfmath
```



```

fm =

        RoundMode: floor
      OverflowMode: wrap
        ProductMode: FullPrecision
MaxProductWordLength: 128
        SumMode: FullPrecision
MaxSumWordLength: 128
      CastBeforeSum: true

```

Given fixed-point operands, the coder follows full-precision cast before sum semantics. Each addition or subtraction increases the result width by one bit. Further casting is required to bring the results back to a smaller bit width.

In the following example function, two complex operands (with real and imaginary `ufix4` components) are summed, with a complex result having real and imaginary `ufix5` components. The result is then cast back to the original bit width.

```

function z = fcn(x, y)
% addition of two complex numbers x,y of type 'ufix4'

% x+y will have 'ufix5' type
z = x+y;

% to cast the result back to 'ufix4'
% z = fi(x + y, numerictype(x), fimath(x));

```

The following example shows VHDL code generated from this function.

```

ENTITY complex_add_entity IS
  PORT (
    clk : IN std_logic;
    clk_enable : IN std_logic;
    reset : IN std_logic;
    x_re : IN std_logic_vector(3 DOWNTO 0);
    x_im : IN std_logic_vector(3 DOWNTO 0);
    y_re : IN std_logic_vector(3 DOWNTO 0);
    y_im : IN std_logic_vector(3 DOWNTO 0);

```

```

        z_re : OUT std_logic_vector(4 DOWNTO 0);
        z_im : OUT std_logic_vector(4 DOWNTO 0));
END complex_add_entity;

ARCHITECTURE fsm_SFHDL OF complex_add_entity IS

BEGIN
    -- addition of two complex numbers x,y of type 'ufix4'
    -- x+y will have 'ufix5' type
    z_re <= std_logic_vector(resize(unsigned(x_re), 5) +
                            resize(unsigned(y_re), 5));

    z_im <= std_logic_vector(resize(unsigned(x_im), 5) +
                            resize(unsigned(y_im), 5));

    -- to cast the result back to 'ufix4' use
    -- z = fi(x + y, numericity(x), fimath(x));

END fsm_SFHDL;

```

Similarly, for the product operation in FullPrecision mode, the result bit width increases to the sum of the lengths of the individual operands. Further casting is required to bring the results back to a smaller bit width.

The following example function shows how the product of two complex operands (with real and imaginary ufix4 components) can be cast back to the original bit width.

```

function z = fcn(x, y)
% Multiplication of two complex numbers x,y of type 'ufix4'

% x*y will have 'ufix8' type
z = x * y;

% to cast the result back to 'ufix4'
% z = fi(x * y, numericity(x), fimath(x));

```

The following example shows VHDL code generated from this function.

```

ENTITY complex_mul IS

```

```

PORT (
    clk : IN std_logic;
    clk_enable : IN std_logic;
    reset : IN std_logic;
    x_re : IN std_logic_vector(3 DOWNTO 0);
    x_im : IN std_logic_vector(3 DOWNTO 0);
    y_re : IN std_logic_vector(3 DOWNTO 0);
    y_im : IN std_logic_vector(3 DOWNTO 0);
    z_re : OUT std_logic_vector(8 DOWNTO 0);
    z_im : OUT std_logic_vector(8 DOWNTO 0));
END complex_mul;

ARCHITECTURE fsm_SFHDL OF complex_mul IS

    SIGNAL pr1 : unsigned(7 DOWNTO 0);
    SIGNAL pr2 : unsigned(7 DOWNTO 0);
    SIGNAL pr1in : unsigned(8 DOWNTO 0);
    SIGNAL pr2in : unsigned(8 DOWNTO 0);
    SIGNAL pre : unsigned(8 DOWNTO 0);
    SIGNAL pi1 : unsigned(7 DOWNTO 0);
    SIGNAL pi2 : unsigned(7 DOWNTO 0);
    SIGNAL pi1in : unsigned(8 DOWNTO 0);
    SIGNAL pi2in : unsigned(8 DOWNTO 0);
    SIGNAL pim : unsigned(8 DOWNTO 0);

BEGIN
    -- addition of two complex numbers x,y of type 'ufix4'
    -- x*y will have 'ufix8' type
    pr1 <= unsigned(x_re) * unsigned(y_re);
    pr2 <= unsigned(x_im) * unsigned(y_im);
    pr1in <= resize(pr1, 9);
    pr2in <= resize(pr2, 9);
    pre <= pr1in - pr2in;
    pi1 <= unsigned(x_re) * unsigned(y_im);
    pi2 <= unsigned(x_im) * unsigned(y_re);
    pi1in <= resize(pi1, 9);
    pi2in <= resize(pi2, 9);
    pim <= pi1in + pi2in;
    z_re <= std_logic_vector(pre);

```

```
z_im <= std_logic_vector(pim);  
-- to cast the result back to 'ufix4'  
-- z = fi(x * y, numericity(x), fimath(x));  
END fsm_SFHDL;
```

## Support for Vectors of Complex Numbers

You can generate HDL code for vectors of complex numbers. Like scalar complex numbers, vectors of complex numbers are flattened down to vectors of real and imaginary parts in generated HDL code.

For example in the following script `t` is a complex vector variable of base type `ufix4` and size `[1,2]`.

```
function y = fcn(u1, u2)  
  
t = [u1 u2];  
y = t+1;
```

In the generated HDL code the variable `t` is broken down into real and imaginary parts with the same two-element array. .

```
VARIABLE t_re : vector_of_unsigned4(0 TO 3);  
VARIABLE t_im : vector_of_unsigned4(0 TO 3);
```

The real and imaginary parts of the complex number have the same vector of type `ufix4`, as shown in the following code.

```
TYPE vector_of_unsigned4 IS ARRAY (NATURAL RANGE <>) OF unsigned(3 DOWNT0 0);
```

Complex vector-based operations (+, -, \* etc.,) are similarly broken down to vectors of real and imaginary parts. Operations are performed independently on the elements of such vectors, following MATLAB semantics for vectors of complex numbers.

In both VHDL and Verilog code generated from MATLAB code, complex vector ports are always flattened. If complex vector variables appear on inputs and outputs, real and imaginary vector components are further flattened to scalars.

In the following code, `u1` and `u2` are scalar complex numbers and `y` is a vector of complex numbers.

```
function y = fcn(u1, u2)

t = [u1 u2];
y = t+1;
```

This generates the following port declarations in a VHDL entity definition.

```
ENTITY _MATLAB_Function IS
  PORT (
    clk : IN std_logic;
    clk_enable : IN std_logic;
    reset : IN std_logic;
    u1_re : IN vector_of_std_logic_vector4(0 TO 1);
    u1_im : IN vector_of_std_logic_vector4(0 TO 1);
    u2_re : IN vector_of_std_logic_vector4(0 TO 1);
    u2_im : IN vector_of_std_logic_vector4(0 TO 1);
    y_re : OUT vector_of_std_logic_vector32(0 TO 3);
    y_im : OUT vector_of_std_logic_vector32(0 TO 3));
END _MATLAB_Function;
```

## Other Operations on Complex Numbers

The coder supports the following functions with complex operands:

- `complex`
- `real`
- `imag`
- `conj`
- `transpose`
- `ctranspose`
- `isnumeric`
- `isreal`
- `isscalar`

The `isreal` function, which returns 0 for complex numbers, is particularly useful for writing functions that behave differently based on whether the input is a complex or real signal.

```
function y = fcn(u)

% output is same as input if 'u' is real
% output is conjugate of input if 'u' is complex

if isreal(u)
    y = u;
else
    y = conj(u);
end
```

For detailed information on these functions, see “Functions Supported for Code Acceleration or Generation”.

## Shift and Rotate Without Saturation Or Rounding Logic

HDL Coder supports shift and rotate functions that mimic HDL-specific operators without saturation and rounding logic.

The following code implements a barrel shifter/rotator that performs a selected operation (based on the mode argument) on a fixed-point input operand.

```
function y = fcn(u, mode)
% Multi Function Barrel Shifter/Rotator

% fixed width shift operation
fixed_width = uint8(3);

switch mode
    case 1
        % shift left logical
        y = bitsll(u, fixed_width);
    case 2
        % shift right logical
        y = bitsrl(u, fixed_width);
    case 3
        % shift right arithmetic
        y = bitsra(u, fixed_width);
    case 4
        % rotate left
        y = bitrol(u, fixed_width);
    case 5
        % rotate right
        y = bitror(u, fixed_width);
    otherwise
        % do nothing
        y = u;
end
```

In VHDL code generated for this function, the shift and rotate functions map directly to shift and rotate instructions in VHDL.

```
CASE mode IS
    WHEN "00000001" =>
```

```

        -- shift left logical
        -- '<S2>:1:8'
        cr := signed(u) sll 3;
        y <= std_logic_vector(cr);
    WHEN "00000010" =>
        -- shift right logical
        -- '<S2>:1:11'
        b_cr := signed(u) srl 3;
        y <= std_logic_vector(b_cr);
    WHEN "00000011" =>
        -- shift right arithmetic
        -- '<S2>:1:14'
        c_cr := SHIFT_RIGHT(signed(u) , 3);
        y <= std_logic_vector(c_cr);
    WHEN "00000100" =>
        -- rotate left
        -- '<S2>:1:17'
        d_cr := signed(u) rol 3;
        y <= std_logic_vector(d_cr);
    WHEN "00000101" =>
        -- rotate right
        -- '<S2>:1:20'
        e_cr := signed(u) ror 3;
        y <= std_logic_vector(e_cr);
    WHEN OTHERS =>
        -- do nothing
        -- '<S2>:1:23'
        y <= u;
    END CASE;

```

The corresponding Verilog code is similar, except that Verilog does not have native operators for rotate instructions.

```

    case ( mode)
    1 :
        begin
            // shift left logical
            // '<S2>:1:8'
            cr = u <<< 3;
            y = cr;

```



```
    end
2 :
    begin
        // shift right logical
        //'<S2>:1:11'
        b_cr = u >> 3;
        y = b_cr;
    end
3 :
    begin
        // shift right arithmetic
        //'<S2>:1:14'
        c_cr = u >>> 3;
        y = c_cr;
    end
4 :
    begin
        // rotate left
        //'<S2>:1:17'
        d_cr = {u[12:0], u[15:13]};
        y = d_cr;
    end
5 :
    begin
        // rotate right
        //'<S2>:1:20'
        e_cr = {u[2:0], u[15:3]};
        y = e_cr;
    end
default :
    begin
        // do nothing
        //'<S2>:1:23'
        y = u;
    end
endcase
```

## Bit Slicing and Bit Concatenation

This section describes how to use the functions `bitsliceget` and `bitconcat` to access and manipulate bit slices (fields) in a fixed-point or integer word. As an example, consider the operation of swapping the upper and lower 4-bit nibbles of an 8-bit byte. The following example accomplishes this task without resorting to traditional mask-and-shift techniques.

```
function y = fcn(u)
% NIBBLE SWAP
y = bitconcat(
    bitsliceget(u, 4, 1),
    bitsliceget(u, 8, 5));
```

The `bitsliceget` and `bitconcat` functions map directly to `slice` and `concat` operators in both VHDL and Verilog.

The following listing shows the corresponding generated VHDL code.

```
ENTITY fcn IS
    PORT (
        clk : IN std_logic;
        clk_enable : IN std_logic;
        reset : IN std_logic;
        u : IN std_logic_vector(7 DOWNTO 0);
        y : OUT std_logic_vector(7 DOWNTO 0));
END nibble_swap_7b;
```

```
ARCHITECTURE fsm_SFHDL OF fcn IS
```

```
BEGIN
    -- NIBBLE SWAP
    y <= u(3 DOWNTO 0) & u(7 DOWNTO 4);
END fsm_SFHDL;
```

The following listing shows the corresponding generated Verilog code.

```
module fcn (clk, clk_enable, reset, u, y );
    input clk;
    input clk_enable;
    input reset;
    input [7:0] u;
    output [7:0] y;

    // NIBBLE SWAP
    assign y = {u[3:0], u[7:4]};

endmodule
```

## Fixed-Point Run-Time Library Functions

HDL code generation support for fixed-point run-time library functions from the Fixed-Point Toolbox is summarized in the following table. See “Fixed-Point Function Limitations” on page 17-85 for general limitations of fixed-point run-time library functions for code generation.

Function	Restrictions
abs	N/A
add	N/A
all	N/A
any	N/A
bitand	Not supported for slope-bias scaled <code>fi</code> objects.
bitandreduce	N/A
bitcmp	N/A
bitconcat	N/A
bitget	N/A
bitor	Not supported for slope-bias scaled <code>fi</code> objects.
bitorreduce	N/A
bitreplicate	N/A
bitrol	N/A
bitror	N/A
bitset	N/A
bitshift	N/A
bitsliceget	N/A
bitsll	N/A
bitsra	N/A
bitsrl	N/A
bitxor	Not supported for slope-bias scaled <code>fi</code> objects.

<b>Function</b>	<b>Restrictions</b>
bitxorreduce	N/A
ceil	N/A
complex	N/A
conj	N/A
conv	<ul style="list-style-type: none"> <li>• Variable-sized inputs are only supported when the <code>SumMode</code> property of the governing <code>fimath</code> is set to <code>Specify precision</code> or <code>Keep LSB</code>.</li> <li>• For variable-sized signals, you may see different results between generated code and MATLAB. <ul style="list-style-type: none"> <li>▪ In the generated code, the output for variable-sized signals is always computed using the <code>SumMode</code> property of the governing <code>fimath</code>.</li> <li>▪ In MATLAB, the output for variable-sized signals is computed using the <code>SumMode</code> property of the governing <code>fimath</code> when both inputs are nonscalar. However, if either input is a scalar, MATLAB computes the output using the <code>ProductMode</code> of the governing <code>fimath</code>.</li> </ul> </li> </ul>
convergent	N/A
cordicabs	Variable-size signals are not supported.
cordicangle	Variable-size signals are not supported.
cordicatan2	Variable-size signals are not supported.
cordiccart2pol	Variable-size signals are not supported.
cordiccxp	Variable-size signals are not supported.
cordiccos	Variable-size signals are not supported.
cordicpol2cart	Variable-size signals are not supported.
cordicrotate	Variable-size signals are not supported.
cordicsin	Variable-size signals are not supported.

<b>Function</b>	<b>Restrictions</b>
cordicsincos	Variable-size signals are not supported.
ctranspose	N/A
diag	If supplied, the index, $k$ , must be a real and scalar integer value that is not a <code>fi</code> object.
disp	Not supported for HDL code generation.
divide	<ul style="list-style-type: none"> <li>• For HDL Code generation, the divisor must be a constant and a power of two.</li> <li>• Any non-<code>fi</code> input must be constant; that is, its value must be known at compile time so that it can be cast to a <code>fi</code> object.</li> <li>• Complex and imaginary divisors are not supported.</li> <li>• Code generation in MATLAB does not support the syntax <code>T.divide(a,b)</code>.</li> </ul>
double	N/A
end	N/A
eps	<ul style="list-style-type: none"> <li>• Supported for scalar fixed-point signals only.</li> <li>• Supported for scalar, vector, and matrix, <code>fi</code> single and <code>fi</code> double signals.</li> </ul>
eq	Not supported for fixed-point signals with different biases.

Function	Restrictions
fi	<ul style="list-style-type: none"> <li>• Use to create a fixed-point constant or variable in the generated code.</li> <li>• The default constructor syntax without any input arguments is not supported.</li> <li>• The syntax <code>fi('PropertyName',PropertyValue...)</code> is not supported. To use property name/property value pairs, you must first specify the value <code>v</code> of the <code>fi</code> object as in <code>fi(v,'PropertyName',PropertyValue...)</code>.</li> <li>• Works for all input values when complete <code>numericType</code> information of the <code>fi</code> object is provided.</li> <li>• Works only for constant input values (value of input must be known at compile time) when complete <code>numericType</code> information of the <code>fi</code> object is not specified.</li> <li>• <code>numericType</code> object information must be available for nonfixed-point Simulink® inputs.</li> </ul>
fimath	<ul style="list-style-type: none"> <li>• Fixed-point signals coming in to a MATLAB Function block from Simulink are assigned a <code>fimath</code> object. You define this object in the MATLAB Function block dialog in the Model Explorer.</li> <li>• Use to create <code>fimath</code> objects in the generated code.</li> </ul>
fix	N/A
floor	N/A
ge	Not supported for fixed-point signals with different biases.
get	Not supported for HDL code generation.
getlsb	N/A

<b>Function</b>	<b>Restrictions</b>
getmsb	N/A
gt	Not supported for fixed-point signals with different biases.
horzcat	N/A
imag	N/A
int8, int16, int32	N/A
iscolumn	N/A
isempty	N/A
isequal	N/A
isfi	N/A
isfimath	N/A
isfimathlocal	N/A
isfinite	N/A
isinf	N/A
isnan	N/A
isnumeric	N/A
isnumericitype	N/A
isreal	N/A
isrow	N/A
isscalar	N/A
issigned	N/A
isvector	N/A
le	Not supported for fixed-point signals with different biases.
length	N/A
logical	N/A
lowerbound	N/A



Function	Restrictions
lsb	<ul style="list-style-type: none"> <li>• Supported for scalar fixed-point signals only.</li> <li>• Supported for scalar, vector, and matrix, <code>fi</code> single and double signals.</li> </ul>
lt	Not supported for fixed-point signals with different biases.
max	N/A
mean	N/A
median	N/A
min	N/A
minus	Any non- <code>fi</code> input must be constant; that is, its value must be known at compile time so that it can be cast to a <code>fi</code> object.
mpower	<ul style="list-style-type: none"> <li>• The exponent input, <code>k</code>, must be constant; that is, its value must be known at compile time.</li> <li>• Variable-sized inputs are only supported when the <code>SumMode</code> property of the governing <code>fimath</code> is set to <code>Specify precision</code> or <code>Keep LSB</code>.</li> <li>• For variable-sized signals, you may see different results between the generated code and MATLAB. <ul style="list-style-type: none"> <li>▪ In the generated code, the output for variable-sized signals is always computed using the <code>SumMode</code> property of the governing <code>fimath</code>.</li> <li>▪ In MATLAB, the output for variable-sized signals is computed using the <code>SumMode</code> property of the governing <code>fimath</code> when the first input, <code>a</code>, is nonscalar. However, when <code>a</code> is a scalar, MATLAB computes the output using the <code>ProductMode</code> of the governing <code>fimath</code>.</li> </ul> </li> </ul>

Function	Restrictions
mpy	When you provide complex inputs to the mpy function inside of a MATLAB Function block, you must declare the input as complex before running the simulation. To do so, go to the <b>Ports and data manager</b> and set the <b>Complexity</b> parameter for all known complex inputs to On.
mrdivide	N/A
mtimes	<ul style="list-style-type: none"> <li>• Any non-fi input must be constant; that is, its value must be known at compile time so that it can be cast to a fi object.</li> <li>• Variable-sized inputs are only supported when the SumMode property of the governing fimath is set to Specify precision or Keep LSB.</li> <li>• For variable-sized signals, you may see different results between the generated code and MATLAB. <ul style="list-style-type: none"> <li>▪ In the generated code, the output for variable-sized signals is always computed using the SumMode property of the governing fimath.</li> <li>▪ In MATLAB, the output for variable-sized signals is computed using the SumMode property of the governing fimath when both inputs are nonscalar. However, if either input is a scalar, MATLAB computes the output using the ProductMode of the governing fimath.</li> </ul> </li> </ul>
ndims	N/A
ne	Not supported for fixed-point signals with different biases.
nearest	N/A

<b>Function</b>	<b>Restrictions</b>
numberofelements	numberofelements and numel both work the same as MATLAB numel for fi objects in the generated code.
numericitype	<ul style="list-style-type: none"> <li>• Fixed-point signals coming in to a MATLAB Function block from Simulink are assigned a numericitype object that is populated with the signal's data type and scaling information.</li> <li>• Returns the data type when the input is a nonfixed-point signal.</li> <li>• Use to create numericitype objects in generated code.</li> </ul>
permute	N/A
plus	Any non-fi input must be constant; that is, its value must be known at compile time so that it can be cast to a fi object.
pow2	Not supported for HDL code generation.
power	The exponent input, $k$ , must be constant; that is, its value must be known at compile time.
range	N/A
rdivide	N/A
real	Not supported for HDL code generation.
realmax	N/A
realmin	N/A
reinterpretcast	N/A
repmat	N/A
rescale	N/A
reshape	N/A
round	N/A
sfi	N/A

<b>Function</b>	<b>Restrictions</b>
sign	N/A
single	N/A
size	N/A
sort	N/A
sqrt	<ul style="list-style-type: none"> <li>• Complex and [Slope Bias] inputs error out.</li> <li>• Negative inputs yield a 0 result.</li> </ul>
storedInteger	N/A
storedIntegerToDouble	N/A
sub	N/A
subasgn	Supported data types for HDL code generation are listed in “Supported Data Types” on page 17-67
subsref	Supported data types for HDL code generation are listed in “Supported Data Types” on page 17-67
sum	Variable-sized inputs are only supported when the SumMode property of the governing fimath is set to Specify precision or Keep LSB.
times	<ul style="list-style-type: none"> <li>• Any non-fi input must be constant; that is, its value must be known at compile time so that it can be cast to a fi object.</li> <li>• When you provide complex inputs to the times function inside of a MATLAB Function block, you must declare the input as complex before running the simulation. To do so, go to the <b>Ports and data manager</b> and set the <b>Complexity</b> parameter for all known complex inputs to 0n.</li> </ul>
transpose	N/A
tril	If supplied, the index, <i>k</i> , must be a real and scalar integer value that is not a fi object.
triu	If supplied, the index, <i>k</i> , must be a real and scalar integer value that is not a fi object.

Function	Restrictions
<code>ufi</code>	N/A
<code>uint8, uint16, uint32</code>	N/A
<code>uminus</code>	N/A
<code>uplus</code>	N/A
<code>upperbound</code>	N/A
<code>vertcat</code>	N/A

## Fixed-Point Function Limitations

In addition to any function-specific limitations listed in the table, the following general limitations always apply to the use of Fixed-Point Toolbox functions in generated code or with `fiaccel`:

- `fipref` and quantizer objects are not supported.
- Dot notation is only supported for getting the values of `fimath` and `numericType` properties. Dot notation is not supported for `fi` objects, and it is not supported for setting properties.
- Word lengths greater than 128 bits are not supported.
- You cannot change the `fimath` or `numericType` of a given variable after that variable has been created.
- The `boolean` and `ScaledDouble` values of the `DataTypeMode` and `DataType` properties are not supported.
- For all `SumMode` property settings other than `FullPrecision`, the `CastBeforeSum` property must be set to `true`.
- The `numel` function returns the number of elements of `fi` objects in the generated code.
- When you compile code containing `fi` objects with nontrivial slope and bias scaling, you may see different results in generated code than you achieve by running the same code in MATLAB.

- All general limitations of C/C++ code generated from MATLAB apply. See “MATLAB Language Features Not Supported for C/C++ Code Generation” for more information.

## MATLAB Design Best Practices for HDL Code Generation

When you generate HDL code from your MATLAB design, you are converting an algorithm into an architecture that must meet hardware area and speed requirements.

For better HDL code and faster code generation, design your MATLAB code according to the following best practices:

- *Serialize your input and output data.* Parallel data processing structures require more hardware resources and a higher pin count.
- *Use add and subtract algorithms instead of algorithms that use functions like sin, divide, and modulo.* Add and subtract operations use fewer hardware resources.
- *Avoid large arrays and matrices.* Large arrays and matrices require more registers and RAM for storage.
- *Convert your code from floating-point to fixed-point.* Floating-point data types are inefficient for hardware realization. The coder provides an automated workflow for floating-point to fixed-point conversion.
- *Unroll loops.* Unroll loops to increase speed at the cost of higher area; unroll fewer loops and enable the loop streaming optimization to conserve area at the cost of lower throughput.
- *Verify your code readiness.* If you are generating code from the command line, verify your code readiness for code generation with the following command:

```
coder.screener('design_function_name')
```

If you use the HDL Workflow Advisor to generate code, this check runs automatically.

## **MATLAB Design Requirements for HDL Code Generation**

Your MATLAB design has the following requirements:

- MATLAB code within the design must be supported for HDL code generation.
- Inputs and outputs must not be matrices or structures.

For a MATLAB language support reference, including supported functions from the Fixed-Point Toolbox, see “MATLAB Algorithm Design”.



## What Is a MATLAB Test Bench?

A test bench is a MATLAB script or function that you write to test the algorithm in your MATLAB design function. The test bench varies the input data to the design to simulate real world conditions. It can also check that the output data meets design specifications.

The coder uses the data it gathers from running your test bench with your design to infer fixed-point data types for floating-point to fixed-point conversion. The coder also uses the data to generate HDL test data for verifying your generated code. For more information on how to write your test bench for the best results, see “MATLAB Test Bench Requirements and Best Practices” on page 1-62.

# MATLAB Test Bench Requirements and Best Practices

## MATLAB Test Bench Requirements

You can use any MATLAB data type and function in your test bench.

A MATLAB test bench has the following requirements:

- For floating-point to fixed-point conversion, the test bench must be a script or a function with no inputs.
- The inputs and outputs in your MATLAB design interface must use the same data types, sizes, and complexity in each call site in your test bench.
- If you enable the **Accelerate test bench for faster simulation** option in the Float-to-Fixed Workflow, the MATLAB constructs in your test bench loop must be compilable.

## MATLAB Test Bench Best Practices

Use the following MATLAB test bench best practices:

- *Design your test bench to cover the full numeric range of data that the design must handle.* The coder uses the data that it accumulates from running the test bench to infer fixed-point data types during floating-point to fixed-point conversion.

If you call the design function multiple times from your test bench, the coder uses the accumulated data from each instance to infer fixed-point types. Both the design and the test bench can call local functions within the file or other functions on the MATLAB path. The call to the design function can be at any level of your test bench hierarchy.

- *Before trying to generate code, run your test bench in MATLAB .* If simulation is slow, accelerate your test bench. To learn how to accelerate your simulation, see “Accelerate MATLAB Algorithms”.
- If you have a loop that calls your design function, use only compilable MATLAB constructs within the loop and enable the **Accelerate test bench for faster simulation** option.
- Before each test bench simulation run, use the `clear variables` command to reset your persistent variables.

To see an example of a test bench, enter this command:

```
showdemo mlhdlc_tutorial_float2fixed_files
```



# Code Generation

---

- “Create and Set Up Your Project” on page 2-2
- “Primary Function Input Specification” on page 2-6

## Create and Set Up Your Project

In this section...
“Create a New Project” on page 2-2
“Open an Existing Project” on page 2-4
“Add Files to the Project” on page 2-4

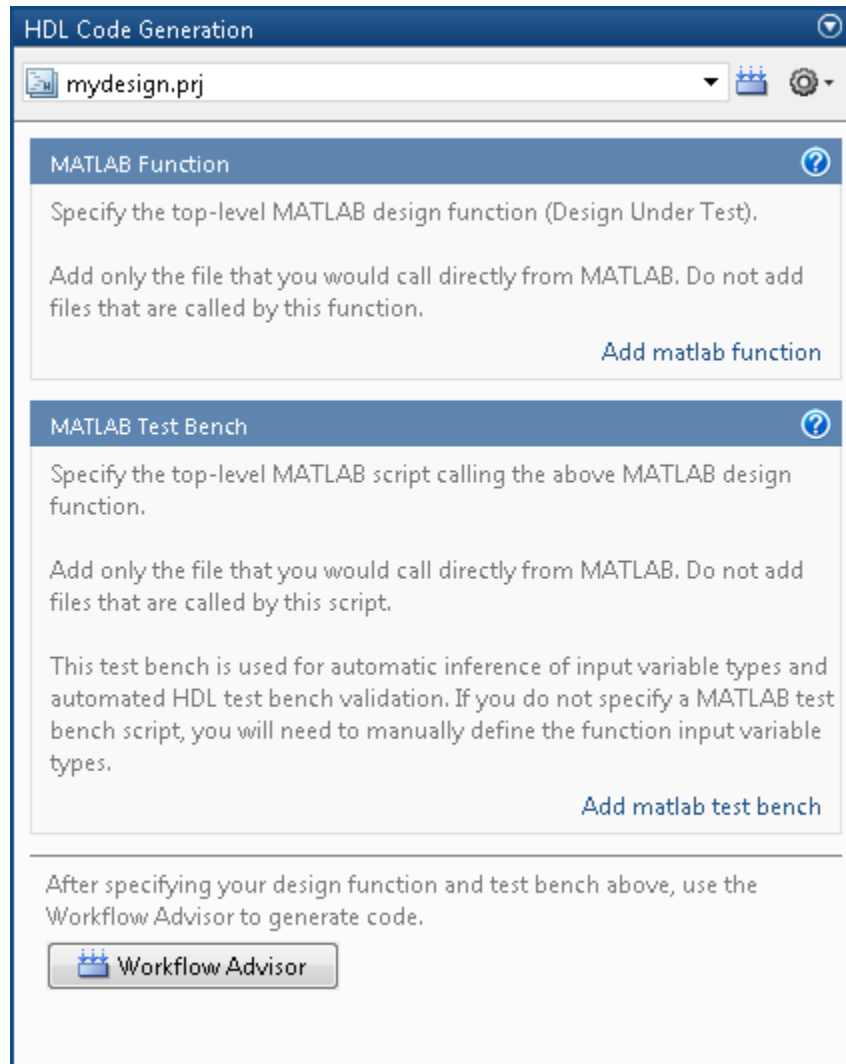
### Create a New Project

**1** At the MATLAB command line, enter:


```
hdlcoder
```

**2** Enter a project name in the project dialog box and click **OK**.

HDL Coder creates the project in the local working folder, and, by default, opens the project in the right side of the MATLAB workspace.



Alternatively, you can create a new HDL Coder project from the Apps gallery:

- 1 On the **Apps** tab, on the far right of the **Apps** section, click the arrow .
- 2 Under **Code Generation**, click **HDL Coder**.

**3** Enter a project name in the project dialog box and click **OK**.

### Open an Existing Project

At the MATLAB command line, enter:

```
open project_name
```

where *project\_name* specifies the full path to the project file.

Alternatively, navigate to the folder that contains your project and double-click the .prj file.

### Add Files to the Project

#### Add the MATLAB Function (Design Under Test)

First, you must add the MATLAB file from which you want to generate code to the project. Add only the top-level function that you call from MATLAB (the Design Under Test). Do not add files that are called by this file. Do not add files that have spaces in their names. The path must not contain spaces, as spaces can lead to code generation failures in certain operating system configurations.

To add a file, do one of the following:

- In the project pane, under **MATLAB Function**, click the **Add MATLAB function** link and browse to the file.
- Drag a file from the current folder and drop it in the project pane under **MATLAB Function**.

If the functions that you added have inputs, and you do not specify a test bench, you must define these inputs. See “Primary Function Input Specification” on page 2-6.

#### Add a MATLAB Test Bench

You must add a MATLAB test bench unless your design does not need fixed-point conversion and you do not want to generate an RTL test bench. If you do not add a test bench, you must define the inputs to your top-level



MATLAB function. For more information, see “Primary Function Input Specification” on page 2-6.

To add a test bench, do one of the following:

- In the project panel, under **MATLAB Test Bench**, click the **Add MATLAB test bench** link and browse to the file.
- Drag a file from the current folder and drop it in the project pane under **MATLAB Test Bench**.

## Primary Function Input Specification

### In this section...

“When to Specify Input Properties” on page 2-6

“Why You Must Specify Input Properties” on page 2-6

“Properties to Specify” on page 2-7

“Rules for Specifying Properties of Primary Inputs” on page 2-12

“Methods for Defining Properties of Primary Inputs” on page 2-12

“Define Input Properties by Example at the Command Line” on page 2-13

“Specify Constant Inputs at the Command Line” on page 2-16

“Specify Variable-Size Inputs at the Command Line” on page 2-18

### When to Specify Input Properties

If you supply a test bench for your MATLAB algorithm, you do not need to manually specify the primary function inputs. The HDL Coder software uses the test bench to infer the data types.

### Why You Must Specify Input Properties

Because C and C++ are statically typed languages, MATLAB Coder™HDL Coder Fixed-Point Toolbox must determine the properties of all variables in the MATLAB files at compile time. To infer variable properties in MATLAB files, MATLAB CoderHDL CoderFixed-Point Toolbox must be able to identify the properties of the inputs to the *primary* function, also known as the *top-level* or *entry-point* function. Therefore, if your primary function has inputs, you must specify the properties of these inputs, to MATLAB CoderHDL CoderFixed-Point Toolbox. If your primary function has no input parameters, MATLAB CoderHDL CoderFixed-Point Toolbox can compile your MATLAB file without modification. You do not need to specify properties of inputs to local functions or external functions called by the primary function.

If you use the tilde (~) character to specify unused function inputs:

- In MATLAB Coder projects, if you want a different type to appear in the generated code, specify the type. Otherwise, the inputs default to real, scalar doubles.
- When generating code with `codegen`, you must specify the type of these inputs using the `-args` option.

If you use the tilde (~) character to specify unused function inputs in an HDL Coder project, and you want a different type to appear in the generated code, specify the type. Otherwise, the inputs default to real, scalar doubles.

## Properties to Specify

If your primary function has inputs, you must specify the following properties for each input.

For...	Specify properties...				
	Class	Size	Complexity	numerictype	fimath
Fixed-point inputs	✓	✓	✓	✓	✓
Each field in a structure input	<p><b>Specify properties for each field according to its class</b></p> <p>When a primary input is a structure, the code generation software treats each field as a separate input. Therefore, you must specify properties for all fields of a primary structure input in the order that they appear in the structure definition:</p> <ul style="list-style-type: none"> <li>• For each field of input structures, specify class, size, and complexity.</li> <li>• For each field that is fixed-point class, also specify <code>numerictype</code>, and <code>fimath</code>.</li> </ul>				
All other inputs	✓	✓	✓		

For...	Specify properties...				
	Class	Size	Complexity	numericity	fimath
Fixed-point inputs	✓	✓	✓	✓	✓
All other inputs	✓	✓	✓		

The following data types are not supported for primary function inputs, although you can use them within the primary function:

- structure
- matrix

Variable-size data is not supported in the test bench or the primary function.

### Default Property Values

MATLAB CoderHDL CoderFixed-Point Toolbox assigns the following default values for properties of primary function inputs.

Property	Default
class	double
size	scalar
complexity	real
numericity	No default
fimath	MATLAB default fimath object

Property	Default
class	double
size	scalar
complexity	real

Property	Default
numericity	No default
fimath	hdlfimath

**Specifying Default Values for Structure Fields.** In most cases, when you don't explicitly specify values for properties, MATLAB CoderHDL CoderFixed-Point Toolbox uses defaults except for structure fields. The only way to name a field in a structure is to set at least one of its properties. Therefore, you might need to specify default values for properties of structure fields. For examples, see [and](#) .

**Specifying Default fimath Values for MEX Functions.** MEX functions generated with MATLAB CoderFixed-Point Toolbox use the default `fimath` value in effect at compile time. If you do not specify a default `fimath` value, MATLAB CoderFixed-Point Toolbox uses the MATLAB default `fimath`. The MATLAB factory default has the following properties:

```
RoundingMethod: Nearest
OverflowAction: Saturate
ProductMode: FullPrecision
SumMode: FullPrecision
CastBeforeSum: true
```

For more information, see “[fimath for Sharing Arithmetic Rules](#)”.

When running MEX functions that depend on the default `fimath` value, do not change this value during your MATLAB session. Otherwise, you receive a run-time warning, alerting you to a mismatch between the compile-time and run-time `fimath` values.

For example, suppose you define the following MATLAB function `test`:

```
function y = test %#codegen
y = fi(0);
```

The function `test` constructs a `fi` object without explicitly specifying a `fimath` object. Therefore, `test` relies on the default `fimath` object in effect at compile time. At the MATLAB prompt, generate the MEX function `text_mex` to use the factory setting of the MATLAB default `fimath`:

```
codegen test
% codegen generates a MEX function, test_mex,
% in the current folder
```

Next, run `test_mex` to display the MATLAB default `fimath` value:

```
test_mex

ans =

      0

      DataTypeMode: Fixed-point: binary point scaling
      Signedness: Signed
      WordLength: 16
      FractionLength: 15
```

Now create a local MATLAB `fimath` value. so you no longer use the default setting:

```
F = fimath('RoundingMethod','Floor');
```

Finally, clear the MEX function from memory and rerun it:

```
clear test_mex
test_mex
```

The mismatch is detected and causes an error:

```
??? This function was generated with a different default
fimath than the current default.
```

```
Error in ==> test_mex
```

### Supported Classes

The following table presents the class names supported by MATLAB CoderHDL CoderFixed-Point Toolbox.

<b>Class Name</b>	<b>Description</b>
logical	Logical array of true and false values
char	Character array
int8	8-bit signed integer array
uint8	8-bit unsigned integer array
int16	16-bit signed integer array
uint16	16-bit unsigned integer array
int32	32-bit signed integer array
uint32	32-bit unsigned integer array
single	Single-precision floating-point or fixed-point number array
double	Double-precision floating-point or fixed-point number array
struct	Structure array
embedded.fi	Fixed-point number array

<b>Class Name</b>	<b>Description</b>
logical	Logical array of true and false values
char	Character array
int8	8-bit signed integer array
uint8	8-bit unsigned integer array
int16	16-bit signed integer array
uint16	16-bit unsigned integer array
int32	32-bit signed integer array
uint32	32-bit unsigned integer array
single	Single-precision floating-point or fixed-point number array

<b>Class Name</b>	<b>Description</b>
double	Double-precision floating-point or fixed-point number array
embedded.fi	Fixed-point number array

## Rules for Specifying Properties of Primary Inputs

When specifying the properties of primary inputs, follow these rules.

- You must specify the class of all primary inputs. If you do not specify the size or complexity of primary inputs, they default to real scalars.
- For each primary function input whose class is fixed point (fi), you must specify the input `numericType` and `fiMath` properties.
- For each primary function input whose class is `struct`, you must specify the properties of each of its fields in the order that they appear in the structure definition.

## Methods for Defining Properties of Primary Inputs

<b>Method</b>	<b>Advantages</b>	<b>Disadvantages</b>
	<ul style="list-style-type: none"> <li>• If you are working in a MATLAB CoderHDL Coder project, easy to use</li> <li>• Does not alter original MATLAB code</li> <li>• MATLAB CoderHDL Coder saves the definitions in the project file</li> </ul>	<ul style="list-style-type: none"> <li>• Not efficient for specifying memory-intensive inputs such as large structures and arrays</li> </ul>
“Define Input Properties by Example at the Command Line” on page 2-13	<ul style="list-style-type: none"> <li>• Easy to use</li> <li>• Does not alter original MATLAB code</li> </ul>	<ul style="list-style-type: none"> <li>• Must be specified at the command line every time you invoke <code>codegen</code> (unless you use a script)</li> </ul>



Method	Advantages	Disadvantages
<p><b>Note</b> If you define input properties programmatically in the MATLAB file, you cannot use this method</p>	<ul style="list-style-type: none"> <li>• Designed for prototyping a function that has a small number of primary inputs</li> </ul>	<ul style="list-style-type: none"> <li>• Not efficient for specifying memory-intensive inputs such as large structures and arrays</li> </ul>
	<ul style="list-style-type: none"> <li>• Integrated with MATLAB code; no need to redefine properties each time you invoke MATLAB CoderHDL Coder</li> <li>• Provides documentation of property specifications in the MATLAB code</li> <li>• Efficient for specifying memory-intensive inputs such as large structures</li> </ul>	<ul style="list-style-type: none"> <li>• Uses complex syntax</li> <li>• MATLAB CoderHDL Coder project files do not currently recognize properties defined programmatically. If you are using a project, you must reenter the input types in the project.</li> </ul>

## Define Input Properties by Example at the Command Line

- “Command Line Option -args” on page 2-14
- “Rules for Using the -args Option” on page 2-14
- “Specifying Properties of Primary Inputs by Example at the Command Line” on page 2-14
- “Specifying Properties of Primary Fixed-Point Inputs by Example at the Command Line” on page 2-15

## Command Line Option `-args`

The `codegen` function provides a command-line option `-args` for specifying the properties of primary (entry-point) function inputs as a cell array of example values. The cell array can be a variable or literal array of constant values. Using this option, you specify the properties of inputs at the same time as you generate code for the MATLAB function with `codegen`. If you have a test function or script that calls the entry-point MATLAB function with the required types, you can use `coder.getArgTypes` to determine the types of the function inputs. `coder.getArgTypes` returns a cell array of `coder.Type` objects that you can pass to `codegen` using the `-args` option. For more information, see the `coder.getArgTypes` function reference information.

See for `codegen`.

## Rules for Using the `-args` Option

When using the `-args` command-line option to define properties by example, follow these rules:

- The cell array of sample values must contain the same number of elements as primary function inputs.
- The order of elements in the cell array must correspond to the order in which inputs appear in the primary function signature — for example, the first element in the cell array defines the properties of the first primary function input.

---

**Note** If you specify an empty cell array with the `-args` option, `codegen` interprets this to mean that the function takes no inputs; a compile-time error occurs if the function does have inputs.

---

## Specifying Properties of Primary Inputs by Example at the Command Line

Consider a MATLAB function that adds its two inputs:

```
function y = mcf(u,v)
%#codegen
y = u + v;
```

The following examples show how to specify different properties of the primary inputs *u* and *v* by example at the command line:

- Use a literal cell array of constants to specify that both inputs are real scalar doubles:

```
codegen mcf -args {0,0}
```

- Use a literal cell array of constants to specify that input *u* is an unsigned 16-bit, 1-by-4 vector and input *v* is a scalar double:

```
codegen mcf -args {zeros(1,4,'uint16'),0}
```

- Assign sample values to a cell array variable to specify that both inputs are real, unsigned 8-bit integer vectors:

```
a = uint8([1;2;3;4])
b = uint8([5;6;7;8])
ex = {a,b}
codegen mcf -args ex
```

### Specifying Properties of Primary Fixed-Point Inputs by Example at the Command Line

To generate a MEX function or C/C++ code for fixed-point MATLAB code, you must install Fixed-Point Toolbox software.

Consider a MATLAB function that calculates the square root of a fixed-point number:

```
##codegen
function y = sqrtfi(x)
y = sqrt(x);
```

To specify the properties of the primary fixed-point input *x* by example on the MATLAB command line, follow these steps:

- 1 Define the `numericType` properties for *x*, as in this example:

```
T = numericType('WordLength',32,...
               'FractionLength',23,...
               'Signed',true);
```

- 2** Define the `fimath` properties for `x`, as in this example:

```
F = fimath('SumMode','SpecifyPrecision',...
          'SumWordLength',32,...
          'SumFractionLength',23,...
          'ProductMode','SpecifyPrecision',...
          'ProductWordLength',32,...
          'ProductFractionLength',23);
```

- 3** Create a fixed-point variable with the `numericType` and `fimath` properties you just defined, as in this example:

```
myeg = { fi(4.0,T,F) };
```

- 4** Compile the function `sqrtfi` using the `codegen` command, passing the variable `myeg` as the argument to the `-args` option, as in this example:

```
codegen sqrtfi -args myeg;
```

## Specify Constant Inputs at the Command Line

In cases where you know your primary inputs will not change at run time, it is more efficient to specify them as constant values than as variables to eliminate unnecessary overhead in generated code. Common uses of constant inputs are for flags that control how an algorithm executes and values that specify the sizes or types of data.

You can define inputs to be constants using the `-args` command-line option with a `coder.Constant` object, as in this example:

```
-args {coder.Constant(constant_input)}
```

This expression specifies that an input will be a constant with the size, class, complexity, and value of *constant\_input*.

## Calling Functions with Constant Inputs

`codegen` compiles constant function inputs into the generated code. As a result, the MEX function signature differs from the MATLAB function signature. At run time you supply the constant argument to the MATLAB function, but not to the MEX function.

For example, consider the following function `identity` which copies its input to its output:

```
function y = identity(u) %#codegen
y = u;
```

To generate a MEX function `identity_mex` with a constant input, at the MATLAB prompt, type the following command:

```
codegen identity -args {coder.Constant(42)}
```

To run the MATLAB function, supply the constant argument:

```
identity(42)
```

You get the following result:

```
ans =
    42
```

Now, try running the MEX function with this command:

```
identity_mex
```

You should get the same answer.

## Specifying a Structure as a Constant Input

Suppose you define a structure `tmp` in the MATLAB workspace to specify the dimensions of a matrix:

```
tmp = struct('rows', 2, 'cols', 3);
```

The following MATLAB function `rowcol` accepts a structure input `p` to define matrix `y`:

```
function y = rowcol(u,p) %#codegen
y = zeros(p.rows,p.cols) + u;
```

The following example shows how to specify that primary input `u` is a double scalar variable and primary input `p` is a constant structure:

```
codegen rowcol -args {0,coder.Constant(tmp)}
```

## Specify Variable-Size Inputs at the Command Line

Variable-size data is data whose size might change at run time. MATLAB supports bounded and unbounded variable-size data for code generation. *Bounded variable-size data* has fixed upper bounds. This data can be allocated statically on the stack or dynamically on the heap. *Unbounded variable-size data* does not have fixed upper bounds. This data must be allocated on the heap. You can define inputs to have one or more variable-size dimensions — and specify their upper bounds — using the `-args` option and `coder.typeof` function:

```
-args {coder.typeof(example_value, size_vector, variable_dims)}
```

Specifies a variable-size input with:

- Same class and complexity as *example\_value*
- Same size and upper bounds as *size\_vector*
- Variable dimensions specified by *variable\_dims*

When you enable dynamic memory allocation, you can specify `Inf` in the size vector for dimensions with unknown upper bounds at compile time.

When *variable\_dims* is a scalar, it is applied to all the dimensions, with the following exceptions:

- If the dimension is 1 or 0, which are fixed.
- If the dimension is unbounded, which is always variable size.

For more information, see `coder.typeof` and `.`

## Specifying a Variable-Size Vector Input

- 1 Write a function that computes the average of every `n` elements of a vector `A` and stores them in a vector `B`:

```
function B = nway(A,n) %#codegen
% Compute average of every N elements of A and put them in B.
```

```
coder.extrinsic('error');
if ((mod(numel(A),n) == 0) && (n>=1 && n<=numel(A)))
    B = ones(1,numel(A)/n);
    k = 1;
    for i = 1 : numel(A)/n
        B(i) = mean(A(k + (0:n-1)));
        k = k + n;
    end
else
    B = zeros(1,0);
    error('n <= 0 or does not divide number of elements evenly');
end
```

- 2** Specify the first input A as a vector of double values. Its first dimension stays fixed in size and its second dimension can grow to an upper bound of 100. Specify the second input n as a double scalar.

```
codegen -report nway -args {coder.typeof(0,[1 100],1),1}
```

- 3** As an alternative, assign the `coder.typeof` expression to a MATLAB variable, then pass the variable as an argument to `-args`:

```
vareg = coder.typeof(0,[1 100],1)
codegen -report nway -args {vareg, 0}
```





# Code Generation

---

- “Basic HDL Code Generation with the Workflow Advisor” on page 3-2
- “HDL Code Generation from System Objects” on page 3-12
- “Model State with Persistent Variables and System Objects” on page 3-17
- “Floating-Point to Fixed-Point Conversion” on page 3-21
- “Fixed-Point Type Conversion and Refinement” on page 3-36
- “Working with Generated Fixed-Point Files” on page 3-46
- “MATLAB Function Block Generation” on page 3-54
- “System Design with HDL Code Generation from MATLAB and Simulink” on page 3-56
- “Xilinx System Generator Black Box Block Generation” on page 3-61
- “Generate Xilinx System Generator for DSP Black Box from MATLAB HDL Design” on page 3-63
- “Generate Code Using the Command Line Interface” on page 3-70
- “Clock Enable Rate Specification” on page 3-71
- “Test Bench Clock Enable Toggle Rate Specification” on page 3-73

## Basic HDL Code Generation with the Workflow Advisor

This example shows how to work with MATLAB HDL Coder™ projects to generate HDL from MATLAB designs.

### Introduction

This example helps you familiarize yourself with the following aspects of HDL code generation:

- 1 Generating HDL code from MATLAB design.
- 2 Generating a HDL test bench from a MATLAB test bench.
- 3 Verifying the generated HDL code using a HDL simulator.
- 4 Synthesizing the generated HDL code using a HDL synthesis tool.

### MATLAB Design

The MATLAB code used in this example implements a simple symmetric FIR filter. This example also shows a MATLAB test bench that exercises the filter.

```
design_name = 'mlhdlc_sfir.m';  
testbench_name = 'mlhdlc_sfir_tb.m';
```

- 1 MATLAB Design: mlhdlc\_sfir
- 2 MATLAB testbench: mlhdlc\_sfir\_tb

### Create a New Folder and Copy Relevant Files

Execute the following lines of code to copy the necessary example files into a temporary folder.

```
mlhdlc_demo_dir = fullfile(matlabroot, 'toolbox', 'hdlcoder', 'hdlcoderdemo');  
mlhdlc_temp_dir = [tempdir 'mlhdlc_sfir'];  
  
% Create a temporary folder and copy the MATLAB files.  
cd(tempdir);  
[~, ~, ~] = rmdir(mlhdlc_temp_dir, 's');
```

```
mkdir(mlhdlc_temp_dir);  
cd(mlhdlc_temp_dir);  
  
copyfile(fullfile(mlhdlc_demo_dir, design_name), mlhdlc_temp_dir);  
copyfile(fullfile(mlhdlc_demo_dir, testbench_name), mlhdlc_temp_dir);
```

### **Simulate the Design**

Simulate the design with the test bench prior to code generation to make sure there are no runtime errors.

```
mlhdlc_sfir_tb
```

### **Create a New HDL Coder Project**

To create a new project, enter the following command:

```
coder -hdlcoder -new mlhdlc_sfir
```

Next, add the file 'mlhdlc\_sfir.m' to the project as the MATLAB Function and 'mlhdlc\_sfir\_tb.m' as the MATLAB Test Bench.

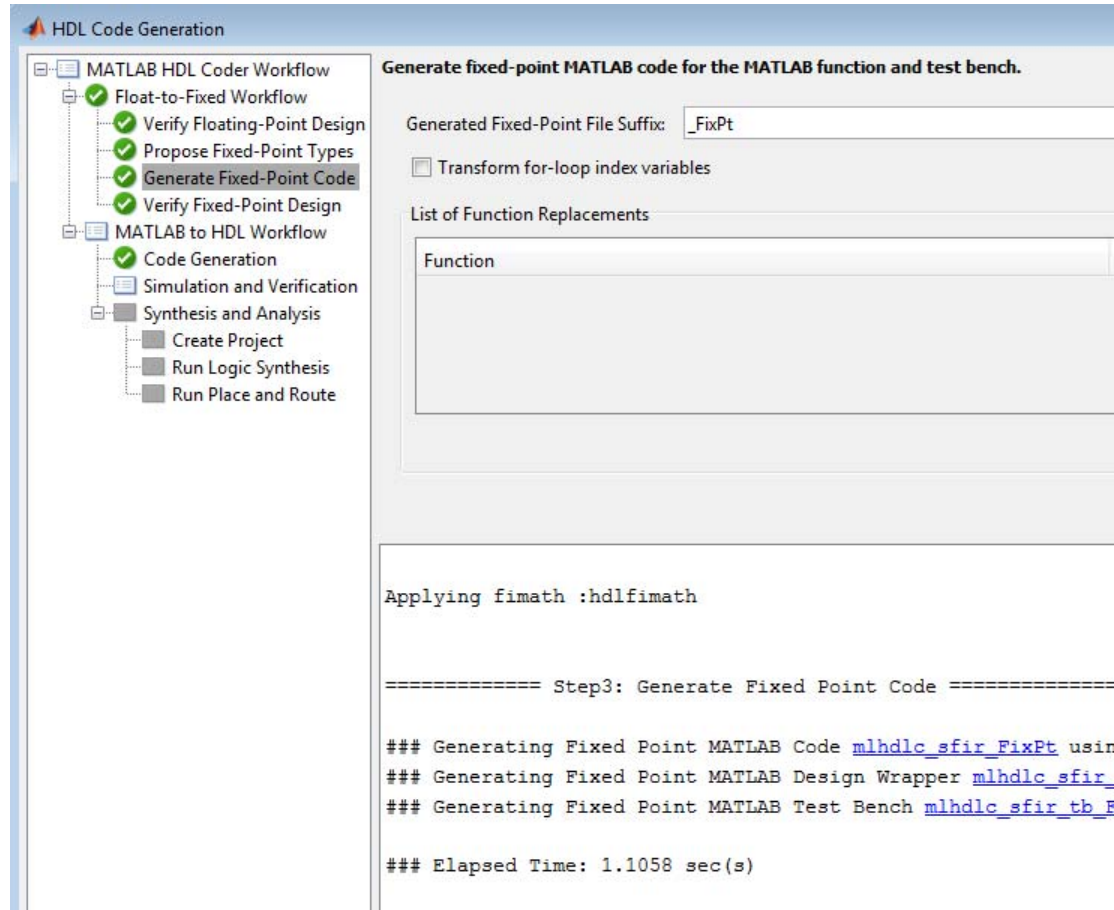
You can refer to Getting Started with MATLAB to HDL Workflow tutorial for a more complete introduction to creating and populating HDL Coder projects.

### **Step 1: Generate Fixed-Point MATLAB Code**

Right-click the 'Float-to-Fixed Workflow' step and choose the option 'Run this task' to run all the steps to generate fixed-point MATLAB code.

Examine the generated fixed-point MATLAB code by clicking the links in the log window to open the MATLAB code in the editor.

For more details on fixed-point conversion, refer to the Floating-Point to Fixed-Point Conversion tutorial.



#### Step 2: Generate HDL Code

This step generates Verilog code from the generated fixed-point MATLAB design, and a Verilog test bench from the MATLAB test bench wrapper.

To set code generation options and generate HDL code:

- 1 Click the 'Code Generation' step to view the HDL code generation options panel.

- 2** In the Target tab, choose 'Verilog' as the 'Language' option.
- 3** Select the 'Generate HDL' and 'Generate HDL test bench' options.
- 4** In the Test bench tab, choose the 'Multi-file test bench' option to generate test bench code and test bench data (stimulus and response) in separate files.
- 5** In the 'Optimizations' tab, choose '1' as the Input and Output pipeline length, and enable the 'Distribute pipeline registers' option.
- 6** In the 'Coding style' tab, choose 'Include MATLAB source code as comments' and 'Generate report' to generate a code generation report with comments and traceability links.
- 7** Click the 'Run' button to generate both the Verilog design and testbench with reports.

**Code Generation Options**

Target Selection  
Language: Verilog

Output Settings

- Check HDL conformance
- Generate HDL
- Generate HDL test bench
- Generate EDA scripts

Test Bench Options

- Multi file test bench

Optimization Options

- Distribute pipeline registers

Input pipelining: 1

Output pipelining: 1

Coding Style Options

Generated Code Comments

- Preserve MATLAB code comments
- Include MATLAB source code as comments
- Generate Report

Examine the log window and click the links to explore the generated code and the reports.

```

### Begin Verilog Code Generation
### Working on mlhdlc_sfir_FixPt as mlhdlc\_sfir\_FixPt.v
### The DUT requires an initial pipeline setup latency. Each output port experiences these
### Output port 0: 2 cycles
### Output port 1: 2 cycles
### Output port 2: 2 cycles
### Generating Resource Utilization Report resource\_report.html Resource Report

### Begin Test Bench Generation
### Collect Test Bench Stimulus and Response
### Begin Simulation to log data

### Simulation to log data completed in 2.4955 sec(s)
### ### Accounting for Output port Latency: 2 cycles
### Collecting data...
### Begin HDL test bench file generation with logged samples
### Generating test bench package: mlhdlc\_sfir\_FixPt\_tb\_pkg.v
### Generating test bench data file: mlhdlc\_sfir\_FixPt\_tb\_data.v
### Generating test bench: mlhdlc\_sfir\_FixPt\_tb.v

Code generation successful: View report MATLAB Report with
### Elapsed Time: 55.3389 sec(s) Traceability Links

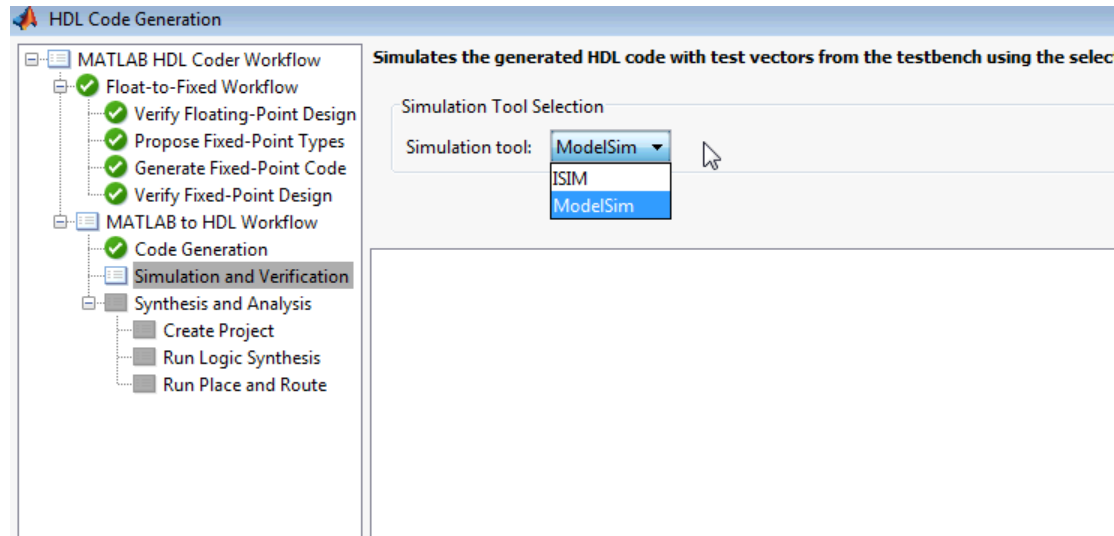
```

Verilog Code

Verilog Testbench

### Step 3: Simulate the Generated Code

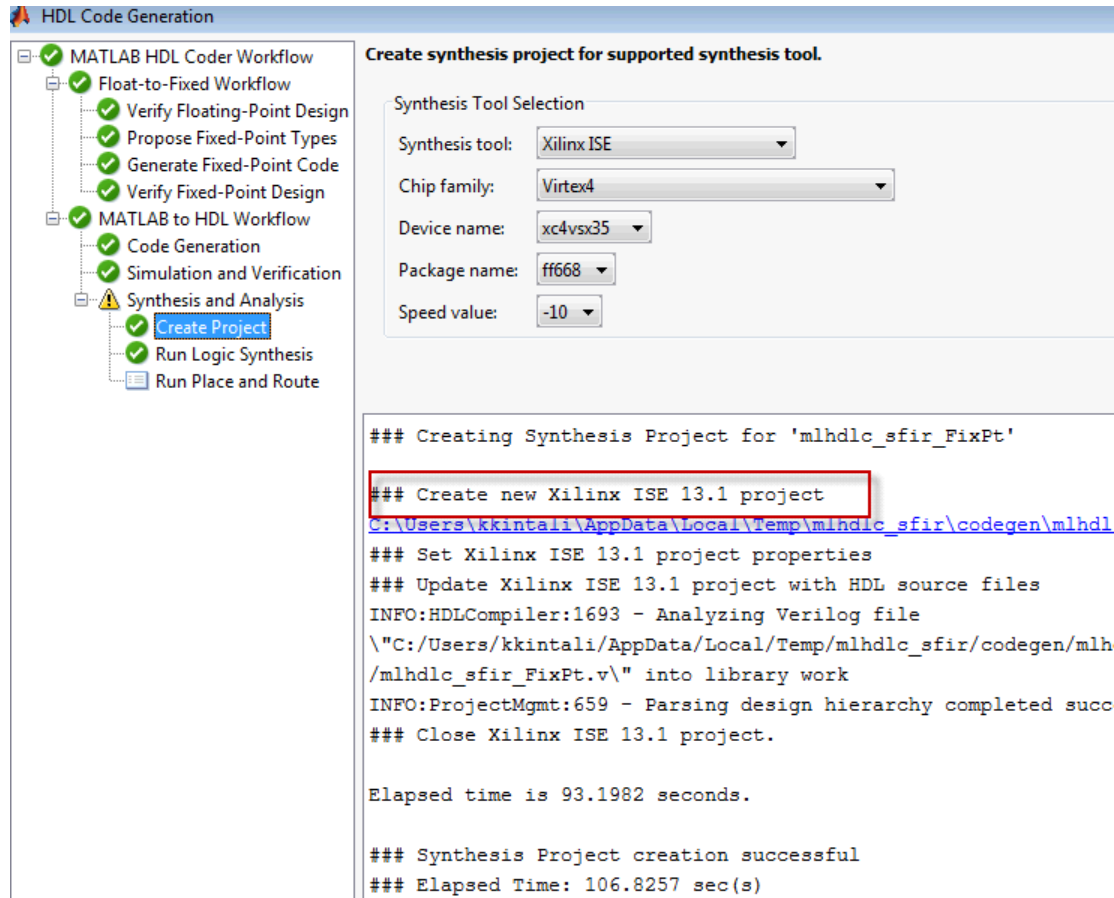
HDL Coder automates the process of running the generated HDL test bench using the ModelSim or ISIM™ simulator, and reports if the generated HDL simulation matches the numerics and latency with respect to the fixed-point MATLAB simulation.



#### Step 4: Synthesize the Generated Code

HDL Coder also creates a Xilinx ISE™ or Altera Quartus™ project with the selected options and runs the selected logic synthesis and place-and-route steps for the generated HDL code.





**HDL Code Generation**

**CREATE synthesis project for supported synthesis tool.**

Synthesis Tool Selection

Synthesis tool: Xilinx ISE

Chip family: Virtex4

Device name: xc4vsx35

Package name: ff668

Speed value: -10

Workflow Steps:

- MATLAB HDL Coder Workflow
  - Float-to-Fixed Workflow
    - Verify Floating-Point Design
    - Propose Fixed-Point Types
    - Generate Fixed-Point Code
    - Verify Fixed-Point Design
  - MATLAB to HDL Workflow
    - Code Generation
    - Simulation and Verification
    - Synthesis and Analysis
      - Create Project**
      - Run Logic Synthesis
      - Run Place and Route

```
### Creating Synthesis Project for 'mlhdlc_sfir_FixPt'  
### Create new Xilinx ISE 13.1 project  
C:\Users\kkintali\AppData\Local\Temp\mlhdlc_sfir\codegen\mlhdlc_sfir_FixPt  
### Set Xilinx ISE 13.1 project properties  
### Update Xilinx ISE 13.1 project with HDL source files  
INFO:HDLCompiler:1693 - Analyzing Verilog file  
\"C:/Users/kkintali/AppData/Local/Temp/mlhdlc_sfir/codegen/mlhdlc_sfir_FixPt.v\" into library work  
INFO:ProjectMgmt:659 - Parsing design hierarchy completed successfully  
### Close Xilinx ISE 13.1 project.  
  
Elapsed time is 93.1982 seconds.  
  
### Synthesis Project creation successful  
### Elapsed Time: 106.8257 sec(s)
```

Examine the log window to view the results of synthesis steps.

**HDL Code Generation**

Launch selected synthesis tool and synthesize the generated HDL code.

Asynchronous Control Signals Information:

```
-----
Control Signal | Buffer(FP name) | Load |
-----+-----+-----
reset | IBUF | 321 |
-----+-----+-----
```

Timing Summary:

```
-----
Speed Grade: -10

Minimum period: 5.527ns (Maximum Frequency: 180.933MHz)
Minimum input arrival time before clock: 6.132ns
Maximum output required time after clock: 6.717ns
Maximum combinational path delay: 7.093ns
-----
```

```
=====  

Process "Synthesize - XST" completed successfully  

### Synthesis Complete.  

### Close Xilinx ISE 13.1 project.  

Elapsed time is 101.9205 seconds.  

### Generating Synthesis report mlhdlc\_sfir\_FixPt\_syn\_results.  

### Synthesis successful  

### Elapsed Time: 101.9728 sec(s)
```

#### Clean up the Generated Files

Run the following commands to clean up the temporary project folder.

```
mlhdlc_demo_dir = fullfile(matlabroot, 'toolbox', 'hdlcoder', 'hdlcoderdemo
```

```
mlhdlc_temp_dir = [tempdir 'mlhdlc_sfir'];  
clear mex;  
cd (mlhdlc_demo_dir);  
rmdir(mlhdlc_temp_dir, 's');
```

## HDL Code Generation from System Objects

This example shows how to generate HDL code from MATLAB code that contains System objects.

### MATLAB Design

The MATLAB code used in this example implements a simple symmetric FIR filter and uses the `dsp.Delay` System object to model state. This example also shows a MATLAB test bench that exercises the filter.

```
design_name = 'mlhdlc_sysobj_ex.m';
testbench_name = 'mlhdlc_sysobj_ex_tb.m';
```

Let us take a look at the MATLAB design.

```
type(design_name);
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% MATLAB design: Symmetric FIR Filter
%
% Design pattern covered in this example:
% Filter states modeled using DSP System object (dsp.Delay)
% Filter coefficients passed in as parameters to the design
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%#codegen
function [y_out, delayed_xout] = mlhdlc_sysobj_ex(x_in, h_in1, h_in2, h_in3)
% Symmetric FIR Filter

persistent h1 h2 h3 h4 h5 h6 h7 h8;
if isempty(h1)
    h1 = dsp.Delay('FrameBasedProcessing', false);
    h2 = dsp.Delay('FrameBasedProcessing', false);
    h3 = dsp.Delay('FrameBasedProcessing', false);
    h4 = dsp.Delay('FrameBasedProcessing', false);
    h5 = dsp.Delay('FrameBasedProcessing', false);
    h6 = dsp.Delay('FrameBasedProcessing', false);
    h7 = dsp.Delay('FrameBasedProcessing', false);
```

```
        h8 = dsp.Delay('FrameBasedProcessing', false);
    end

    h1p = step(h1, x_in);
    h2p = step(h2, h1p);
    h3p = step(h3, h2p);
    h4p = step(h4, h3p);
    h5p = step(h5, h4p);
    h6p = step(h6, h5p);
    h7p = step(h7, h6p);
    h8p = step(h8, h7p);

    a1 = h1p + h8p;
    a2 = h2p + h7p;
    a3 = h3p + h6p;
    a4 = h4p + h5p;

    m1 = h_in1 * a1;
    m2 = h_in2 * a2;
    m3 = h_in3 * a3;
    m4 = h_in4 * a4;

    a5 = m1 + m2;
    a6 = m3 + m4;

    % filtered output
    y_out = a5 + a6;
    % delayout input signal
    delayed_xout = h8p;

end

type(testbench_name);
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% MATLAB test bench for the FIR filter
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
clear mlhdlc_sysobj_ex;

x_in = cos(2.*pi.*(0:0.001:2).*(1+(0:0.001:2).*75)).';

h1 = -0.1339;
h2 = -0.0838;
h3 = 0.2026;
h4 = 0.4064;

len = length(x_in);
y_out_sysobj = zeros(1,len);
x_out_sysobj = zeros(1,len);
a = 10;

for ii=1:len
    data = x_in(ii);
    % call to the design 'sfir' that is targeted for hardware
    [y_out_sysobj(ii), x_out_sysobj(ii)] = mlhdlc_sysobj_ex(data, h1, h2, h3, h4, a);
end

figure('Name', [mfilename, '_plot']);
subplot(2,1,1);
plot(1:len,x_in); title('Input signal with noise');
subplot(2,1,2);
plot(1:len,y_out_sysobj); title('Filtered output signal');
```

### **Create a New Folder and Copy Relevant Files**

Execute the following lines of code to copy the necessary example files into a temporary folder.

```
mlhdlc_demo_dir = fullfile(matlabroot, 'toolbox', 'hdlcoder', 'hdlcoderdemo');
mlhdlc_temp_dir = [tempdir 'mlhdlc_sysobj_intro'];

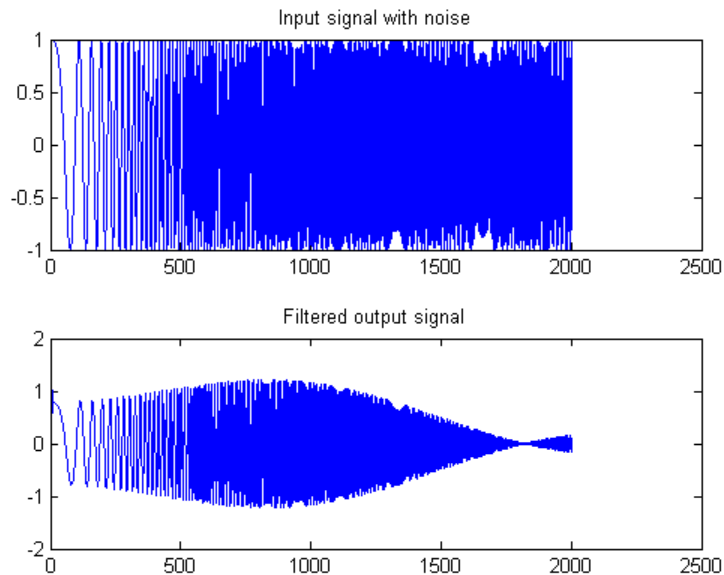
% Create a temporary folder and copy the MATLAB files.
cd(tempdir);
[~, ~, ~] = rmdir(mlhdlc_temp_dir, 's');
```

```
mkdir(mlhdlc_temp_dir);  
cd(mlhdlc_temp_dir);  
  
copyfile(fullfile(mlhdlc_demo_dir, design_name), mlhdlc_temp_dir);  
copyfile(fullfile(mlhdlc_demo_dir, testbench_name), mlhdlc_temp_dir);
```

### Simulate the Design

Simulate the design with the test bench prior to code generation to make sure there are no runtime errors.

```
mlhdlc_sysobj_ex_tb
```



### Create a New HDL Coder™ Project

To create a new project, enter the following command:

```
coder -hdlcoder -new mlhdlc_sysobj_prj
```

Next, add the file 'mlhdlc\_sysobj\_ex.m' to the project as the MATLAB Function and 'mlhdlc\_sysobj\_ex\_tb.m' as the MATLAB Test Bench.

You can refer to the Getting Started with MATLAB to HDL Workflow tutorial for a more complete tutorial on creating and populating MATLAB HDL Coder projects.

### **Run Fixed-Point Conversion and HDL Code Generation**

Launch the Workflow Advisor. In the Workflow Advisor, right-click the 'Code Generation' step. Choose the option 'Run to selected task' to run all the steps from the beginning through HDL code generation.

Examine the generated HDL code by clicking the links in the log window.

### **Supported System objects**

Refer to the documentation for a list of System objects supported for HDL code generation.

### **Clean up the Generated Files**

Run the following commands to clean up the temporary project folder.

```
mlhdlc_demo_dir = fullfile(matlabroot, 'toolbox', 'hdlcoder', 'hdlcoderdemo');
mlhdlc_temp_dir = [tempdir 'mlhdlc_sysobj_intro'];
clear mex;
cd (mlhdlc_demo_dir);
rmdir(mlhdlc_temp_dir, 's');
```



# Model State with Persistent Variables and System Objects

This example shows how to use persistent variables and System objects to model state and delays in a MATLAB design for HDL code generation.

## Introduction

Using System objects to model delay results in concise generated code.

In MATLAB, multiple calls to a function having persistent variables do not result in multiple delays. Instead, the state in the function gets updated multiple times.

```
% In order to reuse code implemented in a function with states,  
% you need to duplicate functions multiple times to create multiple  
% instances of the algorithm with delay.
```

## Examine the MATLAB Code

Let us take a quick look at the implementation of the Sobel algorithm.

Examine the design to see how the delays and line buffers are modeled using:

- Persistent variables: `mlhdlc_sobel`
- System objects: `mlhdlc_sysobj_sobel`

Notice that the `'filterdelay'` function is duplicated with different function names in `'mlhdlc_sobel'` code to instantiate multiple versions of the algorithm in MATLAB for HDL code generation.

The delay line implementation is more complicated when done using MATLAB persistent variables.

Now examine the simplified implementation of the same algorithm using System objects in `'mlhdlc_sysobj_sobel'`.

When used within the constraints of HDL code generation, the `dsp.Delay` objects always map to registers. For persistent variables to be inferred as registers, you have to be careful to read the variable before writing to it to map it to a register.

**MATLAB Design**

```
demo_files = {...  
    'mlhdlc_sysobj_sobel.m', ...  
    'mlhdlc_sysobj_sobel_tb.m', ...  
    'mlhdlc_sobel.m', ...  
    'mlhdlc_sobel_tb.m'  
};
```

**Create a New Folder and Copy Relevant Files**

Execute the following lines of code to copy the necessary example files into a temporary folder.

```
mlhdlc_demo_dir = fullfile(matlabroot, 'toolbox', 'hdlcoder', 'hdlcoderdemo');  
mlhdlc_temp_dir = [tempdir 'mlhdlc_delay_modeling'];  
  
% create a temporary folder and copy the MATLAB files  
cd(tempdir);  
[~, ~, ~] = rmdir(mlhdlc_temp_dir, 's');  
mkdir(mlhdlc_temp_dir);  
cd(mlhdlc_temp_dir);  
  
for ii=1:numel(demo_files)  
    copyfile(fullfile(mlhdlc_demo_dir, demo_files{ii}), mlhdlc_temp_dir);  
end
```

**Known Limitations**

HDL Coder™ only supports the 'step' method of the System object and does not support 'output' and 'update' methods.

With support for only the step method, delays cannot be used in modeling feedback paths. For example, the following piece of MATLAB code cannot be supported using the dsp.Delay System object.

```
##codegen  
function y = accumulate(u)  
persistent p;  
if isempty(p)  
    p = 0;
```

```
end
y = p;
p = p + u;
```

### **Create a New HDL Coder Project**

To create a new project, enter the following command:

```
coder -hdlcoder -new mlhdlc_sobel
```

Next, add the file 'mlhdlc\_sobel.m' to the project as the MATLAB Function and 'mlhdlc\_sobel\_tb.m' as the MATLAB Test Bench.

You can refer to the Getting Started with MATLAB to HDL Workflow tutorial for a more complete tutorial on creating and populating MATLAB HDL Coder projects.

### **Run Fixed-Point Conversion and HDL Code Generation**

Launch the Workflow Advisor and right-click the 'Code Generation' step. Choose the option 'Run to selected task' to run all the steps from the beginning through HDL code generation.

Examine the generated HDL code by clicking the hyperlinks in the Code Generation Log window.

Now, create a new project for the system object design:

```
coder -hdlcoder -new mlhdlc_sysobj_sobel
```

Add the file 'mlhdlc\_sysobj\_sobel.m' to the project as the MATLAB Function and 'mlhdlc\_sysobj\_sobel\_tb.m' as the MATLAB Test Bench.

Repeat the code generation steps and examine the generated fixed-point MATLAB and HDL code.

### **Additional Notes:**

You can model integer delay using dsp.Delay object by setting the 'Length' property to be greater than 1. These delay objects will be mapped to shift registers in the generated code.

If the optimization option 'Map persistent array variables to RAMs' is enabled, delay System objects will get mapped to block RAMs under the following conditions:

- 'InitialConditions' property of the dsp.Delay is set to zero.
- Delay input data type is not floating-point.
- RAMSize (DelayLength \* InputWordLength) is greater than or equal to the 'RAM Mapping Threshold'.

### **Clean up the Generated Files**

Run the following commands to clean up the temporary project folder.

```
mlhdlc_demo_dir = fullfile(matlabroot, 'toolbox', 'hdlcoder', 'hdlcoderdemo');
mlhdlc_temp_dir = [tempdir 'mlhdlc_delay_modeling'];
clear mex;
cd (mlhdlc_demo_dir);
rmdir(mlhdlc_temp_dir, 's');
```

## Floating-Point to Fixed-Point Conversion

This example shows how to start with a floating-point design in MATLAB, iteratively converge on an efficient fixed-point design in MATLAB, and verify the numerical accuracy of the generated fixed-point design.

Signal processing applications for reconfigurable platforms require algorithms that are typically specified using floating-point operations. However, for power, cost, and performance reasons, they are usually implemented with fixed-point operations either in software for DSP cores or as special-purpose hardware in FPGAs. Fixed-point conversion can be very challenging and time-consuming, typically demanding 25 to 50 percent of the total design and implementation time. Automated tools can simplify and accelerate the conversion process.

For software implementations, the aim is to define an optimized fixed-point specification which minimizes the code size and the execution time for a given computation accuracy constraint. This optimization is achieved through the modification of the binary point location (for scaling) and the selection of the data word length according to the different data types supported by the target processor.

For hardware implementations, the complete architecture can be optimized. An efficient implementation will minimize both the area used and the power consumption. Thus, the conversion process goal typically is focused around minimizing the operator word length.

The floating-point to fixed-point workflow is currently integrated in the HDL Workflow Advisor that you have been introduced to in the tutorial Getting Started with MATLAB to HDL Workflow.

### Introduction

The floating-point to fixed-point conversion workflow in HDL Coder™ includes the following steps:

- 1 Verify that the floating-point design is compatible with code generation.
- 2 Compute fixed-point types based on the simulation of the testbench.

- 3** Generate readable and traceable fixed-point MATLAB code.
- 4** Verify the generated fixed-point design.
- 5** Compare the numerical accuracy of the generated code with the original floating point code.

**MATLAB Design**

The MATLAB code used in this example is a simple second-order direct-form 2 transposed filter. This example also contains a MATLAB testbench that exercises the filter.

```
design_name = 'mlhdlc_df2t_filter.m';  
testbench_name = 'mlhdlc_df2t_filter_tb.m';
```

Examine the MATLAB design.

```
type(design_name);  
  
%#codegen  
function y = mlhdlc_df2t_filter(x)  
  
persistent z;  
if isempty(z)  
    % Filter states as a column vector  
    z = zeros(2,1);  
end  
  
% Filter coefficients as constants  
b = [0.29290771484375    0.585784912109375    0.292907714843750];  
a = [1.0                0.0                0.171600341796875];  
  
y    = b(1)*x + z(1);  
z(1) = (b(2)*x + z(2)) - a(2) * y;  
z(2) = b(3)*x - a(3) * y;  
  
end
```

For the floating-point to fixed-point workflow, it is desirable to have a complete testbench. The quality of the proposed fixed-point data types depends on how well the testbench covers the dynamic range of the design with the desired accuracy.

For more details on the requirements for the floating-point design and the testbench, refer to the 'Floating-Point Design Structure' structure section of the Working with Generated Fixed-Point Files tutorial.

```
type(testbench_name);
```

```
Fs = 256;           % Sampling frequency
Ts = 1/Fs;         % Sample time
t = 0:Ts:1-Ts;    % Time vector from 0 to 1 second
f1 = Fs/2;        % Target frequency of chirp set to Nyquist
in = sin(pi*f1*t.^2); % Linear chirp from 0 to Fs/2 Hz in 1 second
out = zeros(size(in)); % Output the same size as the input

for ii=1:length(in)
    out(ii) = mlhdlc_df2t_filter(in(ii));
end

% Plot
figure('Name', [mfilename, '_plot']);
subplot(2,1,1);
plot(in);
xlabel('Time')
ylabel('Amplitude')
title('Input Signal (with Noise)')

subplot(2,1,2);
plot(out);
xlabel('Time')
ylabel('Amplitude')
title('Output Signal (filtered)')
```

### **Create a New Folder and Copy Relevant Files**

Execute the following lines of code to copy the necessary example files into a temporary folder.

```
mlhdlc_demo_dir = fullfile(matlabroot, 'toolbox', 'hdlcoder', 'hdlcoderdemo');
mlhdlc_temp_dir = [tempdir 'mlhdlcflt2fix_prj'];

% create a temporary folder and copy the MATLAB files
cd(tempdir);
[~, ~, ~] = rmdir(mlhdlc_temp_dir, 's');
mkdir(mlhdlc_temp_dir);
cd(mlhdlc_temp_dir);

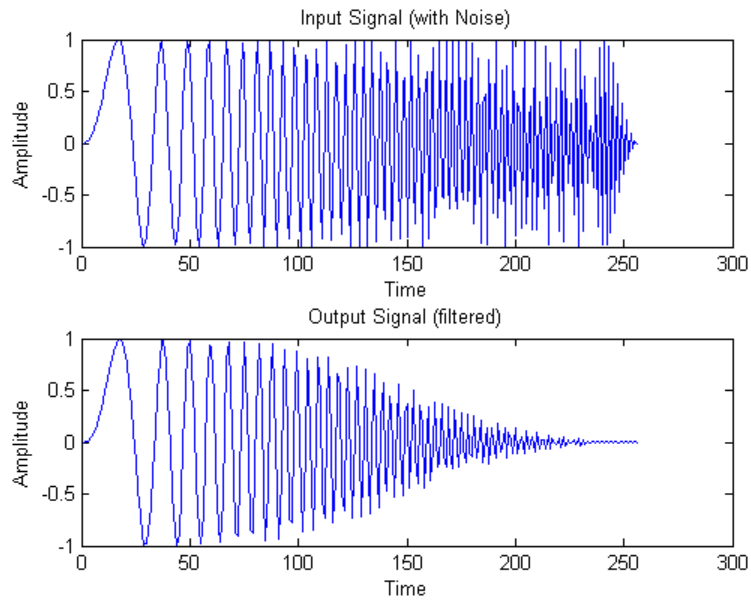
copyfile(fullfile(mlhdlc_demo_dir, design_name), mlhdlc_temp_dir);
copyfile(fullfile(mlhdlc_demo_dir, testbench_name), mlhdlc_temp_dir);
```

### **Simulate the Design**

Simulate the design with the test bench prior to code generation to make sure there are no runtime errors.

```
mlhdlc_df2t_filter_tb
```





### Create a New HDL Coder Project

To create a new project, enter the following command:

```
coder -hdlcoder -new flt2fix_project
```

Next, add the file 'mlhdlc\_filter.m' to the project as the MATLAB Function and 'mlhdlc\_filter\_tb.m' as the MATLAB Test Bench.

You can refer to Getting Started with MATLAB to HDL Workflow tutorial for a more complete tutorial on creating and populating MATLAB HDL Coder projects.

### Fixed-Point Code Generation Workflow

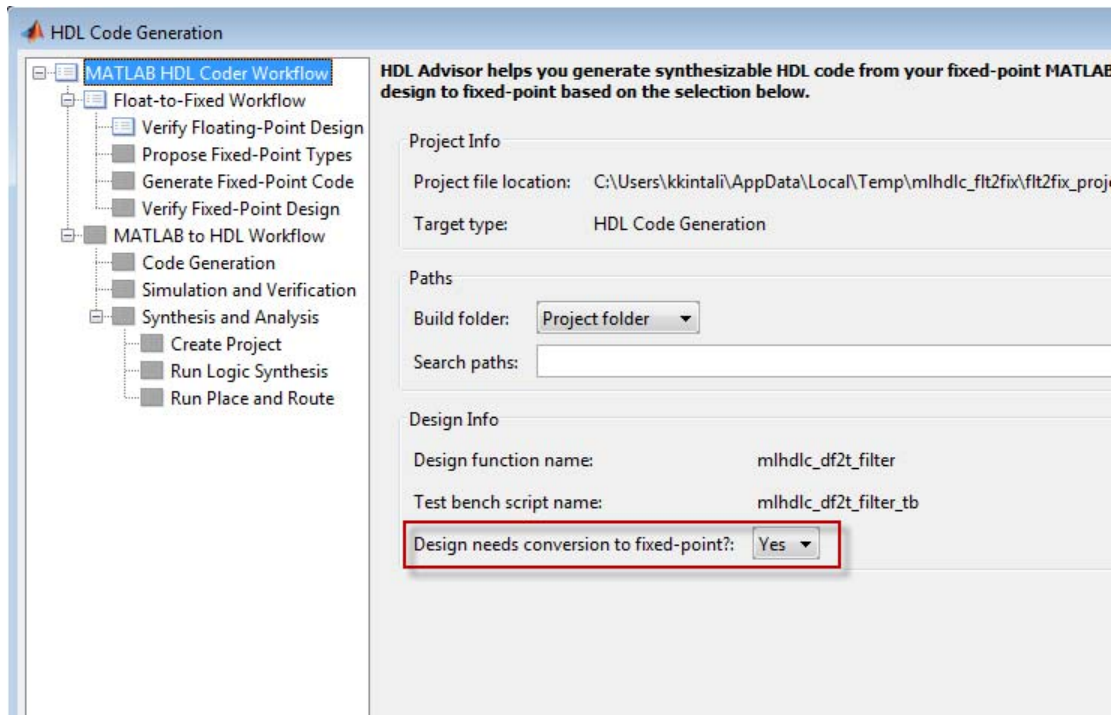
The floating-point to fixed-point conversion workflow allows you to:

- Verify that the floating-point design is code generation compliant

- Propose fixed-point types based on simulation data and word length settings
- Allow the user to manually adjust the proposed fixed-point types
- Generate fixed-point MATLAB code
- Verify that the generated fixed-point MATLAB code has the desired numeric accuracy

#### Step 1: Launch Workflow Advisor

- 1 Click the Advisor button to launch the Workflow Advisor.
- 2 Choose 'Yes' for the option 'Design needs conversion to fixed-point'.



#### Step 2: Verify the Floating-Point Design

- 1 Click the 'Verify Floating-Point Design' step.
- 2 Select the option, 'Log all IO for comparison plots'.
- 3 Click 'Run' to execute the instrumented floating-point simulation.

In this step, the original design is instrumented so that the minimum and maximum values for all variables in the design are collected during simulation.

The screenshot shows the HDL Code Generation tool interface. On the left, a tree view shows the workflow steps, with 'Verify Floating-Point Design' selected and marked with a green checkmark. On the right, the 'Analyze the MATLAB design and test bench; run a floating-point simulation to infer fixed-point types' step is active. Below the title bar, there are two checkboxes: 'Accelerate test bench for faster simulation' (unchecked) and 'Log all IO for comparison plots' (checked). The main output area shows the following text:

```

===== Step1: Verify Floating Point =====
Printing file dependency tree for mlhdlc_df2t_filter_tb
+ mlhdlc_df2t_filter_tb.m
+ mlhdlc_df2t_filter.m
### Analyzing the design 'mlhdlc_df2t_filter'
### Analyzing the test bench 'mlhdlc_df2t_filter_tb'
### Checking for streaming loop in the testbench 'mlhdlc_df2t_filter'
### Begin Floating Point Simulation (Instrumented)
### Generating Mex file for 'mlhdlc_df2t_filter_logged'

### Running Mex simulation
### Floating Point Simulation Completed in 0.0112 sec(s)
### Elapsed Time: 2.6056 sec(s)

```

Enabling the 'Log all IO for comparison plots' option captures all output data from the design during the floating-point simulation. This data is used later to compare against the output from the generated fixed-point code. This option only supports scalar variables.

### **Step 3: Determine Fixed-Point Types**

- 1** Click the 'Propose Fixed-Point Types' step.
- 2** Leave the default fixed-point settings.
- 3** Click 'Run'

Notice that the 'Proposed fixed-point types for variables' table is now populated with proposed types.

This step, for all variables, can compute and propose:

- Fraction lengths for a given fixed word length setting, or
- Word lengths for a given fixed fraction length setting.

This step proposes fixed-point types for each variable in the design based on the recorded min/max values of the floating point variables, along with your customizations to guide the type selection process.

**Propose fixed-point data types for variables in the MATLAB design based on simulation**

Basic Settings | **Advanced Settings**

Fixed-point type computation settings

Propose fraction lengths for specified word length

Propose word lengths for specified fraction length

Default word length:

Default fraction length:

Safety margin for simulation min/max (%):

Proposed fixed-point types for variables

Design	Variable	Min	Max
mlhdlc_df2t_filter	a	0.0	
	b	0.29290771484375	0.58578491
	x	-0.9999811752826012	
	y	-0.994520660237777	0.997456302
	z	-0.8000850613830756	0.798289314

[\[Clear Customizations\]](#)

[\[Show Types Report\]](#)

#### Step 4: Explore the Proposed Fixed-Point Type Table

The type table contains the following information for each variable existing in the floating-point MATLAB design, organized by function:

- Min: The minimum value assigned to the variable during simulation.

- Max: The maximum value assigned to the variable during simulation.
- Int: Whether all values assigned during simulation are integers.

The type proposal step uses the above information and combines it with the user-specified word length settings to propose a fixed-point type for each variable.

The values for 'RoundMode' and 'OverflowMode' can be controlled via the 'fimath Settings' control on the Advanced Settings tab.

```
fm = hdlfimath;  
fprintf(1, 'Rounding Mode: %s\nOverflow Mode: %s\n', fm.RoundMode, fm.OverflowMode);
```

```
Rounding Mode: floor  
Overflow Mode: wrap
```

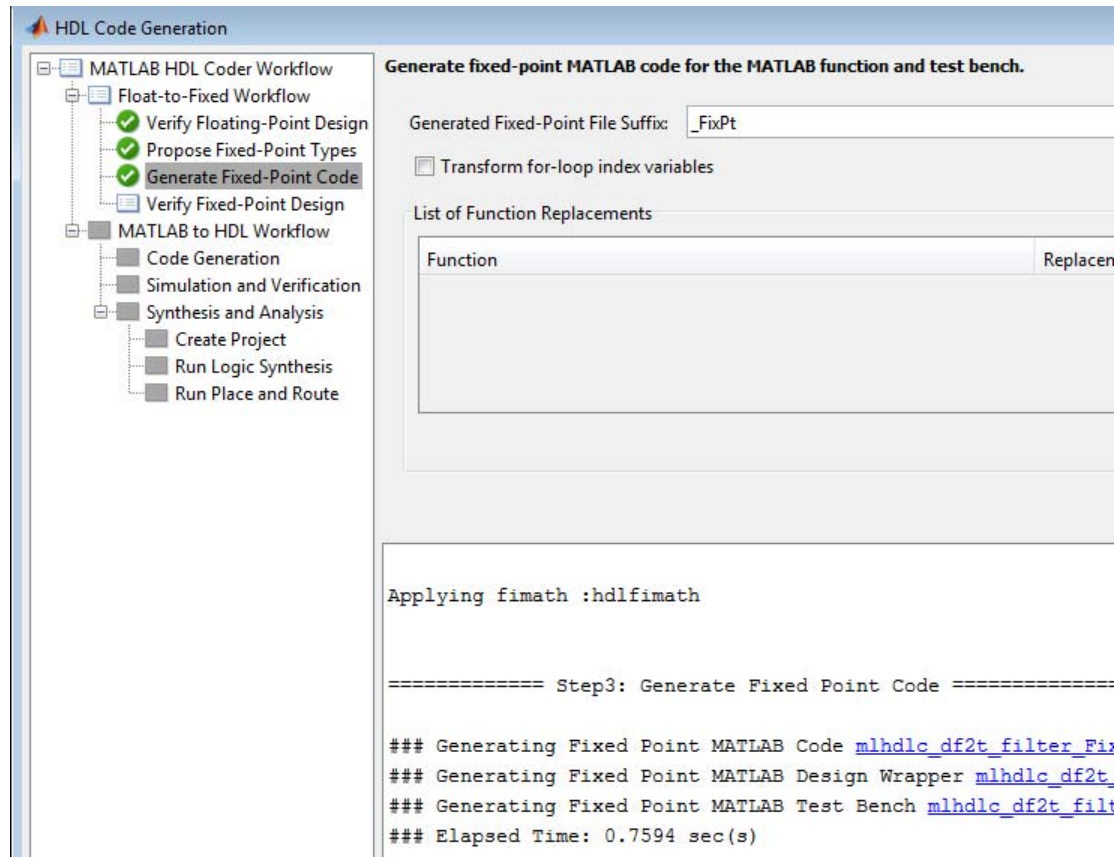
All information in the table is editable and is saved with your code generation project.

You can refer to the Fixed-Point Type Conversion and Refinement example for more details on this task.

#### **Step 5: Generate the Fixed-Point Code**

- 1** Click the 'Generate Fixed-Point Code' step.
- 2** Click 'Run'.

In this step, the fixed-point types from the previous step are used to generate a fixed-point MATLAB design from the original floating-point implementation.



The generated code and other conversion artifacts are available via hyperlinks in the output window. The fixed-point types are explicitly shown in the generated MATLAB code.

The screenshot displays the MATLAB Editor interface with two panes. The top pane shows the source MATLAB code for a function named `mlhdlc_df2t_filter`. The bottom pane shows the generated HDL Coder code for the same function, named `mlhdlc_df2t_filter_FixPt`.

**Top Pane: MATLAB Source Code**

```

1  %#codegen
2  function y = mlhdlc_df2t_filter(x)
3
4  persistent z a b;
5  if isempty(z)
6      % Filter states as a column vector
7      z = zeros(2,1);
8
9      % Filter coefficients as constants
10     b = [0.29290771484375    0.585784912109375    0.292907714843750];
11     a = [1.0                0.0                0.171600341796875];
12 end
13
14 y = b(1)*x + z(1);
15 z(1) = (b(2)*x + z(2)) - a(2) * y;
16 z(2) = b(3)*x - a(3) * y;
17
18 end
19

```

**Bottom Pane: Generated HDL Coder Code**

```

1  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
2  %
3  %           Generated by MATLAB 7.14, MATLAB Coder 2.2 and HDL Coder 3.0
4  %
5  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
6  %#codegen
7  function y = mlhdlc_df2t_filter_FixPt(x)
8
9  fm = hdlfimath;
10 persistent z a b
11 if isempty( z )
12     % Filter states as a column vector
13     z = fi(zeros( 2, 1 ), 1, 14, 13, fm);
14     % Filter coefficients as constants
15     b = fi([ 0.29290771484375, 0.585784912109375, 0.292907714843750 ], 0, 14, 14, f
16     a = fi([ 1.0, 0.0, 0.171600341796875 ], 0, 14, 13, fm);
17 end
18 y = fi(b( 1 )*x + z( 1 ), 1, 14, 12, fm);
19 z( 1 ) = fi((b( 2 )*x + z( 2 )) - a( 2 )*y, 1, 14, 13, fm);
20 z( 2 ) = fi(b( 3 )*x - a( 3 )*y, 1, 14, 13, fm);
21 end
22

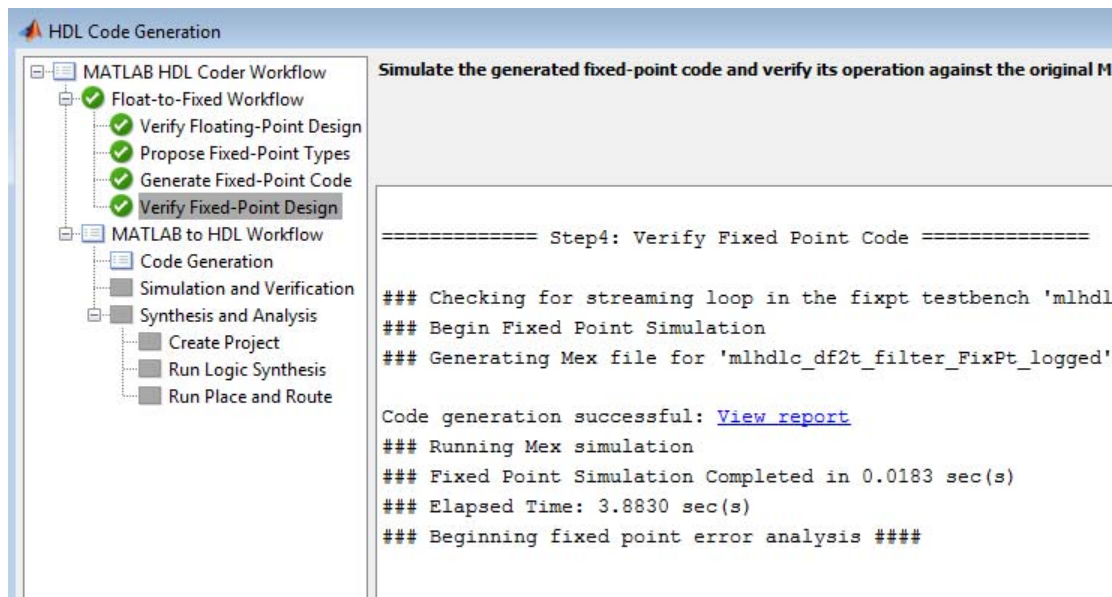
```



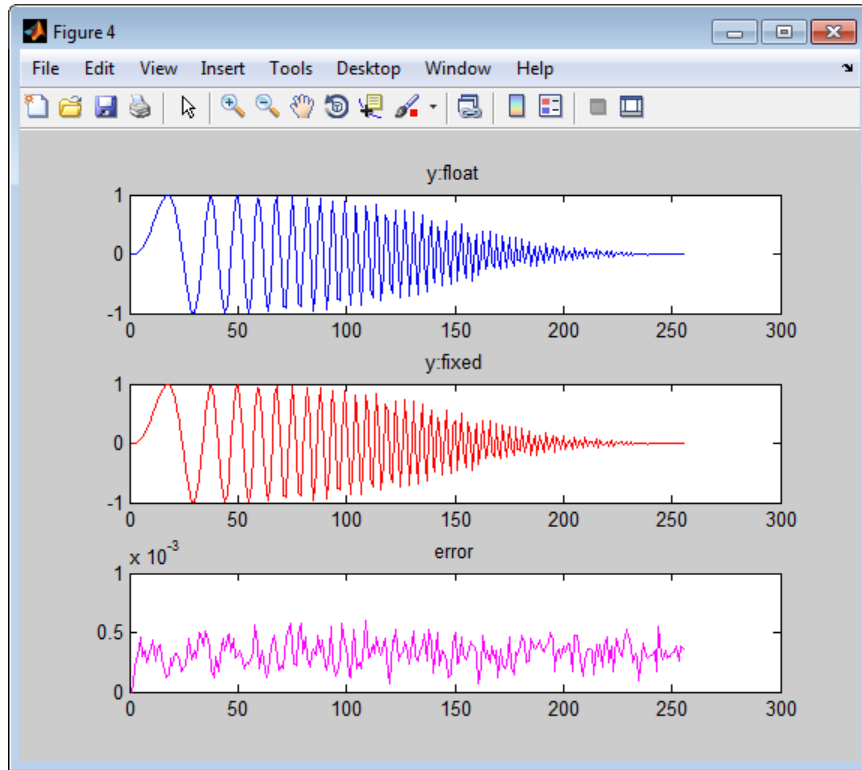
## Step 6: Verify the Generated Fixed-Point Code

- 1 Click the 'Verify Fixed-Point Design' step.
- 2 Click 'Run'.

In this step, the generated fixed-point code is executed using MATLAB Coder.



If you enable the 'Log all IO for comparison plots' option on the 'Verify Floating-Point Design' pane, an additional plot is generated for each scalar output that shows the floating point and fixed point results, as well as the difference between the two. For non-scalar outputs, only the error information is shown.



#### Step 7: Iterate on the Results

If the numerical results do not meet your desired accuracy after fixed-point simulation, you can return to the 'Propose Fixed-Point Types' step in the Workflow Advisor. Adjust the word length settings or individually modify types as desired, and repeat the rest of the steps in the workflow until you achieve your desired results.

You can refer to the Fixed-Point Type Conversion and Refinement example for more details on how to iterate and refine the numerics of the algorithm in the generated fixed-point code.

#### Clean up the Generated Files

Run the following commands to clean up the temporary project folder.

```
mlhdlc_demo_dir = fullfile(matlabroot, 'toolbox', 'hdlcoder', 'hdlcoderdemo');
mlhdlc_temp_dir = [tempdir 'mlhdlcflt2fix_prj'];
clear mex;
cd (mlhdlc_demo_dir);
rmdir(mlhdlc_temp_dir, 's');
```

## Fixed-Point Type Conversion and Refinement

This example shows how to achieve your desired numerical accuracy when converting fixed-point MATLAB code to floating-point code using the HDL Workflow Advisor.

### Introduction

The floating-point to fixed-point conversion workflow in HDL Coder™ includes the following steps:

- 1 Verify the floating-point design is compatible for code generation.
- 2 Compute fixed-point types based on the simulation of the testbench.
- 3 Generate readable and traceable fixed-point MATLAB code.
- 4 Verify the generated fixed-point design.

This tutorial uses a Kalman filter suitable for C code generation to illustrate some key aspects of fixed-point conversion workflow, specifically steps 2 and 3 in the above list.

### MATLAB Design

The MATLAB code used in this example implements a simple Kalman filter. This example also contains a MATLAB testbench that exercises the filter.

```
design_name = 'mlhdlc_kalman_c.m';  
testbench_name = 'mlhdlc_kalman_c_tb.m';
```

- 1 MATLAB Design: mlhdlc\_kalman\_c
- 2 MATLAB testbench: mlhdlc\_kalman\_c\_tb

### Create a New Folder and Copy Relevant Files

Execute the following lines of code to copy the necessary example files into a temporary folder.

```
mlhdlc_demo_dir = fullfile(matlabroot, 'toolbox', 'hdlcoder', 'hdlcoderdemo
```

```
mlhdlc_temp_dir = [tempdir 'mlhdlcflt2fix'];

% create a temporary folder and copy the MATLAB files
cd(tempdir);
[~, ~, ~] = rmdir(mlhdlc_temp_dir, 's');
mkdir(mlhdlc_temp_dir);
cd(mlhdlc_temp_dir);

copyfile(fullfile(mlhdlc_demo_dir, design_name), mlhdlc_temp_dir);
copyfile(fullfile(mlhdlc_demo_dir, testbench_name), mlhdlc_temp_dir);
copyfile(fullfile(mlhdlc_demo_dir, 'mlhdlc_backslash.m'), mlhdlc_temp_dir);
```

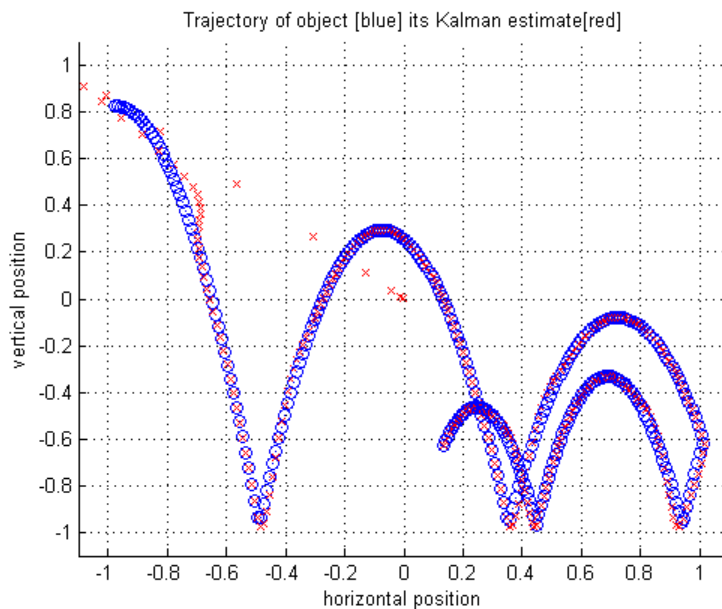
### **Simulate the Design**

Simulate the design with the testbench prior to code generation to make sure there are no runtime errors.

```
mlhdlc_kalman_c_tb
```

```
Running -----> mlhdlc_kalman_c_tb
```

```
Current plot held
Current plot released
```



#### Create a New HDL Coder Project

To create a new project, enter the following command:

```
coder -hdlcoder -new flt2fix_project
```

Next, add the file 'mlhdlc\_kalman\_c.m' to the project as the MATLAB Function and 'mlhdlc\_kalman\_c\_tb.m' as the MATLAB Test Bench.

You can refer to Getting Started with MATLAB to HDL Workflow tutorial for a more complete tutorial on creating and populating HDL Coder projects.

#### Fixed-Point Code Generation Workflow

Perform the following tasks before moving on to the fixed-point type proposal step:

- 1 Click the Advisor button to launch the Workflow Advisor.
- 2 Choose 'Yes' for the 'Design needs conversion to fixed-point' option.

- 3 Click the 'Verify Floating-Point Design' workflow step.
- 4 Select the option 'Log all IO for comparison plots'.
- 5 Click 'Run' to execute the instrumented floating-point simulation.

Refer to Floating-Point to Fixed-Point Conversion for a more complete tutorial on these steps.

### **Determine the Initial Fixed Point Types**

After instrumented floating-point simulation completes, you can move to the 'Propose Fixed-Point Types' step.

This step proposes fixed-point types for each variable in the design based on the recorded min/max values of the floating point variables and user input.

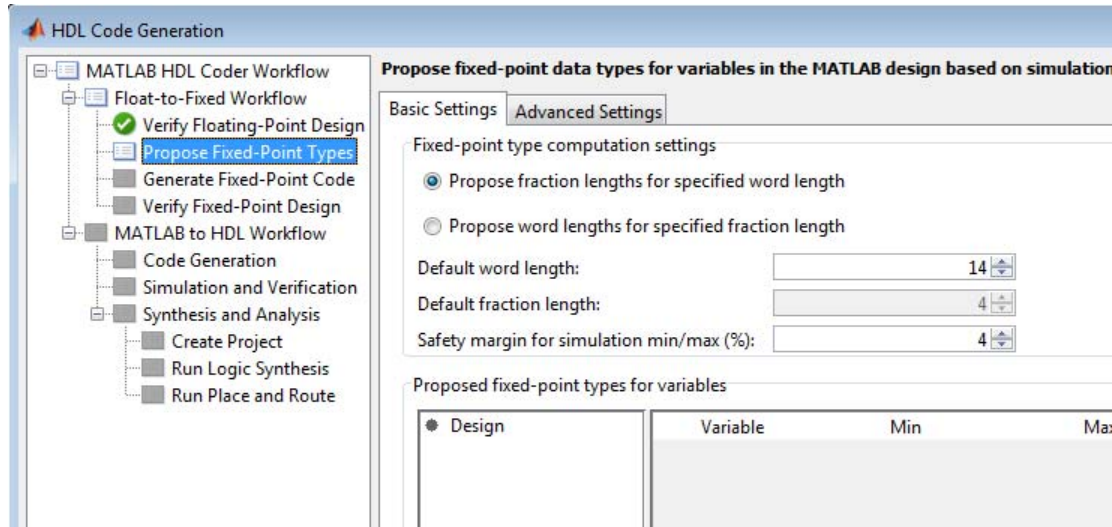
This step, for all variables, can compute and propose:

- Fraction lengths for a given fixed word length setting, or
- Word lengths for a given fixed fraction length setting.

### **Choose the Word Length Setting**

When you are starting with a floating-point design and going through the floating-point to fixed-point conversion for the first time, it is a good practice to start by specifying a 'Default Word Length' setting based on the largest dynamic range of all the variables in the design.

In this example, we start with a default word length of 14 and run the 'Propose Fixed-Point Types' step.



#### Explore the Proposed Fixed-Point Type Table

The type table contains the following information for each variable, organized by function, existing in the floating-point MATLAB design:

- Min: The minimum value assigned to the variable during simulation.
- Max: The maximum value assigned to the variable during simulation.
- Int: Whether all values assigned during simulation are integer.

The type proposal step uses the above information and combines it with the user-specified word length settings to propose a fixed-point type for each variable.

#### Interpret the Proposed Numeric Types for Variables

Based on the simulation range (min & max) values and the default word length setting, a numeric type is proposed for each variable.

The following table shows numeric type proposals for a 'Default word length' of 14 bits.



Propose fixed-point data types for variables in the MATLAB design based on simulation data and wordlength settings.

Basic Settings    **Advanced Settings**

Fixed-point type computation settings

Propose fraction lengths for specified word length

Propose word lengths for specified fraction length

Default word length:

Default fraction length:

Safety margin for simulation min/max (%):

Proposed fixed-point types for variables

Design	Variable	Min	Max	Int	ProposedType
● fl24_lu_decomp	A	0.0	1.0	<input checked="" type="checkbox"/>	ufix1
● fl25_fsubs	B	0.0	896.7420526311406	<input type="checkbox"/>	ufix14_En4
● fl26_bsubs	H	0.0	1.0	<input checked="" type="checkbox"/>	ufix1
● fl27_mlhdlc_backsla	Q	0.0	1.0	<input checked="" type="checkbox"/>	ufix1
● mlhdlc_kalman_c	R	0.0	1000.0	<input checked="" type="checkbox"/>	ufix11
	S	0.0	1896.7420526311407	<input type="checkbox"/>	ufix14_En3
	dt	1.0	1.0	<input checked="" type="checkbox"/>	ufix1
	klm_gain	0.0	0.47278018188461074	<input type="checkbox"/>	ufix14_En15
	p_est	0.0	472.7801818846108	<input type="checkbox"/>	ufix14_En5
	p_prd	0.0	896.7420526311406	<input type="checkbox"/>	ufix14_En4
	x_est	-1.138593320750606	1.014187225199087	<input type="checkbox"/>	sfix14_En12
	x_prd	-1.351820368460458	1.166096986676349	<input type="checkbox"/>	sfix14_En12
	y	-1.138593320750606	1.014187225199087	<input type="checkbox"/>	sfix14_En12
	y1	-1.138593320750606	1.014187225199087	<input type="checkbox"/>	sfix14_En12
	y2	-0.9750739274389443	0.9773013839510203	<input type="checkbox"/>	sfix14_En12
	z	-0.9760750075842789	1.0090797971434442	<input type="checkbox"/>	sfix14_En12
	z_prd	-1.351820368460458	1.166096986676349	<input type="checkbox"/>	sfix14_En12

Examine the types proposed in the above table for variables instrumented in the top-level design.

Floating-Point Range for variable 'B':

- Simulation Info: Min: 0, Max: 896.7420526311406, Always Integer: No
- Type Proposed: ufix14\_En4 (Signed: No, WordLength: 14, FractionLength: 4)

The floating-point range:

- Has the same number of bits as the 'Default word length'.

- Uses the minimum number of bits to completely represent the range.
- Uses the rest of the bits to represent the precision.

Integer Range for variable 'A':

- Simulation Info: Min: 0, Max: 1, Always Integer: Yes
- Type Proposed: ufix1 (Signed: No, WordLength: 1, FractionLength: 0)

The integer range:

- Has the minimum number of bits to represent the whole integer range.
- Has no fractional bits.

#### **Interpret the Proposed fimath for Variables**

The values for 'RoundMode' and 'OverflowMode' can be controlled via the 'fimath Settings' control on the 'Advanced Settings' tab.

```
fm = hdlfimath;  
fprintf(1, 'Rounding Mode: %s\nOverflow Mode: %s', fm.RoundMode, fm.OverflowMode);
```

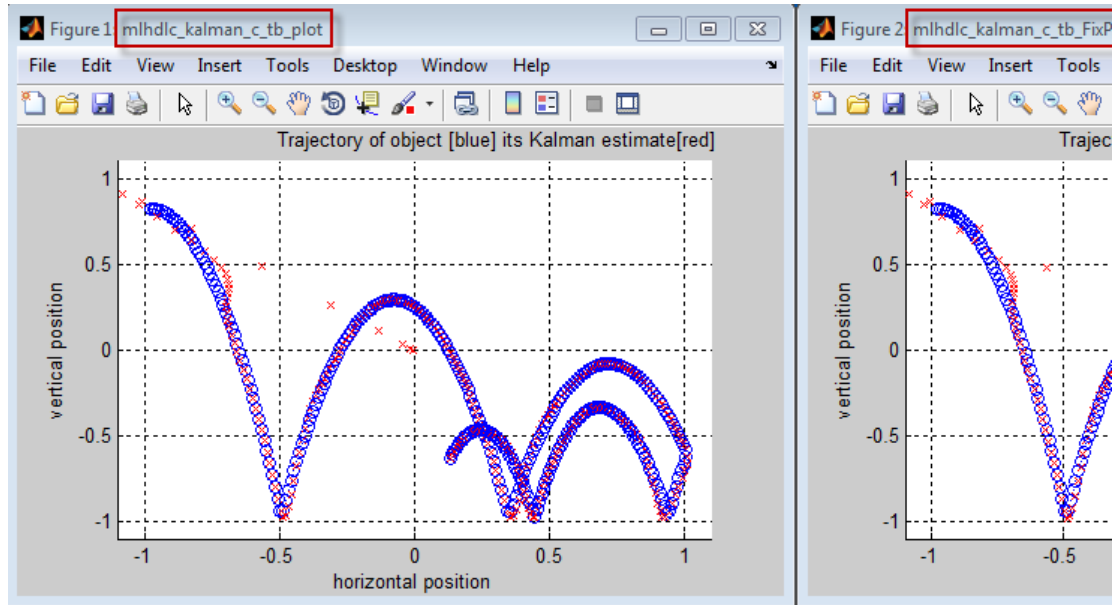
```
% hdlfimath is an easy way to specify hardware friendly parameters for  
% overflow and rounding modes.
```

```
Rounding Mode: floor  
Overflow Mode: wrap
```

All the information in the table is editable, persists across iterations, and is saved with your code generation project.

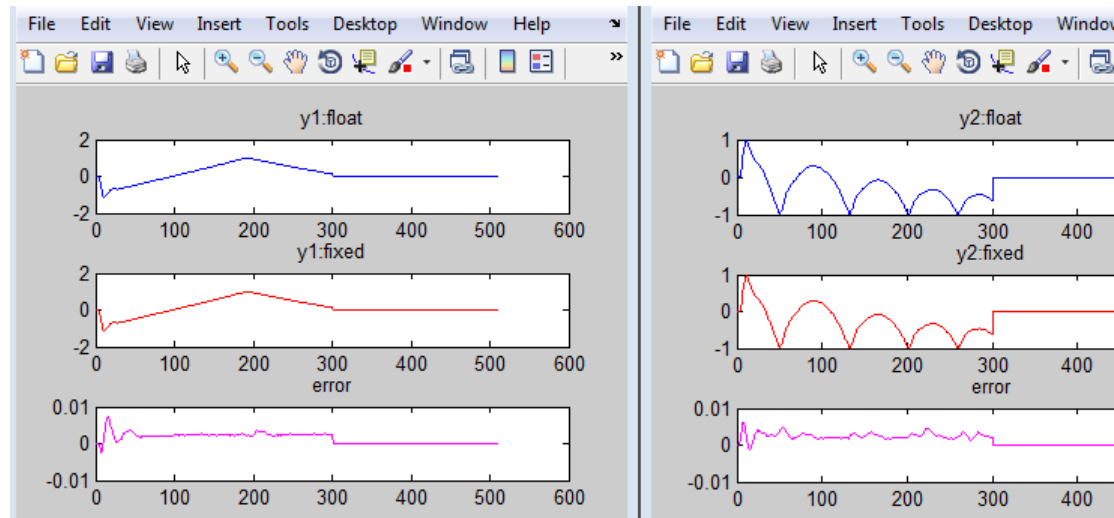
#### **Generate Fixed-Point Code and Verify the Generated Code**

Based on the numeric types proposed for a default word length of 14, continue with fixed-point code generation and verification steps and observe the plots.



Having chosen 'Log all IO for comparison plots', you see additional plots that compare the floating and fixed point simulation results for each output variable.

Examine the error graph for each output variable. It is very high for this particular design.



#### Iterate on the Results

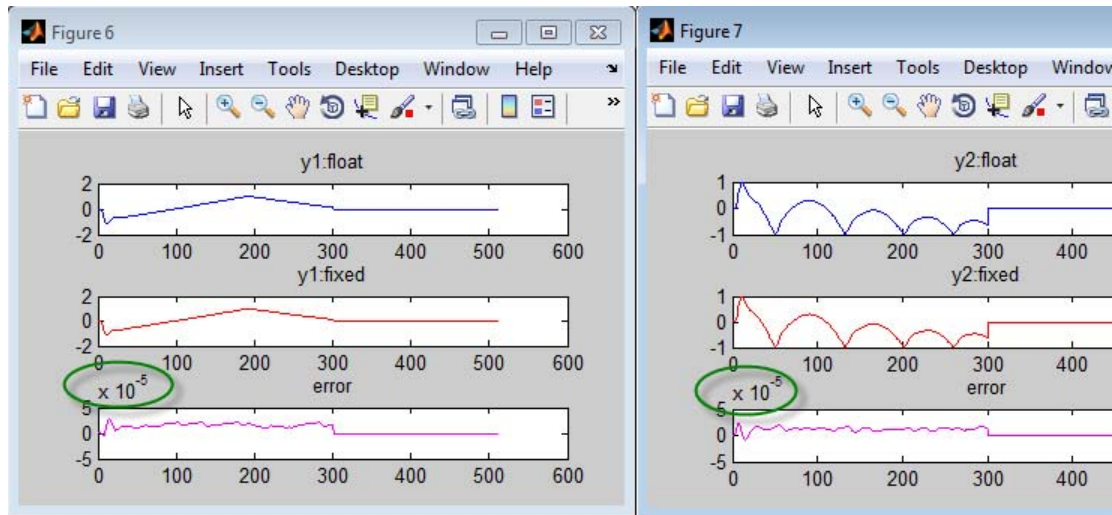
One way to reduce the error is to increase 'Default word length' and repeat the fixed-point conversion.

In this example design, when a word length of 14 bits is chosen there is a lot of truncation error when representing the precision. More bits are required to the right of the binary point to reduce the truncation errors.

Let us now increase the default word length to 22 bits and repeat the type proposal step.

- 1 Click 'Propose Fixed-Point Types'.
- 2 Select a 'Default word length' of 22.
- 3 Right-click 'Propose Fixed-Point Types' and select 'Run This Task'.
- 4 Right click 'Verify Fixed-Point Design' and select 'Run to Selected Task'.

Once these steps are complete, re-examine the comparison plots and notice that the error is now roughly three orders of magnitude smaller.



### Clean up the Generated Files

Run the following commands to clean up the temporary project folder.

```
mlhdlc_demo_dir = fullfile(matlabroot, 'toolbox', 'hdlcoder', 'hdlcoderdemo');
mlhdlc_temp_dir = [tempdir 'mlhdlcflt2fix'];
clear mex;
cd (mlhdlc_demo_dir);
rmdir(mlhdlc_temp_dir, 's');
```

## Working with Generated Fixed-Point Files

This example shows how to work with the files generated during floating-point to fixed-point conversion.

### Introduction

This tutorial uses a simple filter implemented in floating-point and an associated testbench to illustrate the file structure of the generated fixed-point code.

```
design_name = 'mlhdlc_filter.m';  
testbench_name = 'mlhdlc_filter_tb.m';
```

### MATLAB Code

**1** MATLAB Design: mlhdlc\_filter

**2** MATLAB testbench: mlhdlc\_filter\_tb

### Create a New Folder and Copy Relevant Files

Executing the following lines of code copies the necessary example files into a temporary folder.

```
mlhdlc_demo_dir = fullfile(matlabroot, 'toolbox', 'hdlcoder', 'hdlcoderdemo');  
mlhdlc_temp_dir = [tempdir 'mlhdlcflt2fix'];
```

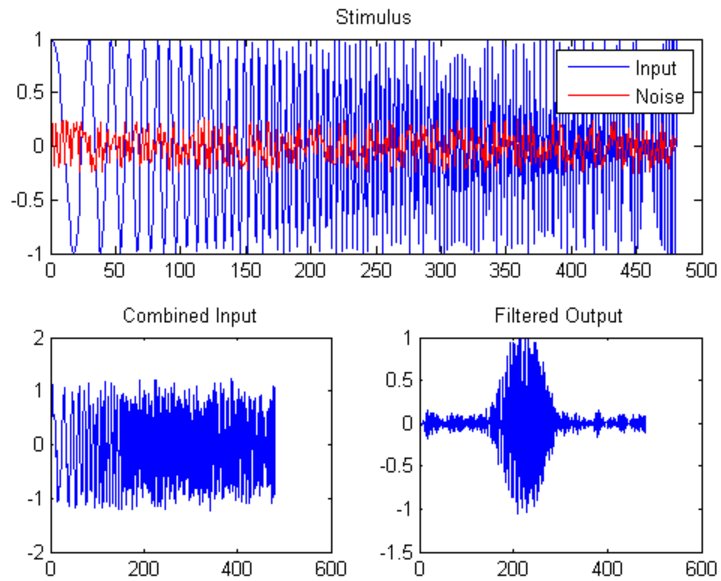
```
% create a temporary folder and copy the MATLAB files  
cd(tempdir);  
[~, ~, ~] = rmdir(mlhdlc_temp_dir, 's');  
mkdir(mlhdlc_temp_dir);  
cd(mlhdlc_temp_dir);
```

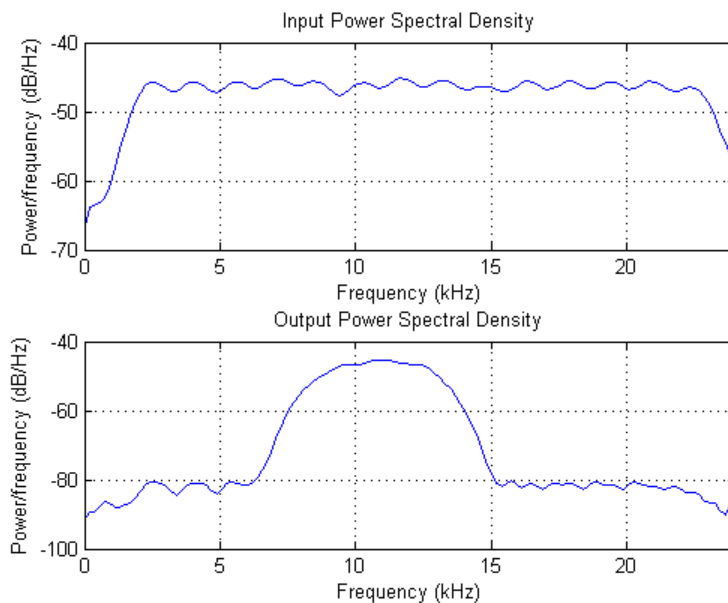
```
copyfile(fullfile(mlhdlc_demo_dir, design_name), mlhdlc_temp_dir);  
copyfile(fullfile(mlhdlc_demo_dir, testbench_name), mlhdlc_temp_dir);
```

### Simulate the Design

Simulate the design with the testbench prior to code generation to make sure there are no runtime errors.

```
mlhdlc_filter_tb
```





#### Create a New HDL Coder™ Project

To create a new project, enter the following command:

```
coder -hdlcoder -new flt2fix_project
```

Next, add the file 'mlhdlc\_filter' to the project as the MATLAB Function and 'mlhdlc\_filter\_tb' as the MATLAB Test Bench.

You can refer to the Getting Started with MATLAB to HDL Workflow tutorial for a more complete tutorial on creating and populating MATLAB HDL Coder projects.

#### Fixed-Point Code Generation Workflow

Perform the following tasks in preparation for the fixed-point code generation step:

- 1 Click the Advisor button to launch the Workflow Advisor.

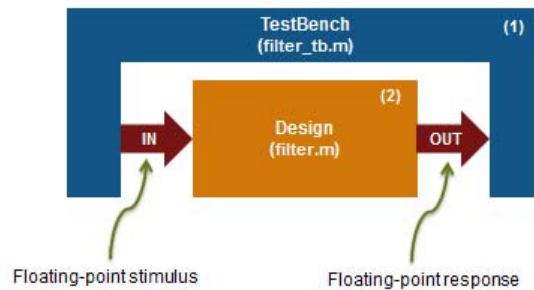


- 2 Choose 'Yes' for the option 'Design needs conversion to fixed-point'.
- 3 Right-click the 'Propose Fixed-Point Types' step.
- 4 Choose 'Run to Selected Task' to execute the instrumented floating-point simulation.

Refer to the Floating-Point to Fixed-Point Conversion tutorial for a more complete description of these steps.

### Floating-Point Design Structure

The original floating-point design and testbench have the following relationship.



For floating-point to fixed-point conversion, the following requirements apply to the original design and the testbench:

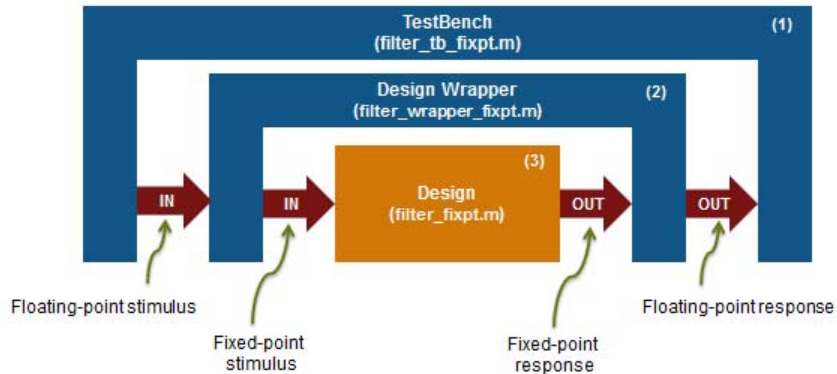
- The testbench 'mlhdlc\_filter\_tb.m' (1) must be a script or a function with no inputs.
- The design 'mlhdlc\_filter.m' (2) must be a function.
- There must be at least one call to the design from the testbench. All call sites contribute when determining the proposed fixed-point types.

- The design input interface (types, size, and complexity) is inferred from the data values driven by the testbench, and must be the same for all call sites throughout simulation.
- Both the design and testbench can call other sub-functions within the file or other functions on the MATLAB path. Functions that exist within matlab/toolbox are not converted to fixed-point.

In the current example, the MATLAB testbench 'mlhdlc\_filter\_tb' has a single call to the design function 'mlhdlc\_filter'. The testbench calls the design with floating-point inputs and accumulates the floating-point results for plotting.

#### Generate the Fixed-Point Code

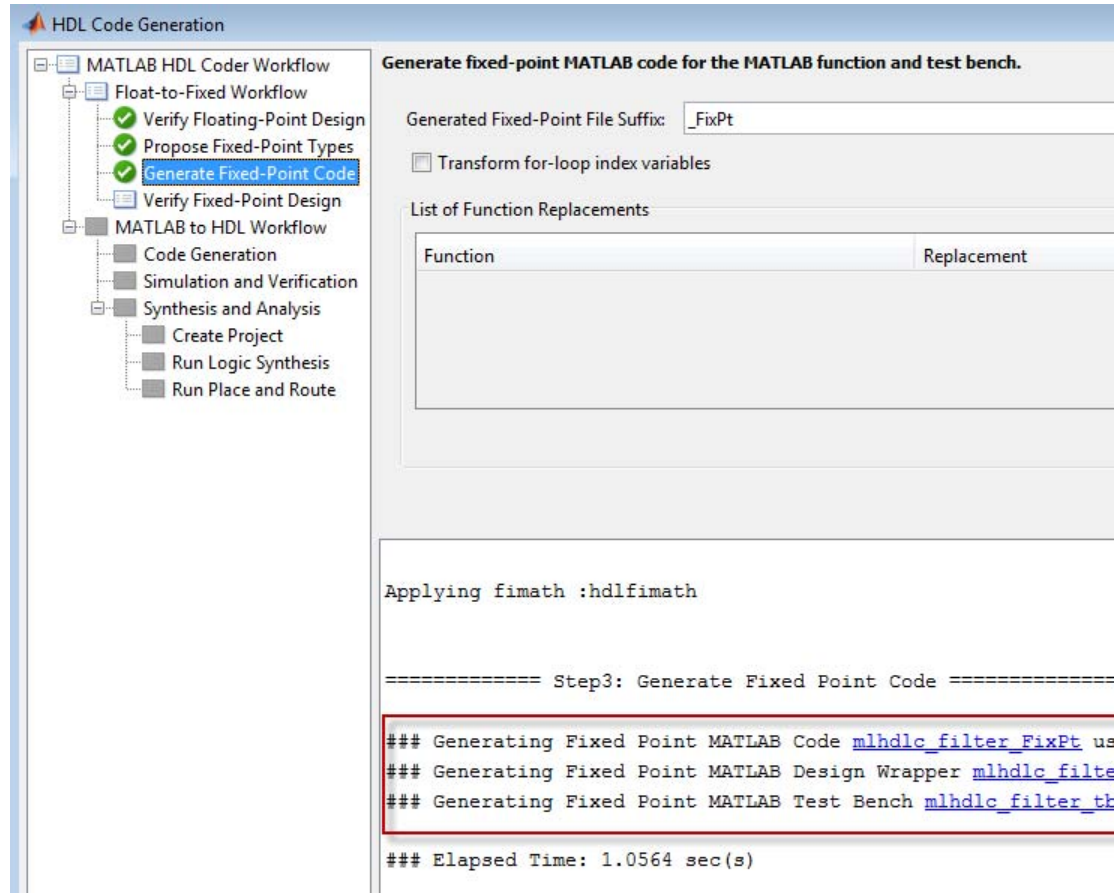
Generate fixed-point code for this design by clicking the 'Run' button from the 'Generate Fixed-Point Code' step. The output files will have the following structure.



The following steps are performed during fixed-point code generation:

- 1 The design file 'mlhdlc\_filter.m' is converted to fixed-point and generates fixed-point MATLAB code, 'mlhdlc\_filter\_FixPt.m' (3).

- 2** All user-written functions called in the floating-point design are converted to fixed-point and included in the generated design file.
- 3** A new design wrapper file is created, called `'mlhdlc_filter_wrapper_FixPt.m'` (2). This file converts the floating-point data values supplied by the testbench to the fixed-point types determined for the design inputs during the conversion step. These fixed-point values are fed into the converted fixed-point design, `'mlhdlc_filter_FixPt.m'`.
- 4** A new testbench file, `'mlhdlc_filter_tb_FixPt.m'`, is created. This file is identical to the original testbench, `'mlhdlc_filter_tb'`, except that it calls the fixed-point wrapper function `'filter_wrapper_FixPt'` instead of the original design function.
- 5** `'mlhdlc_filter_FixPt.m'` will be used for HDL code generation.
- 6** All the generated fixed-point files are stored in the output directory `'codegen/filter/fixpt'`.



Click the links to the generated code in the Workflow Advisor log window to examine the generated fixed-point design, wrapper, and test bench.

#### Clean up the Generated Files

Run the following commands to clean up the temporary project folder.

```
mlhdlc_demo_dir = fullfile(matlabroot, 'toolbox', 'hdlcoder', 'hdlcoderdemo');
mlhdlc_temp_dir = [tempdir 'mlhdlcflt2fix'];
clear mex;
```

```
cd (mlhdlc_demo_dir);  
rmdir(mlhdlc_temp_dir, 's');
```

## MATLAB Function Block Generation

### In this section...

“Requirements for MATLAB Function Block Generation” on page 3-54

“Enable MATLAB Function Block Generation” on page 3-54

“Results of MATLAB Function Block Generation” on page 3-54

### Requirements for MATLAB Function Block Generation

During HDL code generation, your MATLAB algorithm must go through the floating-point to fixed-point conversion process, even if it is already a fixed-point algorithm.

### Enable MATLAB Function Block Generation

#### Using the GUI

To enable MATLAB Function block generation using the HDL Workflow Advisor:

- 1** In the HDL Workflow Advisor, on the left, click **Code Generation**.
- 2** In the **Advanced** tab, select the **Generate MATLAB Function Block Box** option.

#### Using the Command Line

To enable MATLAB Function block generation, at the command line, enter:

```
hdlcfg = coder.config('hdl');  
hdlcfg.GenerateMLFcnBlock = true;
```

### Results of MATLAB Function Block Generation

After you generate HDL code, an untitled model opens containing a MATLAB Function block.

You can use the MATLAB Function block as part of a larger model in Simulink for simulation and further HDL code generation.

To learn more about generating a MATLAB Function block from a MATLAB algorithm, see “System Design with HDL Code Generation from MATLAB and Simulink” on page 3-56.

## System Design with HDL Code Generation from MATLAB and Simulink

This example shows how to generate a MATLAB Function block from a MATLAB design for system simulation, code generation, and FPGA programming in Simulink.

### Introduction

HDL Coder can generate HDL code from both MATLAB and Simulink. The coder can also generate a Simulink component, the MATLAB Function block, from your MATLAB code.

This capability enables you to:

- 1 Design an algorithm in MATLAB;
- 2 Generate a MATLAB Function block from your MATLAB design;
- 3 Use the MATLAB component in a Simulink model of the system;
- 4 Simulate and optimize the system model;
- 5 Generate HDL code; and
- 6 Program an FPGA with the entire system design.

In this example, you will generate a MATLAB Function block from MATLAB code that implements a FIR filter.

### MATLAB Design

The MATLAB code used in the example is a simple FIR filter. The example also shows a MATLAB testbench that exercises the filter.

```
design_name = 'mlhdlc_fir.m';  
testbench_name = 'mlhdlc_fir_tb.m';
```

- 1 Design: mlhdlc\_fir
- 2 Test Bench: mlhdlc\_fir\_tb



### Create a New Folder and Copy Relevant Files

Execute the following lines of code to copy the example files into a temporary folder.

```
mlhdlc_demo_dir = fullfile(matlabroot, 'toolbox', 'hdlcoder', 'hdlcoderdemo');
mlhdlc_temp_dir = [tempdir 'mlhdlc_fir'];

% Create a temporary folder and copy the MATLAB files
cd(tempdir);
[~, ~, ~] = rmdir(mlhdlc_temp_dir, 's');
mkdir(mlhdlc_temp_dir);
cd(mlhdlc_temp_dir);

copyfile(fullfile(mlhdlc_demo_dir, design_name), mlhdlc_temp_dir);
copyfile(fullfile(mlhdlc_demo_dir, testbench_name), mlhdlc_temp_dir);
```

### Simulate the Design

To simulate the design with the test bench prior to code generation to make sure there are no runtime errors, enter the following command:

```
mlhdlc_fir_tb
```

### Create a New Project

To create a new HDL Coder project, enter the following command:

```
coder -hdlcoder -new fir_project
```

Next, add the file 'mlhdlc\_fir.m' to the project as the MATLAB Function and 'mlhdlc\_fir\_tb.m' as the MATLAB Test Bench.

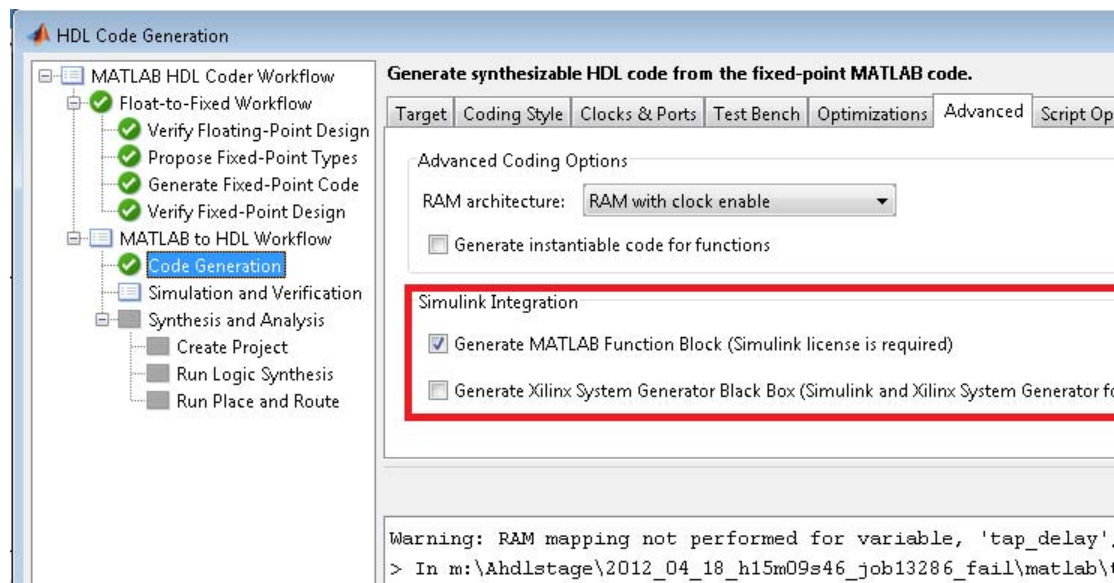
Click the Workflow Advisor button to launch the HDL Workflow Advisor.

### Enable the MATLAB Function Block Option

To generate a MATLAB Function block from a MATLAB HDL design, you must have a Simulink license. If the following command returns '1', Simulink is available:

```
license('test', 'Simulink')
```

In the HDL Workflow Advisor Advanced tab, enable the Generate MATLAB Function Block option.



### Run Floating-Point to Fixed-Point Conversion and Generate Code

To generate a MATLAB Function block, you must also convert your design from floating-point to fixed-point.

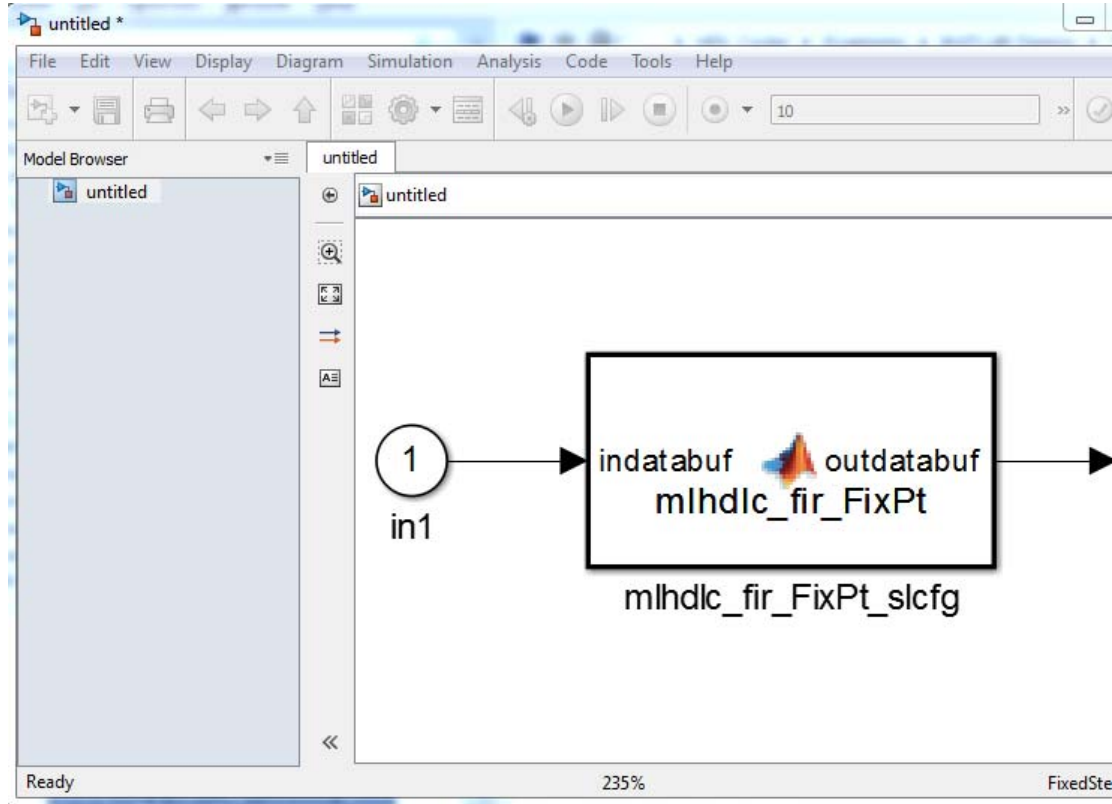
Right-click the 'Code Generation' step and choose the option 'Run to selected task' to run all the steps from the beginning through HDL code generation.

### Examine the Generated MATLAB Function Block

An untitled model opens after HDL code generation. It has a MATLAB Function block containing the fixed-point MATLAB code from your MATLAB HDL design. HDL Coder automatically applies settings to the model and MATLAB Function block so that they can simulate in Simulink and generate HDL code.

To generate HDL code from the MATLAB Function block, enter the following command:

```
makehdl('untitled');
```



You can rename and save the new block to use in a larger Simulink design.

### Clean Up the Generated Files

You can run the following commands to clean up the temporary project folder.

```
mlhdlc_demo_dir = fullfile(matlabroot, 'toolbox', 'hdlcoder', 'hdlcoderdemo');  
mlhdlc_temp_dir = [tempdir 'mlhdlc_fir'];
```

```
clear mex;  
cd (mlhdlc_demo_dir);  
rmdir(mlhdlc_temp_dir, 's');
```

# Xilinx System Generator Black Box Block Generation

## In this section...

“Requirements for System Generator Black Box Block Generation” on page 3-61

“Enable System Generator Black Box Block Generation” on page 3-61

“Results of System Generator Black Box Block Generation” on page 3-62

## Requirements for System Generator Black Box Block Generation

You must have Xilinx® ISE Design Suite 13.4 or later to generate a System Generator Black Box block.

To verify your System Generator setup, at the command line, enter:

```
xlVersion
```

## Enable System Generator Black Box Block Generation

### Using the GUI

To enable System Generator Black Box block generation using the HDL Workflow Advisor:

- 1 In the HDL Workflow Advisor, on the left, click **Code Generation**.
- 2 In the **Advanced** tab, select the **Generate Xilinx System Generator Black Box** option.
- 3 In the **Clocks & Ports** tab, set the following fields:
  - For **Clock input port**, enter `clk`.
  - For **Clock enable input port**, enter `ce`.
  - For **Drive clock enable at**, select **DUT base rate**.

### **Using the Command Line**

To enable System Generator Black Box block generation, at the command line, enter:

```
hdlcfg = coder.config('hdl');  
hdlcfg.GenerateXSGBlock = true;  
hdlcfg.ClockInputPort = 'clk';  
hdlcfg.ClockEnableInputPort = 'ce';  
hdlcfg.EnableRate = 'DutBaseRate';
```

### **Results of System Generator Black Box Block Generation**

After you generate HDL code, you have:

- An XSG subsystem.
- A System Generator Black Box block within the XSG subsystem.
- A System Generator Black Box configuration M-function.

You can use the XSG subsystem in a Simulink model, or use the Black Box block and Black Box configuration M-function in a Xilinx System Generator design.

To learn more about generating a System Generator Black Box block, see “Using Xilinx System Generator for DSP with HDL Coder” on page 15-25.

# Generate Xilinx System Generator for DSP Black Box from MATLAB HDL Design

This example shows how to generate a Xilinx System Generator for DSP Black Box block from a MATLAB HDL design.

## Introduction

HDL Coder can generate a System Generator Black Box block and configuration file from your MATLAB HDL design. After designing an algorithm in MATLAB for HDL code generation, you can then integrate it into a larger system as a Xilinx System Generator Black Box block.

HDL Coder places the generated Black Box block in a Xilinx System Generator (XSG) subsystem. XSG subsystems work with blocks from both Simulink and Xilinx System Generator, so you can use the generated black box block to build a larger system for simulation and code generation.

## MATLAB Design

The MATLAB code in the example implements a simple FIR filter. The example also shows a MATLAB testbench that exercises the filter.

```
design_name = 'mlhdlc_fir.m';  
testbench_name = 'mlhdlc_fir_tb.m';
```

**1** Design: mlhdlc\_fir

**2** Test Bench: mlhdlc\_fir\_tb

## Create a New Folder and Copy Relevant Files

Execute the following lines of code to copy the necessary example files into a temporary folder.

```
mlhdlc_demo_dir = fullfile(matlabroot, 'toolbox', 'hdlcoder', 'hdlcoderdem  
mlhdlc_temp_dir = [tempdir 'mlhdlc_fir'];
```

```
% Create a temporary folder and copy the MATLAB files  
cd(tempdir);
```

```
[~, ~, ~] = rmdir(mlhdlc_temp_dir, 's');  
mkdir(mlhdlc_temp_dir);  
cd(mlhdlc_temp_dir);  
  
copyfile(fullfile(mlhdlc_demo_dir, design_name), mlhdlc_temp_dir);  
copyfile(fullfile(mlhdlc_demo_dir, testbench_name), mlhdlc_temp_dir);
```

#### **Simulate the Design**

To simulate the design with the test bench to make sure there are no runtime errors before code generation, enter the following command:

```
mlhdlc_fir_tb
```

#### **Create a New Project From the Command Line**

To create a new project, enter the following command:

```
coder -hdlcoder -new fir_project
```

Next, add the file 'mlhdlc\_fir.m' to the project as the MATLAB Function and 'mlhdlc\_fir\_tb.m' as the MATLAB Test Bench.

Click the Workflow Advisor button to launch the HDL Workflow Advisor.

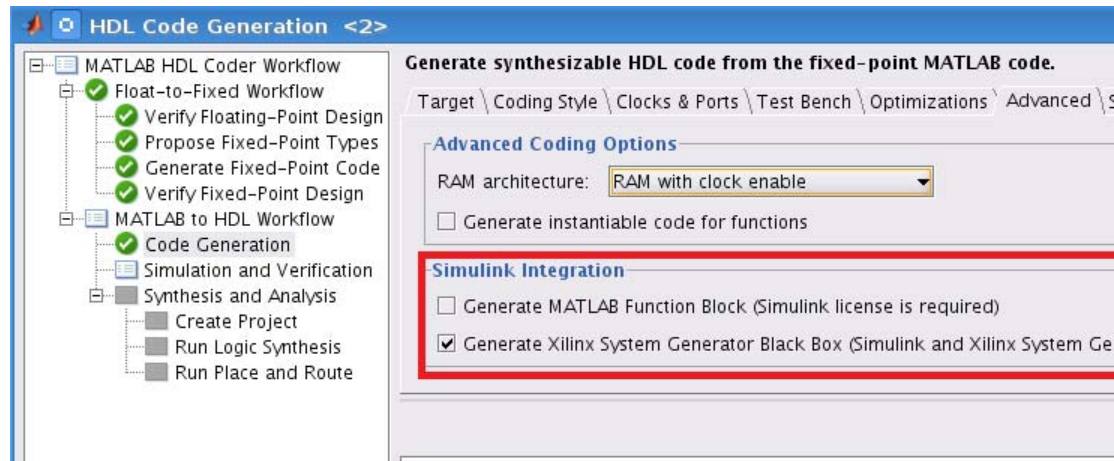
#### **Generate a Xilinx System Generator for DSP Black Box**

To generate a Xilinx System Generator Black Box from a MATLAB HDL design, you must have Xilinx System Generator configured. Enter the following command to check System Generator availability:

```
xlVersion
```

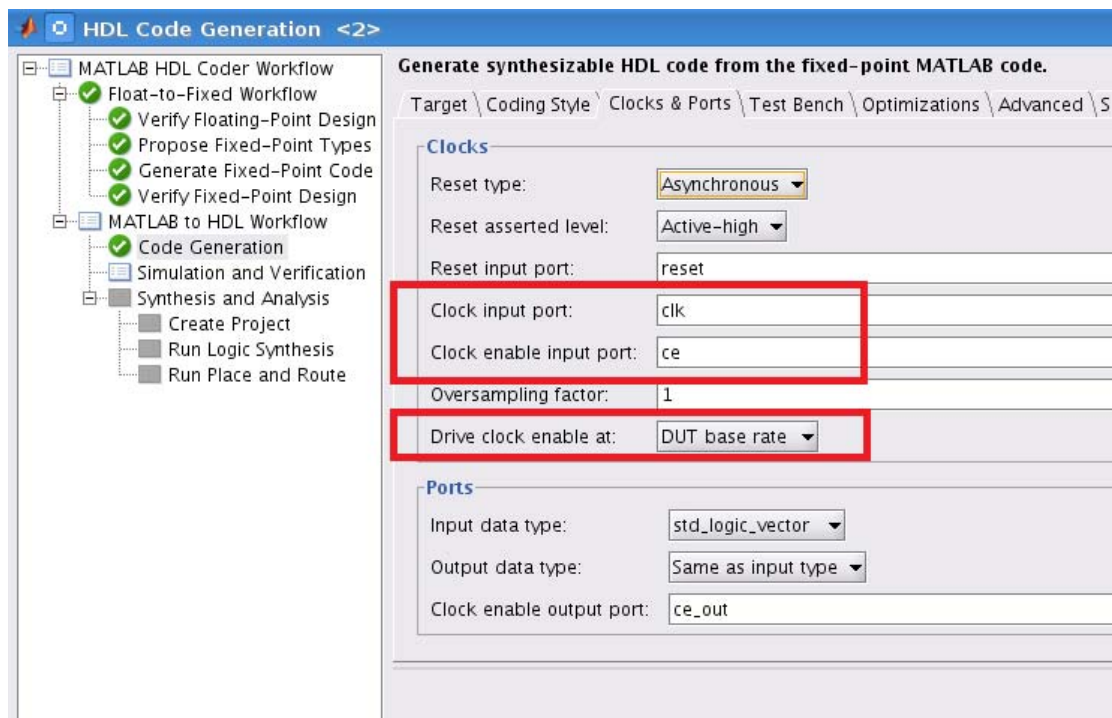
In the Advanced tab of the Workflow Advisor, enable the Generate Xilinx System Generator Black Box option:





To generate code compatible with a Xilinx System Generator Black Box, set:

- 'Clock input port' to 'clk'
- 'Clock enable input port' to 'ce'
- 'Drive clock enable at' to 'DUT base rate'



#### Run Fixed-Point Conversion and Generate Code

Right-click the 'Code Generation' step and choose the 'Run to selected task' option to run all the steps from the beginning through HDL code generation.

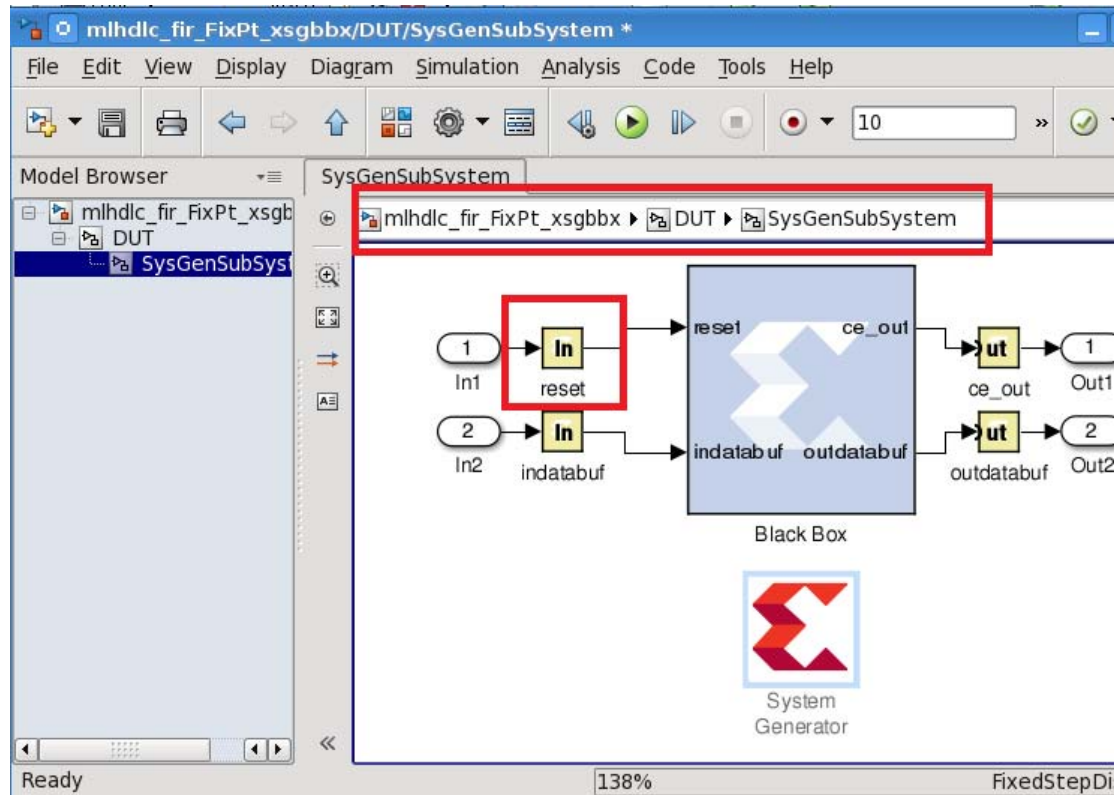
#### Examine the Generated Model and Config File

A new model opens after HDL code generation. It contains a subsystem called DUT at the top level.

The DUT subsystem has an XSG subsystem called SysGenSubSystem, which contains:

- A Xilinx System Generator Black Box block
- A System Generator block

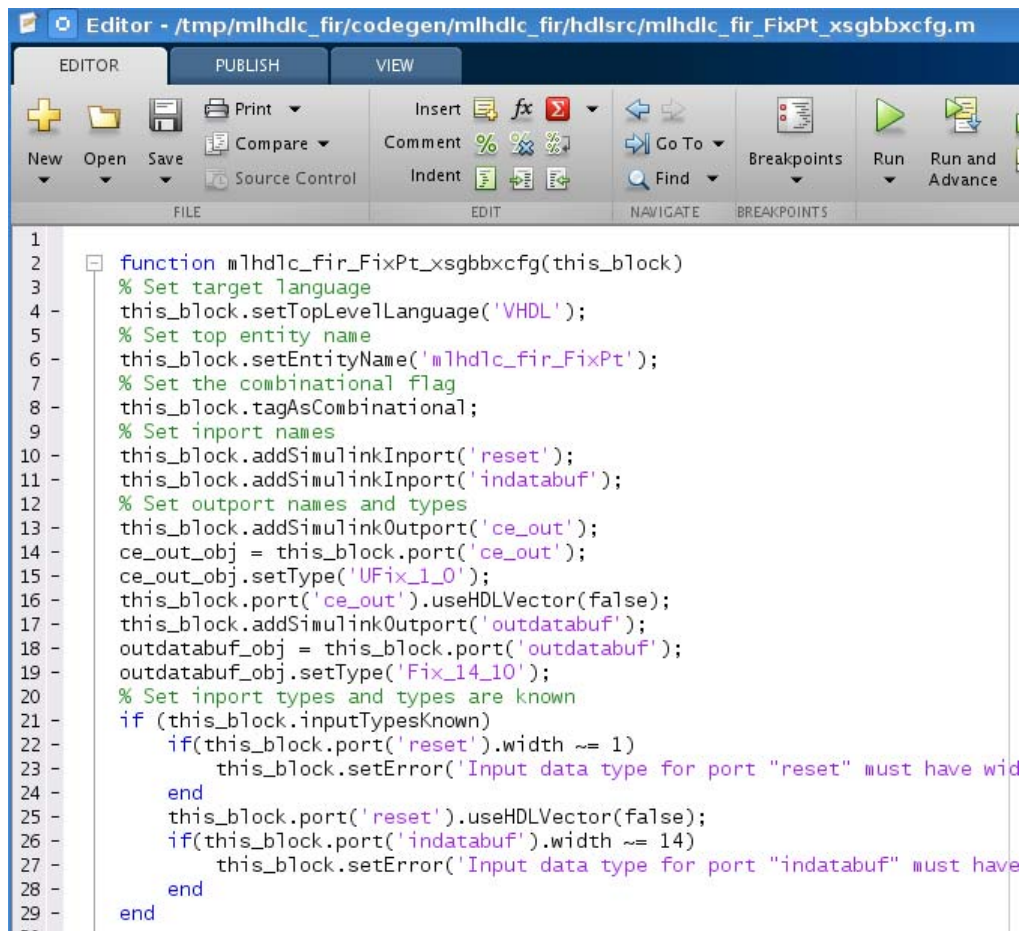
- Gateway-in blocks
- Gateway-out blocks



Notice that in addition to the data ports, there is a reset port on the black box interface, while 'clk' and 'ce' are registered to System Generator by the Black Box configuration file.

The configuration file and your new model are saved in the same directory with generated HDL code. You can open the configuration file by entering the following command:

```
edit('codegen/mlhdlc_fir/hdlsrc/mlhdlc_fir_FixPt_xsgbbxcfg.m');
```



```

1
2  function mlhdlc_fir_FixPt_xsgbbxcfg(this_block)
3  % Set target language
4  this_block.setTopLevelLanguage('VHDL');
5  % Set top entity name
6  this_block.setEntityName('mlhdlc_fir_FixPt');
7  % Set the combinational flag
8  this_block.tagAsCombinational;
9  % Set inport names
10 this_block.addSimulinkInport('reset');
11 this_block.addSimulinkInport('indatabuf');
12 % Set output names and types
13 this_block.addSimulinkOutport('ce_out');
14 ce_out_obj = this_block.port('ce_out');
15 ce_out_obj.setType('UFix_1_0');
16 this_block.port('ce_out').useHDLVector(false);
17 this_block.addSimulinkOutport('outdatabuf');
18 outdatabuf_obj = this_block.port('outdatabuf');
19 outdatabuf_obj.setType('Fix_14_10');
20 % Set inport types and types are known
21 if (this_block.inputTypesKnown)
22     if(this_block.port('reset').width ~= 1)
23         this_block.setError('Input data type for port "reset" must have width 1');
24     end
25     this_block.port('reset').useHDLVector(false);
26     if(this_block.port('indatabuf').width ~= 14)
27         this_block.setError('Input data type for port "indatabuf" must have width 14');
28     end
29 end
30

```

You can now use the generated Xilinx System Generator Black Box block and configuration file in a larger system design.

### Clean up the Generated Files

Run the following commands to clean up the temporary project folder.

```

mlhdlc_demo_dir = fullfile(matlabroot, 'toolbox', 'hdlcoder', 'hdlcoderdemo');
mlhdlc_temp_dir = [tempdir 'mlhdlc_fir'];

```

```
clear mex;  
cd (mlhdlc_demo_dir);  
rmdir(mlhdlc_temp_dir, 's');
```

# Generate Code Using the Command Line Interface

You can use the command line interface to generate HDL code from your MATLAB design and convert your design from floating-point to fixed-point.

To learn how to use the command line interface, open the tutorial:

```
showdemo mlhdlc_tutorial_cli
```

## Clock Enable Rate Specification

### In this section...

“Why Specify the Clock Enable Rate?” on page 3-71

“How to Specify the Clock Enable Rate” on page 3-71

### Why Specify the Clock Enable Rate?

When the coder performs area optimizations, it might upsample parts of your design (DUT), and thereby introduce an increase in your required DUT clock frequency.

If the coder upsamples your design, it generates a message indicating the ratio between the new clock frequency and your original clock frequency. For example, the following message indicates that your design’s new required clock frequency is 4 times higher than the original frequency:

```
The design requires 4 times faster clock with respect to the base rate = 1
```

This frequency increase introduces a rate mismatch between your input clock enable and output clock enable, because the output clock enable runs at the slower original clock frequency.

With the **Drive clock enable at** option, you can choose whether to drive the input clock enable at the faster rate (**DUT base rate**) or at a rate that is less than or equal to the original clock enable rate (**Input data rate**).

### How to Specify the Clock Enable Rate

- 1 In the HDL Workflow Advisor, select **MATLAB to HDL Workflow > Code Generation**. Click the **Clocks & Ports** tab.
- 2 For the **Drive clock enable at** option, select **Input data rate** or **DUT base rate**.

<b>Drive clock enable at Option</b>	<b>Clock Enable Behavior</b>
<b>Input data rate</b> (default)	<p>Each assertion of the input clock enable produces an output clock enable assertion.</p> <p>You can assert the input clock enable at a maximum rate of once every N clocks. N = the upsampled clock rate / original clock rate.</p> <p>For example, if you see the message, “The design requires 4 times faster clock with respect to the base rate = 1”, your maximum input clock enable rate is once every 4 clocks.</p>
<b>DUT base rate</b>	<p>Input clock enable rate does not match the output clock enable rate. You must assert the input clock enable with your input data N times to get 1 output clock enable assertion. N = the upsampled clock rate / original clock rate.</p> <p>For example, if you see the message, “The design requires 4 times faster clock with respect to the base rate = 1”, you must assert the input clock enable 4 times to get 1 output clock enable assertion.</p>



## Test Bench Clock Enable Toggle Rate Specification

### In this section...

“When to Specify Test Bench Clock Enable Toggle Rate” on page 3-73

“How to Specify Test Bench Clock Enable Toggle Rate” on page 3-73

### When to Specify Test Bench Clock Enable Toggle Rate

When you want the test bench to drive your input data at a slower rate than the maximum input clock enable rate, specify the test bench clock enable toggle rate.

This specification can help you to achieve better test coverage, and to simulate the real world input data rate.

---

**Note** The maximum input clock enable rate is once every  $N$  clock cycles.  $N = \frac{\text{upsampled clock rate}}{\text{original clock rate}}$ . Refer to the clock enable behavior for **Input data rate**, in “Clock Enable Rate Specification” on page 3-71.

---

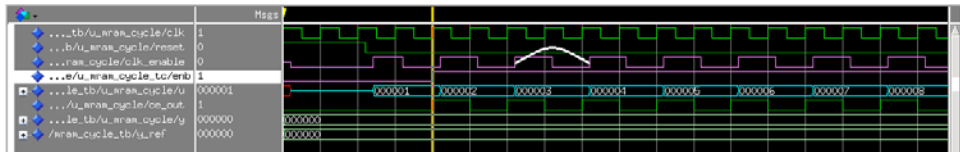
### How to Specify Test Bench Clock Enable Toggle Rate

To set your test bench clock enable toggle rate:

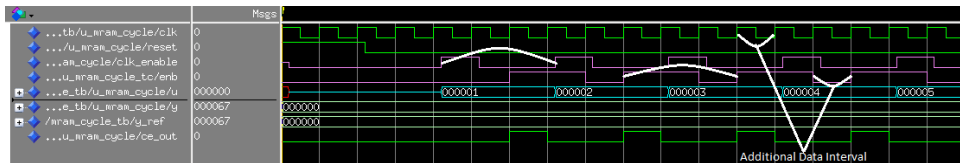
- 1** In the HDL Workflow Advisor, select **MATLAB to HDL Workflow > Code Generation**.
- 2** In the **Clocks & Ports** tab, for the **Drive clock enable at** option, select **Input data rate**.
- 3** In the **Test Bench** tab, for **Input data interval**, enter 0 or an integer greater than the maximum input clock enable interval.

Input data interval, I	Test Bench Clock Enable Behavior
$I = 0$ (default)	Asserts at the maximum input clock enable rate, or once every N cycles. N = the upsampled clock rate / original clock rate.
$I < N$	Not valid; generates an error.
$I = N$	Same as $I = 0$ .
$I > N$	Asserts every I clock cycles.

For example, this timing diagram shows clock enable behavior with **Input data interval** = 0. Here, the maximum input clock enable rate is once every 2 cycles.



The following timing diagram shows the same test bench and DUT with **Input data interval** = 3.



# Optimization

---

- “What Is RAM Mapping?” on page 4-2
- “Map Persistent Arrays and `dsp.Delay` to RAM” on page 4-3
- “RAM Mapping Comparison for MATLAB Code” on page 4-7
- “Pipelining” on page 4-8
- “Loop Optimization” on page 13-44
- “Optimize MATLAB Loops” on page 4-10

### What Is RAM Mapping?

RAM mapping is an area optimization that maps storage and delay elements in your MATLAB code to RAM. Without this optimization, storage and delay elements are mapped to registers. RAM mapping can therefore reduce the area of your design in the target hardware.

You can map the following MATLAB code elements to RAM:

- persistent array variable
- `dsp.Delay System` object
- `hdlram System` object

## Map Persistent Arrays and dsp.Delay to RAM

### In this section...

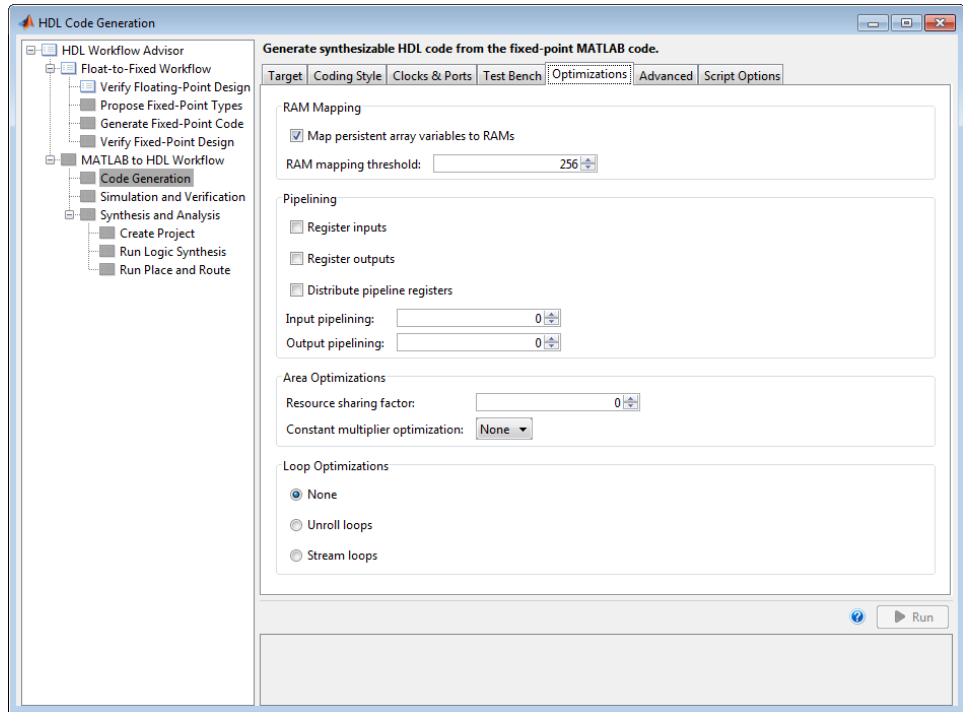
“How To Enable RAM Mapping” on page 4-3

“RAM Mapping Requirements for Persistent Arrays” on page 4-4

“RAM Mapping Requirements for dsp.Delay System Objects” on page 4-5

### How To Enable RAM Mapping

- 1** In the HDL Workflow Advisor, select **MATLAB to HDL Workflow > Code Generation > Optimizations** tab.
- 2** Select the **Map persistent array variables to RAMs** option.
- 3** Set the **RAM mapping threshold** to the size (in bits) of the smallest persistent array or `dsp.Delay` that you want to map to RAM.



## RAM Mapping Requirements for Persistent Arrays

A summary of the mapping behavior for persistent arrays is in the following table.

Map Persistent Array Variables to RAMs Setting	Mapping Behavior
on	<p>A persistent array maps to a block RAM when all of the following conditions are true:</p> <ul style="list-style-type: none"> <li>• Access to the array must be in unconditional code paths.</li> </ul>

<b>Map Persistent Array Variables to RAMs Setting</b>	<b>Mapping Behavior</b>
	<ul style="list-style-type: none"> <li>• Each read or write access is for a single element only. For example, submatrix access is not allowed.</li> <li>• Address computation logic is not read dependent. For example, computation of a read or write address using the data read from the array is not allowed.</li> <li>• RAMSize is greater than or equal to the <b>RAM Mapping Threshold</b> value. RAMSize is the product NumElements * WordLength * Complexity. <ul style="list-style-type: none"> <li>▪ NumElements is the number of elements in the array.</li> <li>▪ WordLength is the number of bits that represent the data type of the array.</li> <li>▪ Complexity is 2 for complex signals; 1 otherwise.</li> </ul> </li> </ul> <p>If any of the conditions are false, the persistent array maps to registers in the HDL code.</p>
off	Persistent arrays map to registers in the generated HDL code.

## RAM Mapping Requirements for dsp.Delay System Objects

A summary of the mapping behavior for a dsp.Delay System object is in the following table.

<b>Map Persistent Array Variables to RAMs Option</b>	<b>Mapping Behavior</b>
on	<p>A dsp.Delay System object maps to a block RAM when all of the following conditions are true:</p> <ul style="list-style-type: none"> <li>• Length property is greater than 4.</li> <li>• InitialConditions property is 0.</li> <li>• Delay input data type is one of the following: <ul style="list-style-type: none"> <li>▪ Real scalar with a non-floating-point data type.</li> <li>▪ Complex scalar with real and imaginary parts that are non-floating-point.</li> <li>▪ Vector where each element is either a non-floating-point real scalar or complex scalar.</li> </ul> </li> <li>• RAMSize is greater than or equal to the <b>RAM Mapping Threshold</b> value. <ul style="list-style-type: none"> <li>▪ RAMSize is the product Length * InputWordLength.</li> <li>▪ InputWordLength is the number of bits that represent the input data type.</li> </ul> </li> </ul> <p>If any of the conditions are false, the dsp.Delay System object maps to registers in the HDL code.</p>
off	<p>A dsp.Delay System object maps to registers in the generated HDL code.</p>



## RAM Mapping Comparison for MATLAB Code

`hdlram`, `dsp.Delay`, and persistent array variables can map to RAM, but have different attributes. The following table summarizes the differences.

Attribute	<code>hdlram</code>	<code>dsp.Delay</code>	Persistent Arrays
RAM mapping criteria	Unconditionally maps to RAM	Maps to RAM in HDL code under specific conditions. See “RAM Mapping Requirements for <code>dsp.Delay</code> System Objects” on page 4-5.	Maps to RAM in HDL code under specific conditions. See “RAM Mapping Requirements for Persistent Arrays” on page 4-4.
Address generation and port mapping	User specified	Automatic	Automatic
Access scheduling	User specified	Automatically inferred	Automatically inferred
Overclocking	None	None	Local multirate if access schedule requires it.
Latency with respect to simulation in MATLAB.	0	0	2 cycles if local multirate; 1 cycle otherwise.
RAM type	User specified	Dual port	Dual port

# Pipelining

Pipelining enables concurrency in the design by taking a longer, repetitively computed function and partitioning it into several local functions that perform an equivalent computation.

Pipelining increases system throughput by increasing the maximum clock rate, at the expense of increased chip area and increased initial latency. The time between accepting the first input and presenting the first output may be longer, but each additional output is presented at a higher rate.

For information on pipelining options, see “Code Generation: Optimizations Tab” on page 6-22.

## Loop Optimization

In this section...
“Loop Streaming” on page 13-44
“Loop Unrolling” on page 13-44

With loop optimization you can stream or unroll loops in generated code. Loop streaming optimizes for area; loop unrolling optimizes for speed.

### Loop Streaming

The coder streams a loop by instantiating the loop body once and using that instance for each loop iteration.

The advantage of loop streaming is decreased area because the loop body is instantiated only once. The disadvantage of loop streaming is lower speed.

### Loop Unrolling

The coder unrolls a loop by instantiating multiple instances of the loop body in the generated code.

The unrolled code can participate in distributed pipelining and resource sharing optimizations. Distributed pipelining can increase speed; resource sharing can decrease area.

Overall, however, the multiple instances created by loop unrolling are likely to increase area. Loop unrolling also makes the code less readable.

## Optimize MATLAB Loops

In this section...
“How to Optimize MATLAB Loops” on page 4-10
“Limitations for MATLAB Loop Optimization” on page 4-10

### How to Optimize MATLAB Loops

To select a loop optimization in the Workflow Advisor:

- 1 Open the Workflow Advisor.
- 2 In the left pane, select **MATLAB HDL Coder Workflow > MATLAB to HDL Workflow > Code Generation**.
- 3 Select the **Optimizations** tab.
- 4 For **Loop Optimizations**, select **None**, **Unroll Loops**, or **Stream Loops**.

### Limitations for MATLAB Loop Optimization

The coder cannot stream a loop if:

- The loop index counts down. The loop index must increase by 1 on each iteration.
- There are 2 or more nested loops at the same level of hierarchy within another loop.
- Any particular persistent variable is updated both inside and outside a loop.

The coder can stream a loop when the persistent variable is:

- Updated inside the loop and read outside the loop.
- Read within the loop and updated outside the loop.

# Speed and Area Optimization

---

## Distributed Pipelining for Clock Speed Optimization

This example shows how to use the distributed pipelining and loop unrolling optimizations in HDL Coder to optimize clock speed.

### Introduction

Distributed pipelining is a design-wide optimization supported by HDL Coder for improving clock frequency. When you turn on the 'Distribute Pipeline Registers' option in HDL Coder, the coder redistributes the input and output pipeline registers of the top level function along with other registers in the design in order to minimize the combinatorial logic between registers and thus maximize the clock speed of the chip synthesized from the generated HDL code.

Consider the following example design of a FIR filter. The combinatorial logic from an input or a register to an output or another register contains a sum of products. Loop unrolling and distributed pipelining moves the output registers at the design level to reduce the amount of combinatorial logic, thus increasing clock speed.

### MATLAB Design

The MATLAB code used in the example is a simple FIR filter. The example also shows a MATLAB test bench that exercises the filter.

```
design_name = 'mlhdlc_fir.m';  
testbench_name = 'mlhdlc_fir_tb.m';
```

**1** Design: mlhdlc\_fir

**2** Test Bench: mlhdlc\_fir\_tb

### Create a New Folder and Copy Relevant Files

Execute the following lines of code to copy the necessary example files into a temporary folder.

```
mlhdlc_demo_dir = fullfile(matlabroot, 'toolbox', 'hdlcoder', 'hdlcoderdemo');  
mlhdlc_temp_dir = [tempdir 'mlhdlc_fir'];
```

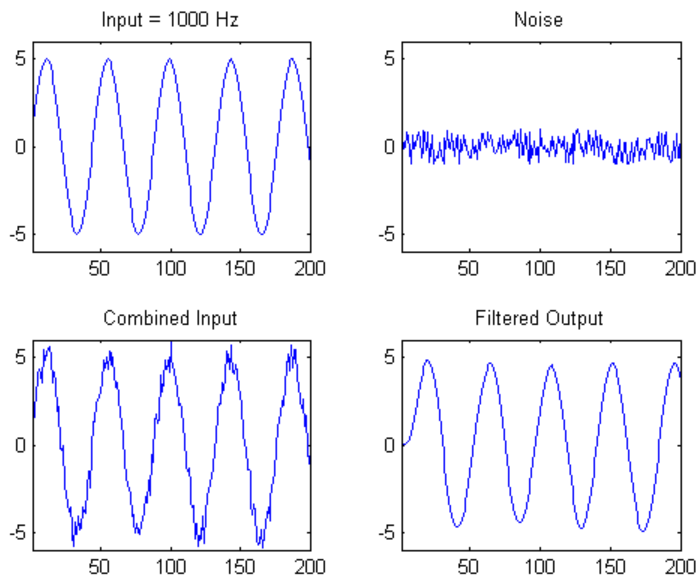
```
% create a temporary folder and copy the MATLAB files
cd(tempdir);
[~, ~, ~] = rmdir(mlhdlc_temp_dir, 's');
mkdir(mlhdlc_temp_dir);
cd(mlhdlc_temp_dir);

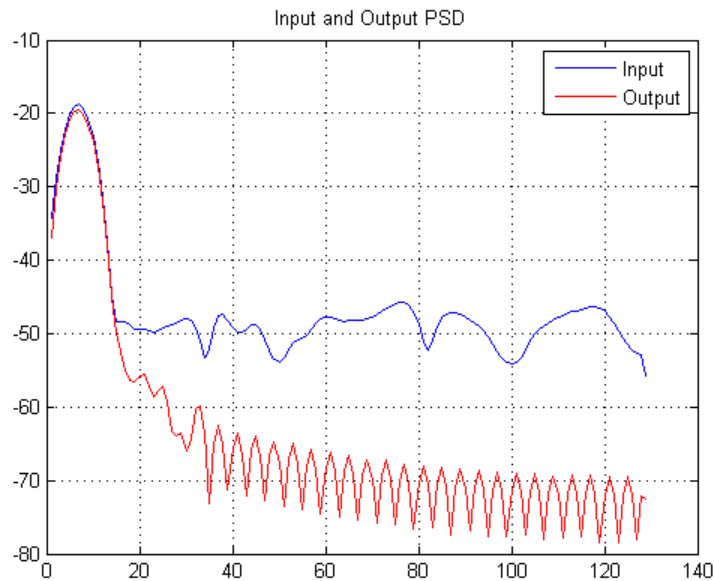
copyfile(fullfile(mlhdlc_demo_dir, design_name), mlhdlc_temp_dir);
copyfile(fullfile(mlhdlc_demo_dir, testbench_name), mlhdlc_temp_dir);
```

### Simulate the Design

Simulate the design with the testbench prior to code generation to make sure there are no run-time errors.

```
mlhdlc_fir_tb
```





### Create a New Project From the Command Line

```
coder -hdlcoder -new fir_project
```

Next, add the file 'mlhdlc\_fir.m' to the project as the MATLAB Function and 'mlhdlc\_fir\_tb.m' as the MATLAB Test Bench.

You can refer to Getting Started with MATLAB to HDL Workflow tutorial for a more complete tutorial on creating and populating MATLAB HDL Coder projects.

### Distributed Pipelining

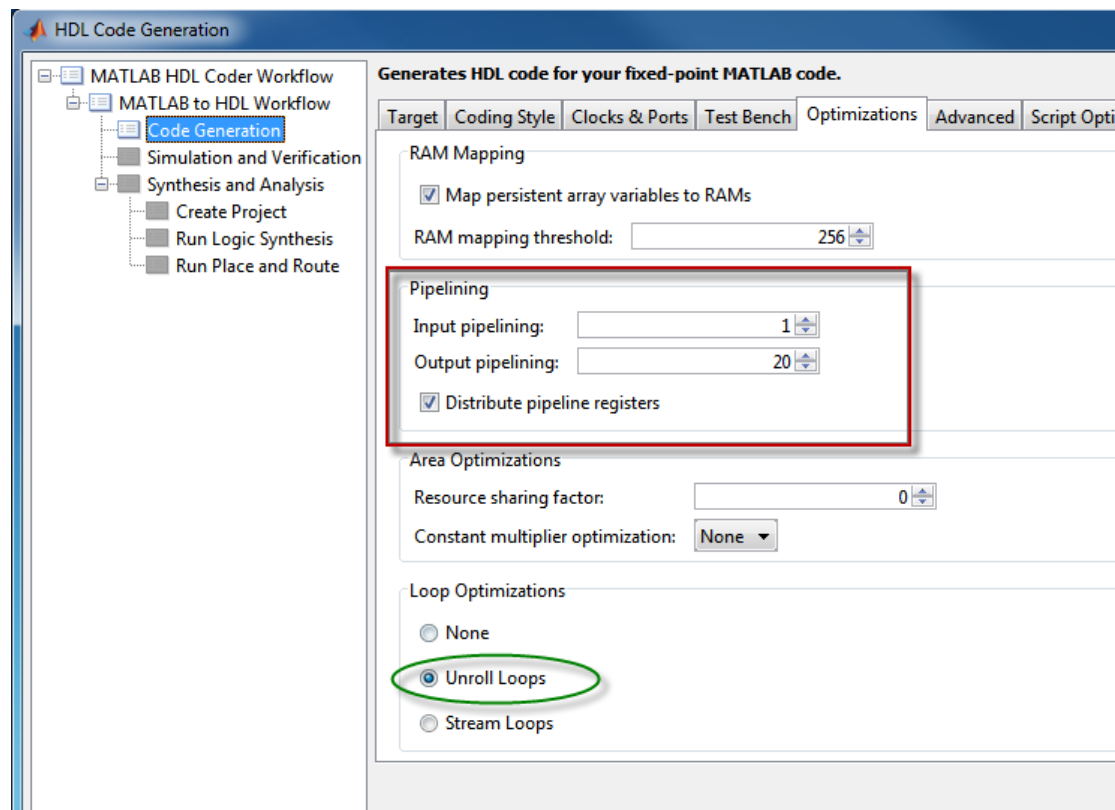
To increase the clock speed, the user can set a number of input and output pipeline stages for any design. In this particular example Input pipelining option is set to '1' and Output pipelining option is set to '20'. Without any additional options turned on these settings will add one input pipeline register at all input ports of the top level design and 20 output pipeline registers at each of the output ports.



If the option 'Distribute pipeline registers' is enabled, HDL Coder tries to reposition the registers to achieve the best clock frequency.

In addition to moving the input and output pipeline registers, HDL Coder also tries to move the registers modeled internally in the design using persistent variables or with system objects like `dsp.Delay`.

Additional opportunities for improvements become available if you unroll loops. The 'Unroll Loops' option unrolls explicit for-loops in MATLAB code in addition to implicit for-loops that are inferred for vector and matrix operations.

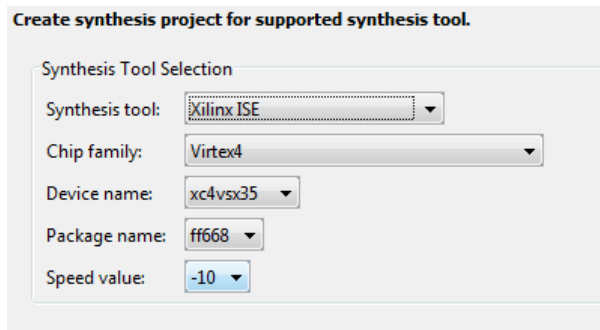


### Run Fixed-Point Conversion and HDL Code Generation

Launch the Workflow Advisor and right click on the 'Code Generation' step. Choose the option 'Run to selected task' to run all the steps from the beginning through the HDL code generation.

### Examine the Synthesis Results

Run the logic synthesis step with the following default options if you have ISE installed on your machine.



**Create synthesis project for supported synthesis tool.**

Synthesis Tool Selection

Synthesis tool: Xilinx ISE

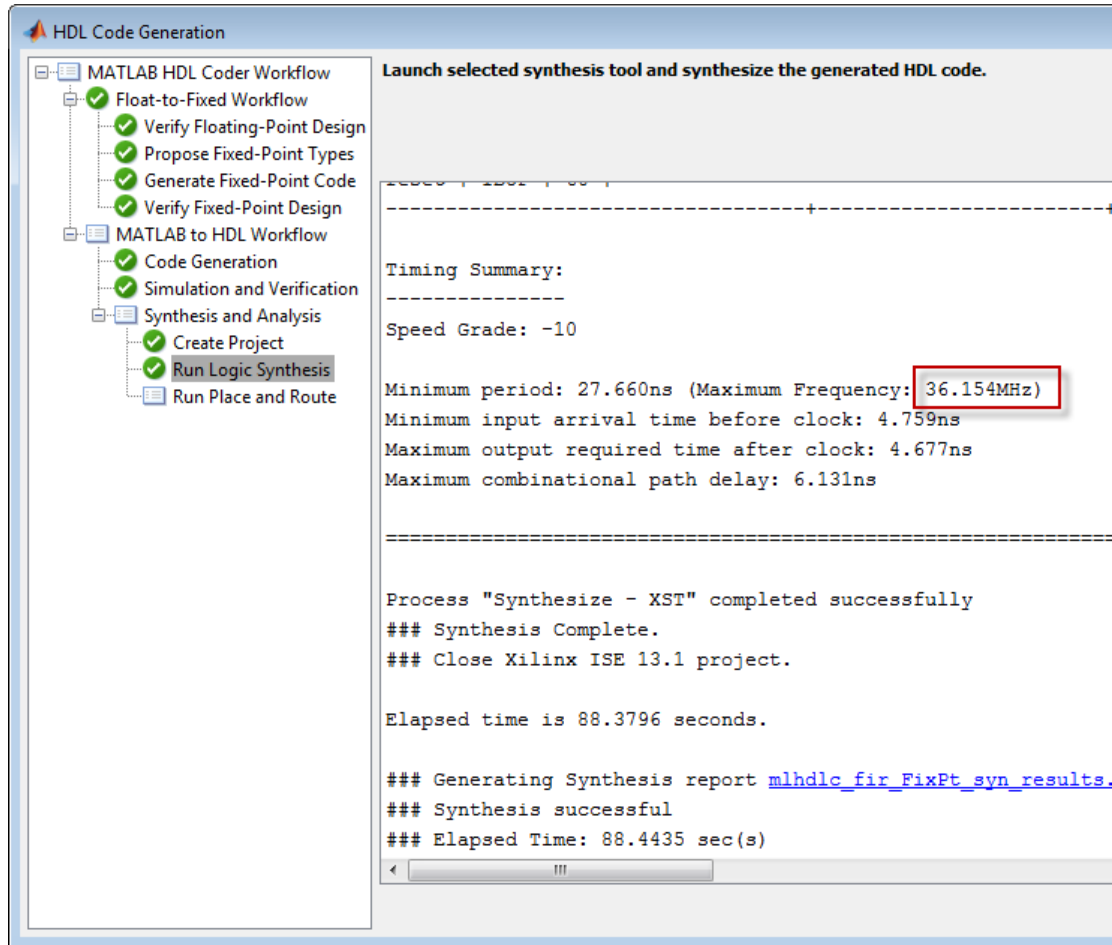
Chip family: Virtex4

Device name: xc4vsx35

Package name: ff668

Speed value: -10

In the synthesis report, note the clock frequency reported by the synthesis tool without any optimization options enabled.



**HDL Code Generation**

- MATLAB HDL Coder Workflow
  - Float-to-Fixed Workflow
    - Verify Floating-Point Design
    - Propose Fixed-Point Types
    - Generate Fixed-Point Code
    - Verify Fixed-Point Design
  - MATLAB to HDL Workflow
    - Code Generation
    - Simulation and Verification
  - Synthesis and Analysis
    - Create Project
    - Run Logic Synthesis
    - Run Place and Route

**Launch selected synthesis tool and synthesize the generated HDL code.**

Timing Summary:

Speed Grade: -10

Minimum period: 27.660ns (Maximum Frequency: 36.154MHz)

Minimum input arrival time before clock: 4.759ns

Maximum output required time after clock: 4.677ns

Maximum combinational path delay: 6.131ns

=====  
Process "Synthesize - XST" completed successfully  
### Synthesis Complete.  
### Close Xilinx ISE 13.1 project.

Elapsed time is 88.3796 seconds.

### Generating Synthesis report [mlhdlc\\_fir\\_FixPt\\_syn\\_results](#).  
### Synthesis successful  
### Elapsed Time: 88.4435 sec(s)

When you synthesize the design with the loop unrolling and distributed pipelining options enabled, you see a significant clock frequency increase with pipelining options turned on.

The screenshot shows the HDL Code Generation tool interface. On the left, a tree view under 'MATLAB HDL Coder Workflow' shows the following steps: Float-to-Fixed Workflow (checked), Verify Floating-Point Design (checked), Propose Fixed-Point Types (checked), Generate Fixed-Point Code (checked), Verify Fixed-Point Design (checked), MATLAB to HDL Workflow (checked), Code Generation (checked), Simulation and Verification (checked), Synthesis and Analysis (checked), Create Project (checked), Run Logic Synthesis (highlighted in blue), and Run Place and Route. On the right, a terminal window displays the following text:

```

Launch selected synthesis tool and synthesize the generated HDL code.

-----
Timing Summary:
-----
Speed Grade: -10

Minimum period: 7.243ns (Maximum Frequency: 138.058MHz)
Minimum input arrival time before clock: 7.867ns
Maximum output required time after clock: 4.677ns
Maximum combinational path delay: 7.594ns

=====

Process "Synthesize - XST" completed successfully
### Synthesis Complete.
### Close Xilinx ISE 13.1 project.

Elapsed time is 180.4699 seconds.

### Generating Synthesis report mlhdlc_fir_FixPt_syn_results.
### Synthesis successful
### Elapsed Time: 180.5247 sec(s)

```

### Clean Up the Generated Files

Run the following commands to clean up the temporary project folder.

```

mlhdlc_demo_dir = fullfile(matlabroot, 'toolbox', 'hdlcoder', 'hdlcoderdemo');
mlhdlc_temp_dir = [tempdir 'mlhdlc_fir'];
clear mex;
cd (mlhdlc_demo_dir);

```

```
rmdir(mlhdlc_temp_dir, 's');
```

# Map Matrices to Block RAMs to Reduce Area

This example shows how to use the RAM mapping optimization in HDL Coder™ to map persistent matrix variables to block RAMs in hardware.

## Introduction

One of the attractive features of writing MATLAB code is the ease of creating, accessing, modifying and manipulating matrices in MATLAB.

When processing such MATLAB code, HDL Coder maps these matrices to wires or registers in HDL. For example, local temporary matrix variables are mapped to wires, whereas persistent matrix variables are mapped to registers.

The latter tends to be an inefficient mapping when the matrix size is large, since the number of register resources available is limited. It also complicates synthesis, placement and routing.

Modern FPGAs feature block RAMs that are designed to have large matrices. HDL Coder takes advantage of this feature and automatically maps matrices to block RAMs to improve area efficiency. For certain designs, mapping these persistent matrices to RAMs is mandatory if the design is to be realized. State-of-the-art synthesis tools may not be able to synthesize designs when large matrices are mapped to registers, whereas the problem size is more manageable when the same matrices are mapped to RAMs.

## MATLAB Design

```
design_name = 'mlhdlc_sobel.m';  
testbench_name = 'mlhdlc_sobel_tb.m';
```

- MATLAB Design: mlhdlc\_sobel
- MATLAB Testbench: mlhdlc\_sobel\_tb
- Input Image: stop\_sign

## Create a New Folder and Copy Relevant Files

Execute the following lines of code to copy the example files into a temporary folder.

```

mlhdlc_demo_dir = fullfile(matlabroot, 'toolbox', 'hdlcoder', 'hdlcoderdemo');
mlhdlc_temp_dir = [tempdir 'mlhdlc_sobel'];

% create a temporary folder and copy the MATLAB files
cd(tempdir);
[~, ~, ~] = rmdir(mlhdlc_temp_dir, 's');
mkdir(mlhdlc_temp_dir);
cd(mlhdlc_temp_dir);

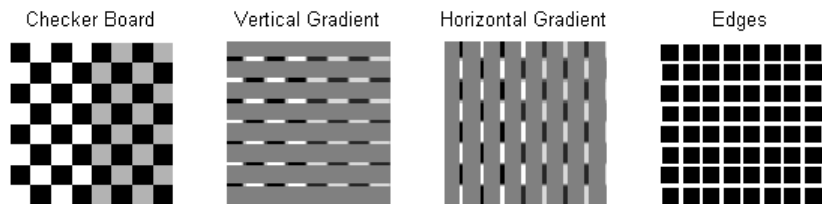
% copy the design files to the temporary directory
copyfile(fullfile(mlhdlc_demo_dir, design_name), mlhdlc_temp_dir);
copyfile(fullfile(mlhdlc_demo_dir, testbench_name), mlhdlc_temp_dir);

```

### Simulate the Design

Simulate the design with the test bench prior to code generation to make sure there are no runtime errors.

```
mlhdlc_sobel_tb
```



### Create a New HDL Coder™ Project

Run the following command to create a new project.

```
coder -hdlcoder -new mlhdlc_ram
```

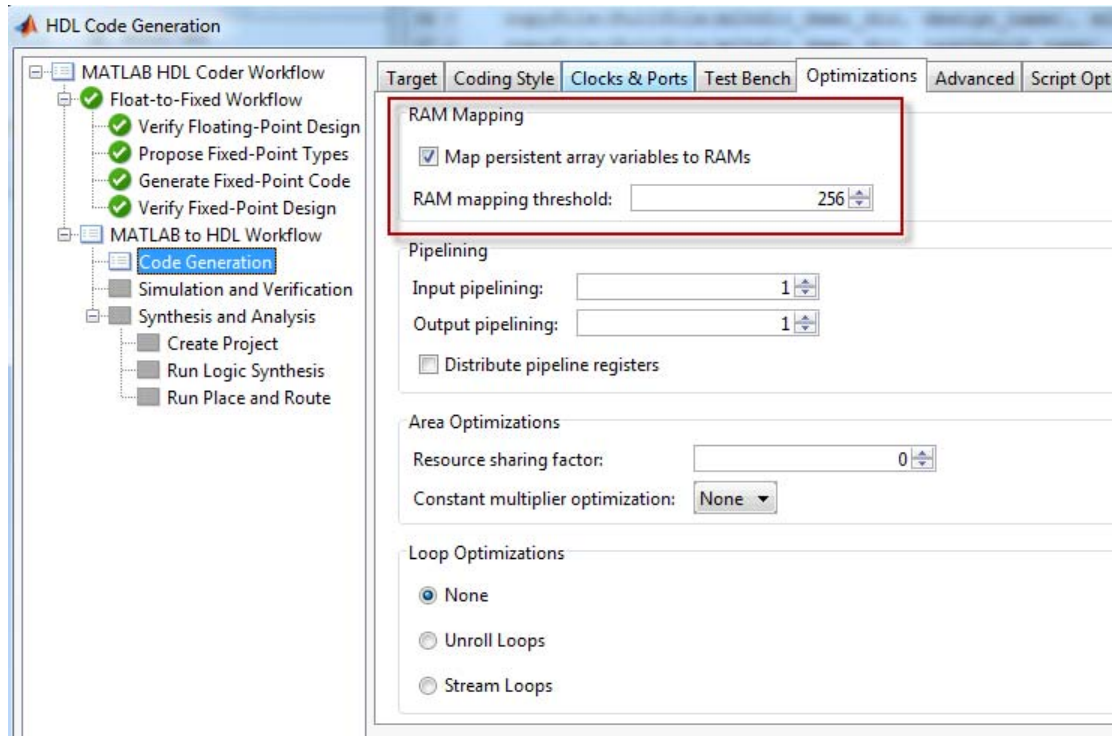
Next, add the file 'mlhdlc\_sobel.m' to the project as the MATLAB function, and 'mlhdlc\_sobel\_tb.m' as the MATLAB test bench.

You can refer to Getting Started with MATLAB to HDL Workflow tutorial for a more complete tutorial on creating and populating MATLAB HDL Coder projects.

### Turn On the RAM Mapping Optimization

Launch the Workflow Advisor.

The checkbox 'Map persistent array variables to RAMs' needs to be turned on to map persistent variables to block RAMs in the generated code.



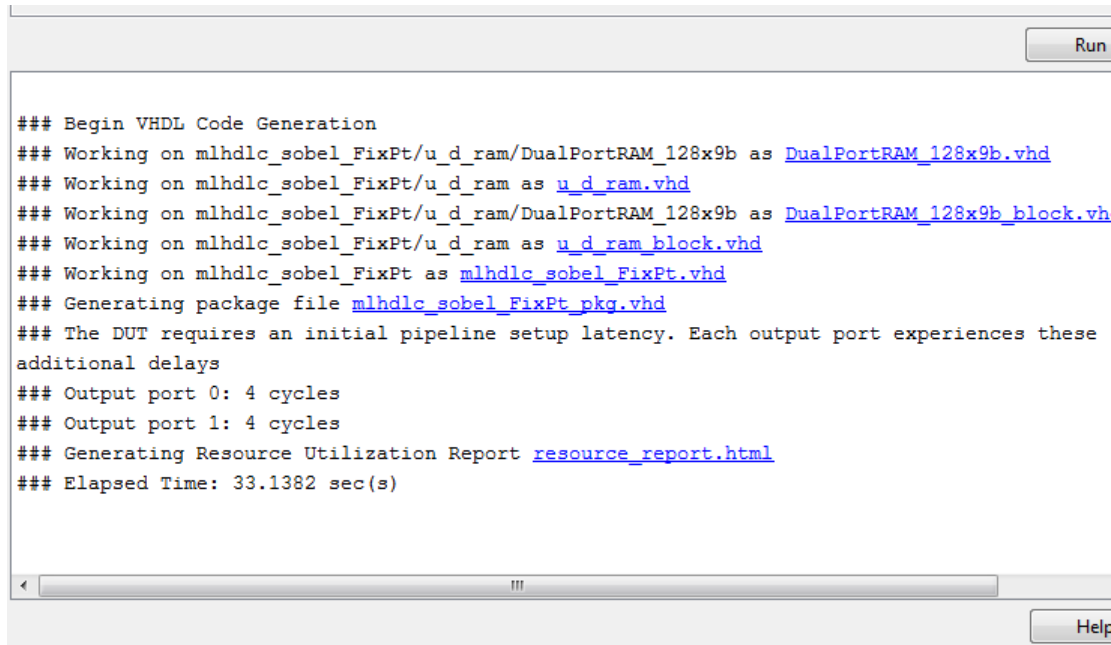
### Run Fixed-Point Conversion and HDL Code Generation



In the Workflow Advisor, right-click the 'Code Generation' step. Choose the option 'Run to selected task' to run all the steps from the beginning through HDL code generation.

### Examine the Generated Code

Examine the messages in the log window to see the RAM files generated along with the design.



```

### Begin VHDL Code Generation
### Working on mlhdlc_sobel_FixPt/u_d_ram/DualPortRAM_128x9b as DualPortRAM\_128x9b.vhd
### Working on mlhdlc_sobel_FixPt/u_d_ram as u\_d\_ram.vhd
### Working on mlhdlc_sobel_FixPt/u_d_ram/DualPortRAM_128x9b as DualPortRAM\_128x9b\_block.vh
### Working on mlhdlc_sobel_FixPt/u_d_ram as u\_d\_ram\_block.vhd
### Working on mlhdlc_sobel_FixPt as mlhdlc\_sobel\_FixPt.vhd
### Generating package file mlhdlc\_sobel\_FixPt\_pkg.vhd
### The DUT requires an initial pipeline setup latency. Each output port experiences these
additional delays
### Output port 0: 4 cycles
### Output port 1: 4 cycles
### Generating Resource Utilization Report resource\_report.html
### Elapsed Time: 33.1382 sec(s)

```

A warning message appears for each persistent matrix variable not mapped to RAM.

### Examine the Resource Report

Take a look at the generated resource report, which shows the number of RAMs inferred, by following the 'Resource Utilization report...' link in the generated code window.

Multipliers	0
Adders/Subtractors	19
Registers	29
RAMs	2
Multiplexers	5

### Additional Notes on RAM Mapping

- Persistent matrix variable accesses must be in unconditional regions, i.e., outside any if-else, switch case, or for-loop code.
- MATLAB functions can have any number of RAM matrices.
- All matrix variables in MATLAB that are declared persistent and meet the threshold criteria get mapped to RAMs.
- A warning is shown when a persistent matrix does not get mapped to RAM.
- Read-dependent write data cycles are not allowed: you cannot compute the write data as a function of the data read from the matrix.
- Persistent matrices cannot be copied as a whole or accessed as a sub matrix: matrix access (read/write) is allowed only on single elements of the matrix.
- Mapping persistent matrices with non-zero initial values to RAMs is not supported.

### Clean up the Generated Files

Run the following commands to clean up the temporary project folder.

```
mlhdlc_demo_dir = fullfile(matlabroot, 'toolbox', 'hdlcoder', 'hdlcoderdemo');
mlhdlc_temp_dir = [tempdir 'mlhdlc_sobel'];
clear mex;
cd (mlhdlc_demo_dir);
rmdir(mlhdlc_temp_dir, 's');
```

## Resource Sharing of Multipliers to Reduce Area

This example shows how to use the resource sharing optimization in HDL Coder™. This optimization identifies functionally equivalent multiplier operations in MATLAB code and shares them in order to optimize design area. You have control over the number of multipliers to be shared in the design.

### Introduction

Resource sharing is a design-wide optimization supported by HDL Coder™ for implementing area-efficient hardware.

This optimization enables users to share hardware resources by mapping 'N' functionally-equivalent MATLAB operators, in this case multipliers, to a single operator.

The user specifies 'N' using the 'Resource Sharing Factor' option in the optimization panel.

Consider the following example model of a symmetric FIR filter. It contains 4 product blocks that are functionally equivalent and which are mapped to 4 multipliers in hardware. The Resource Utilization Report shows the number of multipliers inferred from the design.

### MATLAB Design

The MATLAB code used in the example is a simple symmetric FIR filter written in MATLAB and also has a testbench that exercises the filter.

```
design_name = 'mlhdlc_sharing.m';
testbench_name = 'mlhdlc_sharing_tb.m';
```

Let us take a look at the MATLAB design.

```
type(design_name);
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% MATLAB design: Symmetric FIR Filter
%
```

```
% Key Design pattern covered in this example:
% (1) Filter states represented using the persistent variables
% (2) Filter coefficients passed in as parameters
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Copyright 2011 The MathWorks, Inc.

%#codegen
function [y_out, x_out] = mlhdlc_sharing(x_in, h)
% Symmetric FIR Filter

persistent ud1 ud2 ud3 ud4 ud5 ud6 ud7 ud8;
if isempty(ud1)
    ud1 = 0; ud2 = 0; ud3 = 0; ud4 = 0; ud5 = 0; ud6 = 0; ud7 = 0; ud8 = 0;
end

x_out = ud8;

a1 = ud1 + ud8;
a2 = ud2 + ud7;
a3 = ud3 + ud6;
a4 = ud4 + ud5;

% filtered output
y_out = (h(1) * a1 + h(2) * a2) + (h(3) * a3 + h(4) * a4);

% update the delay line
ud8 = ud7;
ud7 = ud6;
ud6 = ud5;
ud5 = ud4;
ud4 = ud3;
ud3 = ud2;
ud2 = ud1;
ud1 = x_in;

end
```

```

type(testbench_name);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% MATLAB test bench for the FIR filter
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Copyright 2011 The MathWorks, Inc.

clear mlhdlc_sharing;

% input signal with noise
x_in = cos(3.*pi.*(0:0.001:2).*(1+(0:0.001:2).*75)).';

len = length(x_in);
y_out = zeros(1,len);
x_out = zeros(1,len);

% Define a regular MATLAB constant array:
%
% filter coefficients
h = [-0.1339 -0.0838 0.2026 0.4064];

for ii=1:len
    data = x_in(ii);
    % call to the design 'mlhdlc_sfir' that is targeted for hardware
    [y_out(ii), x_out(ii)] = mlhdlc_sharing(data, h);
end

figure('Name', [mfilename, '_plot']);
plot(1:len,y_out);

```

### Create a New Folder and Copy Relevant Files

Execute the following lines of code to copy the necessary example files into a temporary folder.

```

mlhdlc_demo_dir = fullfile(matlabroot, 'toolbox', 'hdlcoder', 'hdlcoderdemo');
mlhdlc_temp_dir = [tempdir 'mlhdlc_sfir_sharing'];

```

```
% create a temporary folder and copy the MATLAB files
cd(tempdir);
[~, ~, ~] = rmdir(mlhdlc_temp_dir, 's');
mkdir(mlhdlc_temp_dir);
cd(mlhdlc_temp_dir);

copyfile(fullfile(mlhdlc_demo_dir, design_name), mlhdlc_temp_dir);
copyfile(fullfile(mlhdlc_demo_dir, testbench_name), mlhdlc_temp_dir);
```

### **Create a New HDL Coder Project**

Run the following command to create a new project:

```
coder -hdlcoder -new mlhdlc_sfir_sharing
```

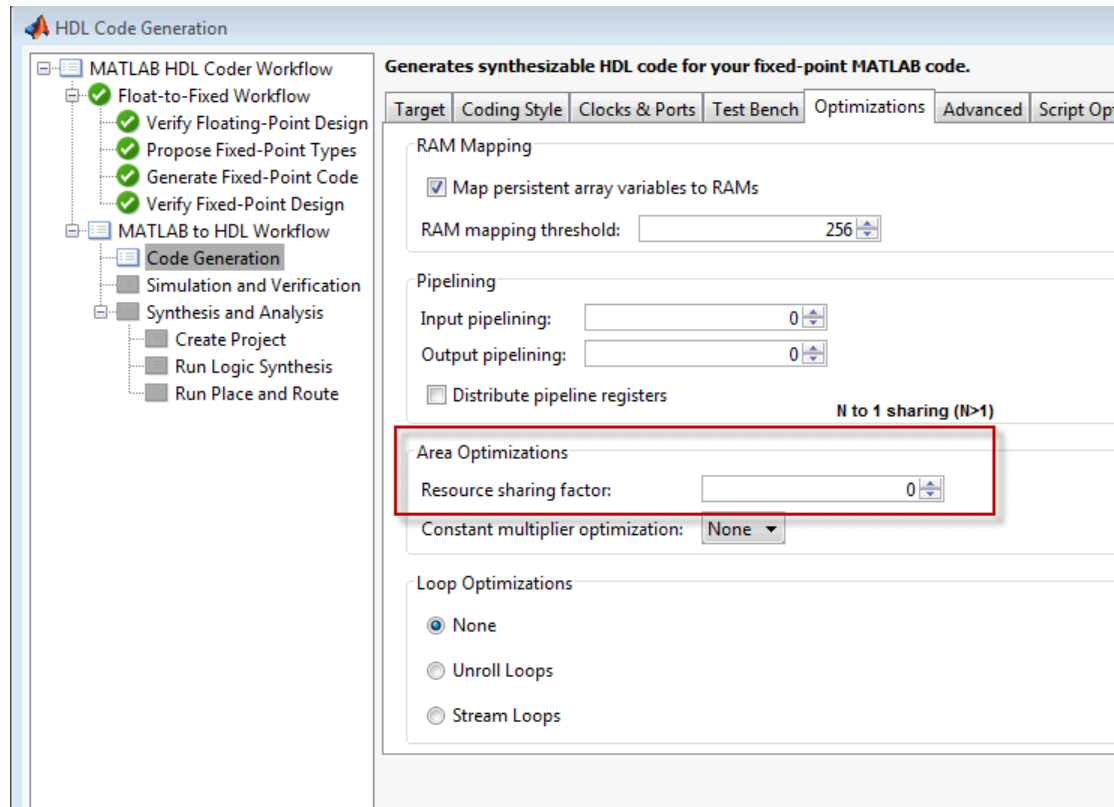
Next, add the file 'mlhdlc\_sharing.m' to the project as the MATLAB Function and 'mlhdlc\_sharing\_tb.m' as the MATLAB Test Bench.

You can refer to Getting Started with MATLAB to HDL Workflow tutorial for a more complete tutorial on creating and populating MATLAB HDL Coder projects.

### **Realize an N-to-1 Mapping of Multipliers**

Turn on the resource sharing optimization by setting the 'Resource Sharing Factor' to a positive integer value.

This parameter specifies 'N' in the N-to-1 hardware mapping. Choose a value of  $N > 1$ .



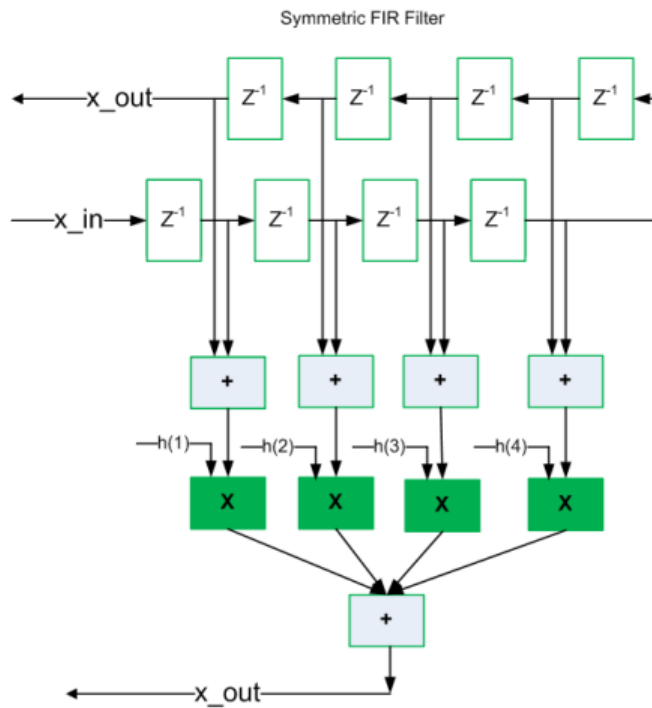
### Examine the Resource Report

There are 4 multiplication operators in this example design. Generating HDL with a 'SharingFactor' of 4 will result in only one multiplier in the generated code.

Multipliers	1
Adders/Subtractors	7
Registers	29
RAMs	0
Multiplexers	12

**Sharing Architecture**

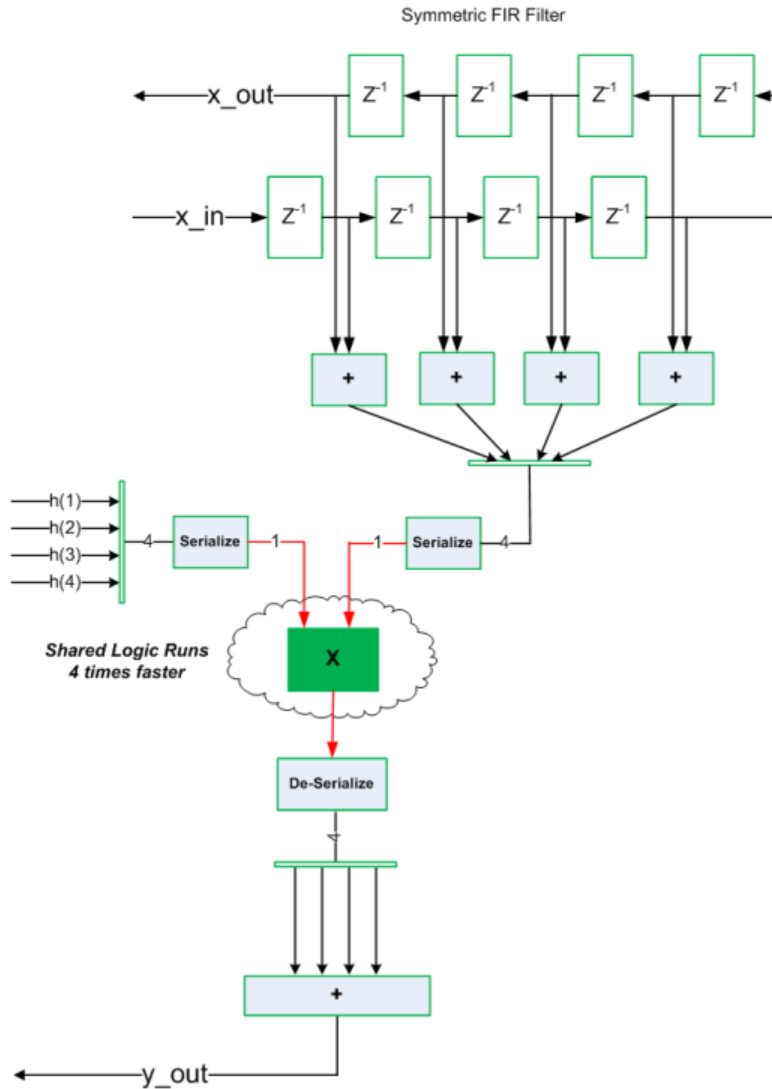
The following figure shows how the algorithm is implemented in hardware when we synthesize the generated code without turning on the sharing optimization.





The following figure shows the sharing architecture automatically implemented by HDL Coder when the sharing optimization option is turned on.

The inputs to the shared multiplier are time-multiplexed at a faster rate (in this case 4x faster and denoted in red). The outputs are then routed to the respective consumers at a slower rate (in green).



**Run Fixed-Point Conversion and HDL Code Generation**

Launch the Workflow Advisor and right-click the 'Code Generation' step. Choose the option 'Run to selected task' to run all the steps from the beginning through the HDL code generation.

### **Run Synthesis and Examine Synthesis Results**

Synthesize the generated code from the design with this optimization turned off, then with it turned on, and examine the area numbers in the resource report.

### **Known Limitations**

Sharing two or more multipliers requires that operands of all the multipliers match exactly in terms of numeric type, size, and complexity.

### **Clean up the Generated Files**

Run the following commands to clean up the temporary project folder.

```
mlhdlc_demo_dir = fullfile(matlabroot, 'toolbox', 'hdlcoder', 'hdlcoderdemo');
mlhdlc_temp_dir = [tempdir 'mlhdlc_sfir_sharing'];
clear mex;
cd (mlhdlc_demo_dir);
rmdir(mlhdlc_temp_dir, 's');
```

## Loop Streaming to Reduce Area

This example shows how to use the design-level loop streaming optimization in HDL Coder™ to optimize area.

### Introduction

A MATLAB for loop generates a FOR\_GENERATE loop in VHDL. Such loops are always spatially unrolled for execution in hardware. In other words, the body of the software loop is replicated as many times in hardware as the number of loop iterations. This results in inefficient area usage.

The loop streaming optimization creates an alternative implementation of a software loop, where the body of the loop is shared in hardware. Instead of spatially replicating copies of the loop body, HDL Coder™ creates a single hardware instance of the loop body that is time-multiplexed across loop iterations.

### MATLAB Design

The MATLAB code used in this example implements a simple FIR filter. This example also shows a MATLAB testbench that exercises the filter.

```
design_name = 'mlhdlc_fir.m';  
testbench_name = 'mlhdlc_fir_tb.m';
```

**1** Design: mlhdlc\_fir

**2** Test Bench: mlhdlc\_fir\_tb

### Create a New Folder and Copy Relevant Files

Execute the following lines of code to copy the necessary example files into a temporary folder.

```
mlhdlc_demo_dir = fullfile(matlabroot, 'toolbox', 'hdlcoder', 'hdlcoderdemo');  
mlhdlc_temp_dir = [tempdir 'mlhdlc_fir'];  
  
% create a temporary folder and copy the MATLAB files  
cd(tempdir);  
[~, ~, ~] = rmdir(mlhdlc_temp_dir, 's');
```

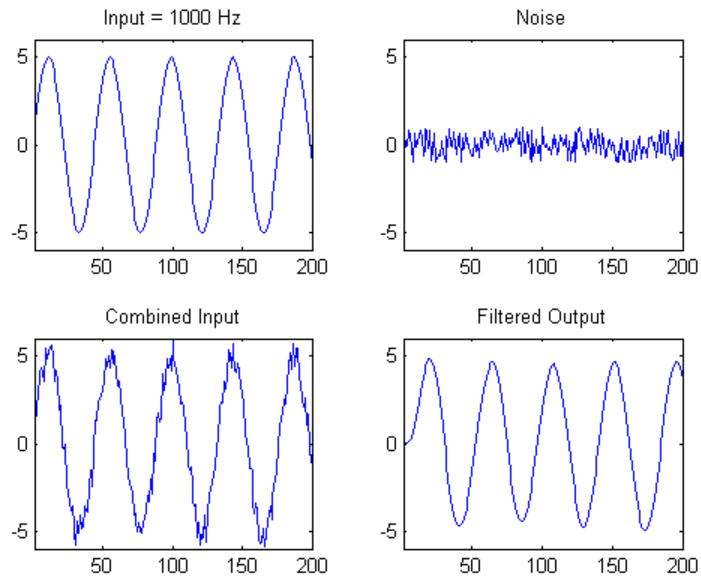
```
mkdir(mlhdlc_temp_dir);  
cd(mlhdlc_temp_dir);
```

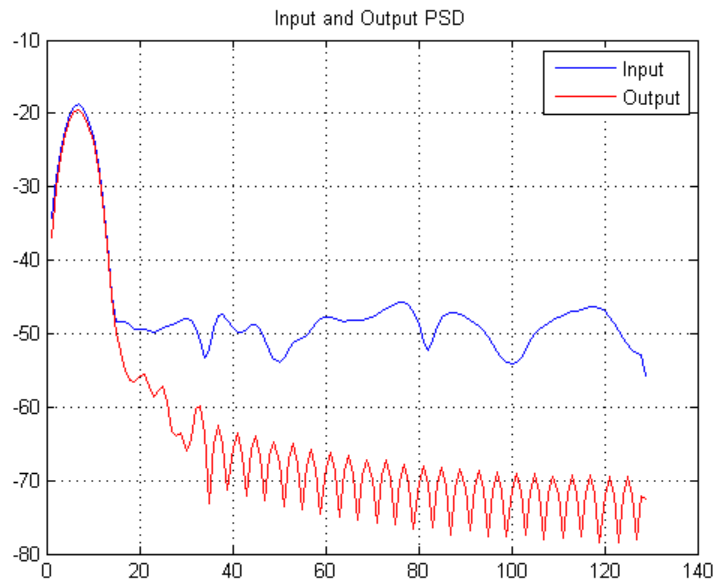
```
copyfile(fullfile(mlhdlc_demo_dir, design_name), mlhdlc_temp_dir);  
copyfile(fullfile(mlhdlc_demo_dir, testbench_name), mlhdlc_temp_dir);
```

### Simulate the Design

Simulate the design with the testbench prior to code generation to make sure there are no runtime errors.

```
mlhdlc_fir_tb
```





### Creating a New Project From the Command Line

To create a new project, enter the following command:

```
coder -hdlcoder -new fir_project
```

Next, add the file 'mlhdlc\_fir.m' to the project as the MATLAB Function and 'mlhdlc\_fir\_tb.m' as the MATLAB Test Bench.

Launch the Workflow Advisor.

You can refer to Getting Started with MATLAB to HDL Workflow tutorial for a more complete tutorial on creating and populating MATLAB HDL Coder projects.

### Turn On Loop Streaming

The loop streaming optimization in HDL Coder converts software loops (either written explicitly using a for-loop statement, or inferred loops from matrix/vector operators) to area-friendly hardware loops.

The screenshot displays the HDL Code Generation tool interface. On the left, a tree view shows the workflow steps, with 'Code Generation' selected under 'MATLAB to HDL Workflow'. The main panel, titled 'Generates synthesizable HDL code for your fixed-point MATLAB code.', contains several optimization tabs: Target, Coding Style, Clocks & Ports, Test Bench, Optimizations, Advanced, and Script Op. The 'Optimizations' tab is active, showing settings for RAM Mapping, Pipelining, Area Optimizations, and Loop Optimizations. The 'Loop Optimizations' section is highlighted with a red rectangle, and the 'Stream Loops' radio button is selected and circled in green.

**HDL Code Generation**

MATLAB HDL Coder Workflow

- Float-to-Fixed Workflow
  - Verify Floating-Point Design
  - Propose Fixed-Point Types
  - Generate Fixed-Point Code
  - Verify Fixed-Point Design
- MATLAB to HDL Workflow
  - Code Generation**
  - Simulation and Verification
  - Synthesis and Analysis
    - Create Project
    - Run Logic Synthesis
    - Run Place and Route

**Generates synthesizable HDL code for your fixed-point MATLAB code.**

Target | Coding Style | Clocks & Ports | Test Bench | **Optimizations** | Advanced | Script Op

**RAM Mapping**

- Map persistent array variables to RAMs
- RAM mapping threshold:

**Pipelining**

- Input pipelining:
- Output pipelining:
- Distribute pipeline registers

**Area Optimizations**

- Resource sharing factor:
- Constant multiplier optimization: **None**

**Loop Optimizations**

- None
- Unroll Loops
- Stream Loops

### Run Fixed-Point Conversion and HDL Code Generation

Right-click the 'Code Generation' step. Choose the option 'Run to selected task' to run all the steps from the beginning through HDL code generation.

### Examine the Generated Code

When you synthesize the design with the loop streaming optimization, you see a reduction in area resources in the resource report. Try generating HDL code with and without the optimization.

The resource report without the loop streaming optimization:

Multipliers	16
Adders/Subtractors	31
Registers	106
RAMs	0
Multiplexers	0

The resource report with the loop streaming optimization enabled:

Multipliers	1
Adders/Subtractors	17
Registers	448
RAMs	0
Multiplexers	5

### Known Limitations

Loops will be streamed only if they are regular nested loops. A regular nested loop structure is defined as one where:



- None of the loops in any level of nesting appear in a conditional flow region, i.e. no loop can be embedded within if-else or switch-else regions.
- Loop index variables are monotonically increasing.
- Total number of iterations of the loop structure is non-zero.
- There are no back-to-back loops at the same level of the nesting hierarchy.

### **Clean up the Generated Files**

Run the following commands to clean up the temporary project folder.

```
mlhdlc_demo_dir = fullfile(matlabroot, 'toolbox', 'hdlcoder', 'hdlcoderdemo');
mlhdlc_temp_dir = [tempdir 'mlhdlc_fir'];
clear mex;
cd (mlhdlc_demo_dir);
rmdir(mlhdlc_temp_dir, 's');
```

## Constant Multiplier Optimization to Reduce Area

This example shows how to perform a design-level area optimization in HDL Coder by converting constant multipliers into shifts and adds using canonical signed digit (CSD) techniques.

### Introduction

This tutorial shows how the use of canonical signed digit (CSD) representation of multiplier constants (for example, in gain coefficients or filter coefficients) can significantly reduce the area of the hardware implementation.

### Canonical Signed Digit (CSD) Representation

A signed digit (SD) representation is an augmented binary representation with weights 0, 1 and -1.

$$X_{10} = \sum_{r=0}^{B-1} x_r \cdot 2^r$$

where

$$x_r = 0, 1, -1(\bar{1})$$

For example, here are a couple of signed digit representations for 93:

$$X_{10} = 64 + 16 + 13 = 01011101$$

$$X_{10} = 128 - 32 - 2 - 1 = 10\bar{1}000\bar{1}\bar{1}$$

Note that the signed digit representation is non-unique. A canonical signed digit (CSD) representation is an SD representation with the minimum number of non-zero elements.

Here are some properties of CSD numbers:

- 1 No two consecutive bits in a CSD number are non-zero
- 2 CSD representation is guaranteed to have minimum number of non-zero bits

### 3 CSD representation of a number is unique

#### CSD Multiplier

Let us see how a CSD representation can yield an implementation requiring a minimum number of adders.

Let us look at CSD example:

$$\begin{aligned}
 y &= 231 * x \\
 &= (11100111) * x && \% 231 \text{ in binary form} \\
 &= (1001'01001') * x && \% 231 \text{ in signed digit form} \\
 &= (256 - 32 + 8 - 1) * x && \% \\
 &= (x \ll 8) - (x \ll 5) + (x \ll 3) - x && \% \text{ cost of CSD: 3 Adders}
 \end{aligned}$$

#### FCSD Multiplier

A combination of factorization and CSD representation of a constant multiplier can lead to further reduction in hardware cost (number of adders).

FCSD can further reduce the number of adders in the above constant multiplier:

$$\begin{aligned}
 y &= 231 * x \\
 &= (7 * 33) * x \\
 &= (x \ll 8 - x) * (x \ll 5 + x) && \% \text{ cost of FCSD: 2 Adders}
 \end{aligned}$$

#### CSD/FCSD Costs

This table shows the costs (C) of all 8-bit multipliers.

$C$	Coefficient
0	1, 2, 4, 8, 16, 32, 64, 128, 256
1	3, 5, 6, 7, 9, 10, 12, 14, 15, 17, 18, 20, 24, 28, 30, 31, 33, 34, 36, 40, 48, 49, 50, 52, 54, 55, 57, 58, 59, 61, 67, 69, 70, 71, 73, 74, 76, 78, 80, 82, 84, 88, 92, 94, 95, 97, 98, 100, 104, 108, 110, 111, 113, 114, 116, 118, 119, 121, 122, 123, 125, 131, 133, 134, 135, 137, 138, 140, 142, 143, 144, 146, 148, 152, 156, 158, 159, 161, 162, 164, 168, 176, 184, 188, 190, 192, 193, 194, 196, 200, 208, 216, 220, 222, 223, 225, 226, 228, 232, 236, 238, 239, 241, 242, 244, 246, 247, 249, 250, 251, 253
2	43, 45, 51, 53, 75, 77, 83, 85, 86, 87, 89, 90, 91, 93, 99, 101, 102, 104, 105, 106, 107, 109, 115, 117, 139, 141, 147, 149, 150, 151, 153, 154, 156, 157, 163, 165, 166, 167, 169, 170, 172, 174, 175, 177, 178, 180, 182, 184, 185, 186, 187, 189, 195, 197, 198, 199, 201, 202, 204, 206, 207, 209, 210, 212, 214, 215, 217, 218, 219, 221, 227, 229, 230, 231, 233, 234, 235, 243, 245
3	171, 173, 179, 181, 203, 205, 211, 213
Minimum costs through factorization	
2	45 = 5 × 9, 51 = 3 × 17, 75 = 5 × 15, 85 = 5 × 17, 90 = 2 × 9 × 5, 99 = 3 × 33, 102 = 2 × 3 × 17, 105 = 7 × 15, 150 = 2 × 5 × 15, 170 = 2 × 5 × 17, 180 = 4 × 9 × 5, 186 = 2 × 3 × 31, 189 = 7 × 9, 195 = 3 × 65, 198 = 2 × 3 × 33, 210 = 2 × 7 × 15, 217 = 7 × 31, 231 = 7 × 33
3	171 = 3 × 57, 173 = 8 + 165, 179 = 51 + 128, 181 = 1 + 180, 203 = 1 + 210, 213 = 3 × 71, 205 = 5 × 41, 203 = 7 × 29

Reference: *Digital Signal Processing with FPGAs by Uwe Meyer-Baese*

The MATLAB code used in this example implements a simple FIR filter. The example also shows a MATLAB test bench that exercises the filter.

```
design_name = 'mlhdlc_csd.m';  
testbench_name = 'mlhdlc_csd_tb.m';
```

**1** Design: mlhdlc\_csd

**2** Test Bench: mlhdlc\_csd\_tb

### **Create a New Folder and Copy Relevant Files**

Execute the following lines of code to copy the necessary example files into a temporary folder.

```
mlhdlc_demo_dir = fullfile(matlabroot, 'toolbox', 'hdlcoder', 'hdlcoderdemo');  
mlhdlc_temp_dir = [tempdir 'mlhdlc_csd'];
```

```
% create a temporary folder and copy the MATLAB files  
cd(tempdir);  
[~, ~, ~] = rmdir(mlhdlc_temp_dir, 's');  
mkdir(mlhdlc_temp_dir);  
cd(mlhdlc_temp_dir);
```

```
copyfile(fullfile(mlhdlc_demo_dir, design_name), mlhdlc_temp_dir);  
copyfile(fullfile(mlhdlc_demo_dir, testbench_name), mlhdlc_temp_dir);
```

### **Simulate the Design**

Simulate the design with the test bench prior to code generation to make sure there are no runtime errors.

```
mlhdlc_csd_tb
```

### **Create a New Project From the Command Line**

Create a new project by entering the following command:

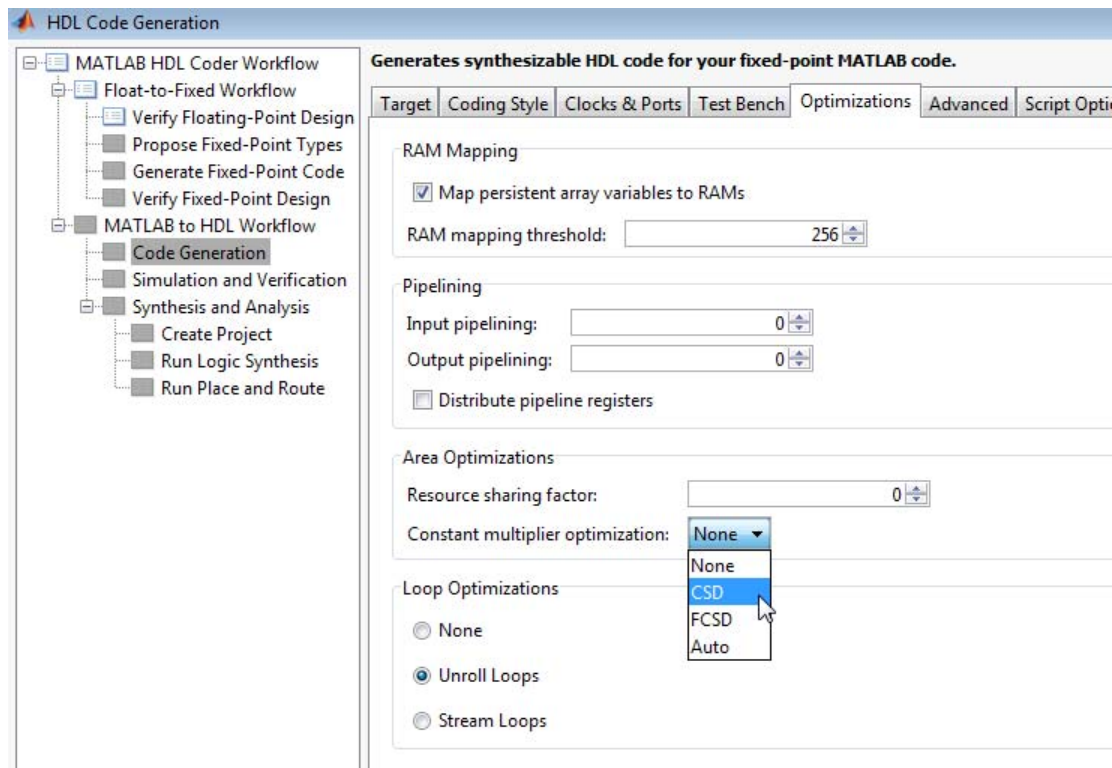
```
coder -hdlcoder -new csd_prj
```

Next, add the file 'mlhdlc\_csd.m' to the project as the MATLAB Function and 'mlhdlc\_csd\_tb.m' as the MATLAB Test Bench.

You can refer to Getting Started with MATLAB to HDL Workflow tutorial for a more complete tutorial on creating and populating MATLAB HDL Coder projects.

### Explore CSD Optimization

Look in the Optimizations tab to explore the constant multiplier optimization options.



The screenshot shows the HDL Code Generation tool interface. The left pane displays the MATLAB HDL Coder Workflow tree, with 'Code Generation' selected under 'MATLAB to HDL Workflow'. The main pane is titled 'Generates synthesizable HDL code for your fixed-point MATLAB code.' and has several tabs: Target, Coding Style, Clocks & Ports, Test Bench, Optimizations (selected), Advanced, and Script Options. The Optimizations tab contains the following settings:

- RAM Mapping:**  Map persistent array variables to RAMs. RAM mapping threshold: 256.
- Pipelining:** Input pipelining: 0, Output pipelining: 0.  Distribute pipeline registers.
- Area Optimizations:** Resource sharing factor: 0. Constant multiplier optimization: **CSD** (selected from a dropdown menu showing None, CSD, FCSD, Auto).
- Loop Optimizations:**  None,  Unroll Loops,  Stream Loops.

### Generate Code without Constant Multiplier Optimization

- 1 Launch the Workflow Advisor.
- 2 Click the 'Code Generation' step.
- 3 In the Optimizations tab, leave the 'Constant multiplier optimization' option as 'None'.
- 4 Enable the 'Unroll Loops' option to inline multiplier constants.
- 5 Right-click 'Code Generation' and choose 'Run the task' to run all the steps from the beginning through HDL code generation.
- 6 Examine the generated code.

```

329  -- filtered output
330  --!mlhdlc_csd_FixPt:40' y_out = fi((h( 1 )*a1 + h( 2 )*a2) + (h( 3 )*a3 + h( 4 )*a4),
331  p22y_out_mul_temp <= (-2194) * a1;
332  p22y_out_add_cast <= resize(p22y_out_mul_temp, 29);
333  p22y_out_mul_temp_1 <= (-1373) * a2;
334  p22y_out_add_cast_1 <= resize(p22y_out_mul_temp_1, 29);
335  p22y_out_add_temp <= p22y_out_add_cast + p22y_out_add_cast_1;
336  p22y_out_add_cast_2 <= resize(p22y_out_add_temp, 30);
337  p22y_out_mul_temp_2 <= 3319 * a3;
338  p22y_out_add_cast_3 <= resize(p22y_out_mul_temp_2, 29);
339  p22y_out_mul_temp_3 <= 6658 * a4;
340  p22y_out_add_cast_4 <= resize(p22y_out_mul_temp_3, 29);
341  p22y_out_add_temp_1 <= p22y_out_add_cast_3 + p22y_out_add_cast_4;
342  p22y_out_add_cast_5 <= resize(p22y_out_add_temp_1, 30);
343  p22y_out_add_temp_2 <= p22y_out_add_cast_2 + p22y_out_add_cast_5;
344  y_out_1 <= p22y_out_add_temp_2(26 DOWNT0 13);
345

```

Take a look at the resource report for adder and multiplier usage without the CSD optimization.

Multipliers	4
Adders/Subtractors	7
Registers	23
RAMs	0
Multiplexers	0

### Generate Code with CSD Optimization

- 1 Launch the Workflow Advisor.
- 2 Click the 'Code Generation' step.
- 3 In the Optimizations tab, choose 'CSD as the 'Constant multiplier optimization' option.
- 4 Enable the 'Unroll Loops' option to inline multiplier constants.
- 5 Right-click 'Code Generation and select 'Run the task' to run all the steps from the beginning through HDL code generation.
- 6 Examine the generated code.

```
329 -- filtered output
330 --'mlhdlc_csd_FixPt:40' y_out = fi((h( 1 )*a1 + h( 2 )*a2) + (h( 3 )*a3 + h( 4 )*a4),
331 -- CSD Encoding (2194) : 0100010010010; Cost (Adders) = 3
332 p22y_out_mul_temp <= - (((resize(a1 & '0' & '0' & '0' & '0' & '0' & '0' & '0' & '0' & '0'
333 p22y_out_add_cast <= resize(p22y_out_mul_temp, 29);
334 -- CSD Encoding (1373) : 0101011001'01; Cost (Adders) = 5
335 p22y_out_mul_temp_1 <= - (((((resize(a2 & '0' & '0' & '0' & '0' & '0' & '0' & '0' & '0' &
336 p22y_out_add_cast_1 <= resize(p22y_out_mul_temp_1, 29);
337 p22y_out_add_temp <= p22y_out_add_cast + p22y_out_add_cast_1;
338 p22y_out_add_cast_2 <= resize(p22y_out_add_temp, 30);
339 -- CSD Encoding (3319) : 0110100001'001'; Cost (Adders) = 4
340 p22y_out_mul_temp_2 <= (((resize(a3 & '0' & '0' & '0' & '0' & '0' & '0' & '0' & '0' & '0' &
341 p22y_out_add_cast_3 <= resize(p22y_out_mul_temp_2, 29);
342 -- CSD Encoding (6658) : 01101000000010; Cost (Adders) = 3
343 p22y_out_mul_temp_3 <= ((resize(a4 & '0' & '0' & '0' & '0' & '0' & '0' & '0' & '0' & '0' &
344 p22y_out_add_cast_4 <= resize(p22y_out_mul_temp_3, 29);
345 p22y_out_add_temp_1 <= p22y_out_add_cast_3 + p22y_out_add_cast_4;
346 p22y_out_add_cast_5 <= resize(p22y_out_add_temp_1, 30);
347 p22y_out_add_temp_2 <= p22y_out_add_cast_2 + p22y_out_add_cast_5;
348 y_out_1 <= p22y_out_add_temp_2(26 DOWNT0 13);
```

Examine the code with comments that outline the CSD encoding for all the constant multipliers.



Look at the resource report and notice that with the CSD optimization, the number of multipliers is reduced to zero and multipliers are replaced by shifts and adders.

Multipliers	0
Adders/Subtractors	24
Registers	23
RAMs	0
Multiplexers	0

### Generate Code with FCSD Optimization

- 1 Launch the Workflow Advisor.
- 2 Click the 'Code Generation' step.
- 3 In the Optimizations tab, choose 'FCSD' as the 'Constant multiplier optimization' option.
- 4 Enable the 'Unroll Loops' option to inline multiplier constants.
- 5 Right-click 'Code Generation' and select 'Run the task' to run all the steps from the beginning through HDL code generation.
- 6 Examine the generated code.



```
clear mex;  
cd (mlhdlc_demo_dir);  
rmdir(mlhdlc_temp_dir, 's');
```

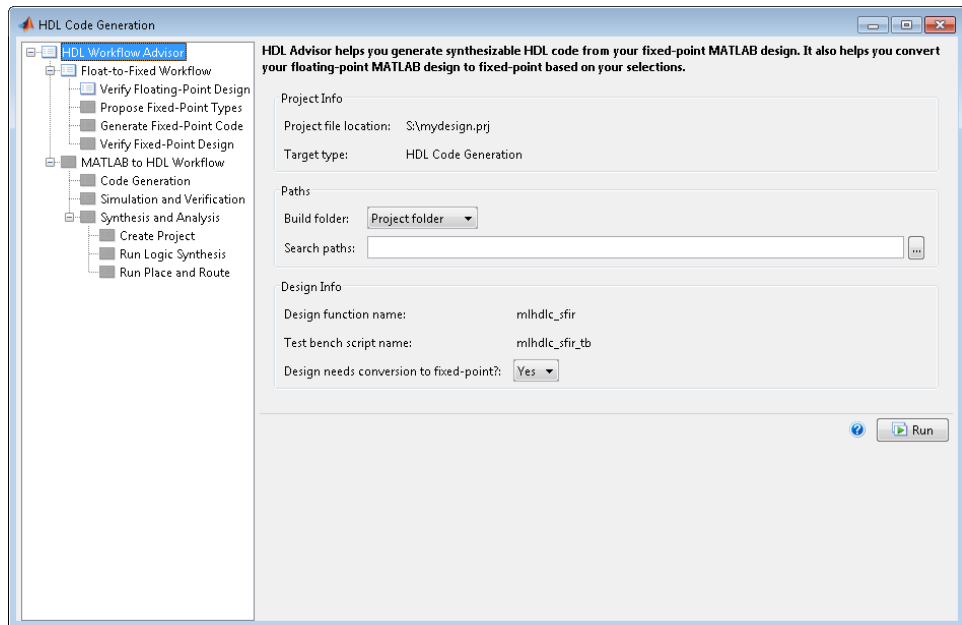


# HDL Workflow Advisor Reference

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- “HDL Workflow Advisor” on page 6-2
- “Floating-Point to Fixed-Point Conversion” on page 6-6
- “MATLAB to HDL Code and Synthesis” on page 6-14

## HDL Workflow Advisor



### Overview

The HDL Workflow Advisor is a tool that supports a suite of tasks covering the stages of the ASIC and FPGA design process, including converting floating-point MATLAB algorithms to fixed-point algorithms. Some tasks perform code validation or checking; others run the HDL code generator or third-party tools. Each folder at the top level of the HDL Workflow Advisor contains a group of related tasks that you can select and run.

Use the HDL Workflow Advisor to:

- Convert floating-point MATLAB algorithms to fixed-point algorithms.  
If you already have a fixed-point MATLAB algorithm, set **Design needs conversion to Fixed Point?** to No to skip this step.
- Generate HDL code from fixed-point MATLAB algorithms.
- Simulate the HDL code using a third-party simulation tool.

- Synthesize the HDL code and run a mapping process that maps the synthesized logic design to the target FPGA.
- Run a Place and Route process that takes the circuit description produced by the previous mapping process, and emits a circuit description suitable for programming an FPGA.

## Procedures

**Automatically Run Tasks.** To automatically run the tasks within a folder:

- 1 Click the **Run** button. The tasks run in order until a task fails.

Alternatively, right-click the folder to open the context menu. From the context menu, select **Run** to run the tasks within the folder.

- 2 If a task in the folder fails:
  - a Fix the failure using the information in the results pane.
  - b Continue the run by clicking the **Run** button.

**Run Individual Tasks.** To run an individual task:

- 1 Click the **Run** button.

Alternatively, right-click the task to open the context menu. From the context menu, select **Run** to run the selected task.

- 2 Review Results. The possible results are:

**Pass:** Move on to the next task.

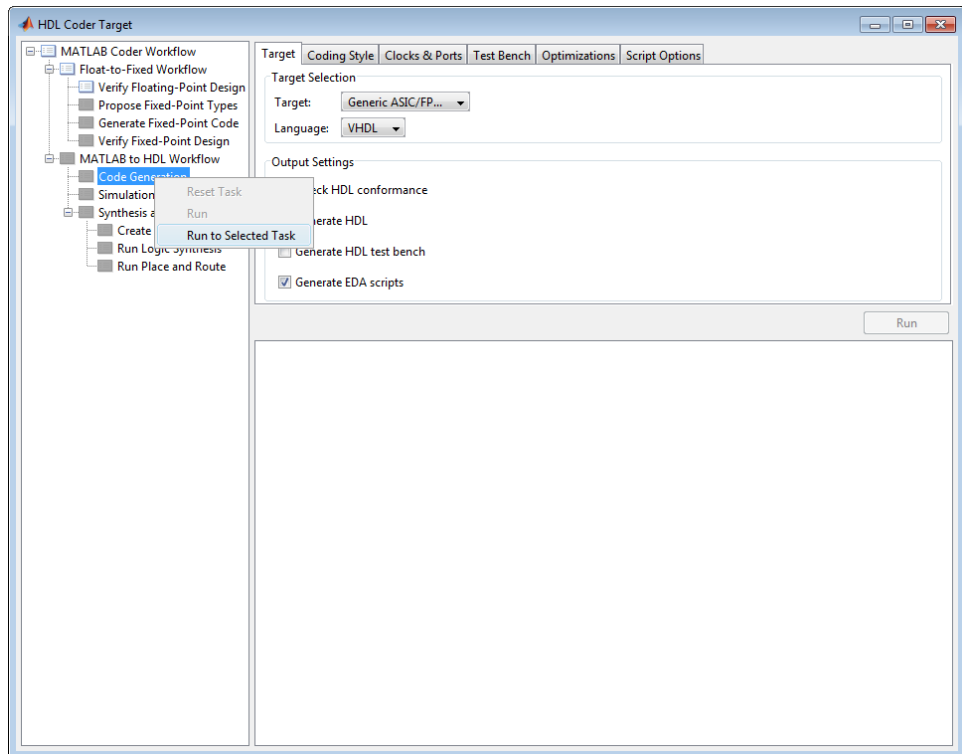
**Warning:** Review results, decide whether to move on or fix.

**Fail:** Review results, do not move on without fixing.

- 3 If required, fix the issue using the information in the results pane.
- 4 Once you have fixed a **Warning** or **Failed** task, rerun the task by clicking **Run**.

**Run to Selected Task.** To run the tasks up to and including the currently selected task:

- 1 Select the last task that you want to run.
- 2 Right-click this task to open the context menu.
- 3 From the context menu, select Run to Selected Task.



---

**Note** If a task before the selected task fails, the Workflow Advisor stops at the failed task.

---

**Reset a Task.** To reset a task:

- 1 Select the task that you want to reset.
- 2 Right-click this task to open the context menu.



- 3 From the context menu, select **Reset Task** to reset this and subsequent tasks.

**Reset All Tasks in a Folder.** To reset a task:

- 1 Select the folder that you want to reset.
- 2 Right-click this folder to open the context menu.
- 3 From the context menu, select **Reset Task** to reset the tasks this folder and subsequent folders.

## Floating-Point to Fixed-Point Conversion

### In this section...

“Floating-Point to Fixed-Point Conversion” on page 6-6

“Verify Floating-Point Design” on page 6-6

“Propose Fixed-Point Types” on page 6-9

“Generate Fixed-Point Code” on page 6-12

“Verify Fixed-Point Design” on page 6-13

### Floating-Point to Fixed-Point Conversion

The floating-point to fixed-point conversion workflow in the HDL Workflow Advisor simulates the floating-point design, proposes fixed-point data types, generates fixed-point code, and verifies the fixed-point design.

The **Float to Fixed** HDL Workflow Advisor task is displayed only if **Design needs conversion to Fixed Point?** is set to **Yes**.

### Verify Floating-Point Design

Analyze the MATLAB function and test bench; run a floating-point simulation.

### Input Parameters

#### Accelerate Test Bench for faster simulation

Generates MEX functions for the main loop in the test bench to speed up simulation.

If your test bench contains a streaming loop that calls your MATLAB function, simulation of your test bench might take a long time. If you select **Accelerate Test Bench for faster simulation**, the Workflow Advisor generates a MEX function for the `for`-loop in the test bench and runs this MEX function to simulate the test bench.

If the streaming loop in the test bench is not suitable for code generation, you might encounter errors. In this case, either check that

the constructs in the loop are suitable for code generation or clear **Accelerate Test Bench for faster simulation**, and then rerun this task. For more information about code generation support, see the MATLAB Coder documentation.

**Default:** On

## Results and Recommended Actions

Conditions	Recommended Action
<p>The Workflow Advisor reports compilation errors in your MATLAB algorithm.</p>	<p>Use the code generation report to examine the errors and fix the issues in the original source code.</p> <p>The MATLAB algorithm that you want to convert to fixed point must be suitable for code generation. For more information, see the MATLAB Coder documentation.</p>
<p>The Workflow Advisor reports compilation errors for the test bench code.</p>	<p>If your test bench contains a streaming loop that calls your algorithm and you have selected <b>Accelerate Test Bench for faster simulation</b>, check that the constructs in the loop are suitable for code generation. For more information, see the MATLAB Coder documentation.</p> <hr/> <p><b>Note</b> You can avoid these errors by clearing <b>Accelerate Test Bench for faster simulation</b>. However, if you do not accelerate your test bench, the simulation might take a long time.</p> <hr/>

<b>Conditions</b>	<b>Recommended Action</b>
You can generate a MEX function and simulate your design without using the Workflow Advisor, but the advisor reports errors at this step.	Report this issue to MathWorks®.
The Workflow Advisor generated a MEX function for your MATLAB algorithm, but there are simulation errors.	Runtime errors occurred. Check your original MATLAB code and test bench.

## Propose Fixed-Point Types

Propose fixed-point data types for variables in the MATLAB algorithm and associated test bench. By default, the advisor proposes fraction lengths for the specified word length.

### Input Parameters

#### Propose Fraction Lengths for specified Word length

Propose fraction lengths for your data types using the simulation range information and the specified word length.

**Default:** On

#### Propose Word Lengths for specified Fraction length

Propose word lengths for your data types using the simulation range information and the specified fraction length. The coder proposes the minimum word length for all data types to avoid overflow.

**Default:** Off

#### Default Word Length

Word length to use for proposed fixed-point data types if you select **Propose Fraction Lengths for specified Word length**

**Default:** 14

#### Default Fraction Length

Fraction length to use for proposed fixed-point data types if you select **Propose Word Lengths for specified Fraction length**

**Default:** 4

#### Safety Margin in Simulation Min/Max (%)

Specify multiplication safety factor for simulation minimum and maximum values.

**Default:** 4

The simulation minimum and maximum values are multiplied by the factor designated by this parameter, allowing you to specify a range different from that obtained from the simulation run. For example, a

value of 4 specifies that you want a range *at least* 4 percent larger. A value of -4 specifies that a range *up to* 4 percent smaller is acceptable.

## Results and Recommended Actions

The advisor lists the results in the **Proposed fixed-point types for variables** table. For each variable, this table provides the following information:

- The simulation minimum value
- The simulation maximum value
- Whether the variable is a constant
- Whether the variable is an integer
- The proposed fixed-point data type for the specified word (or fraction) length

The screenshot shows the HDL Code Generation software interface. The main window displays the 'Proposed fixed-point data types for variables in your MATLAB design based on simulation data and word length settings.' The 'Advanced Settings' tab is active, showing 'Propose fraction lengths for specified word length' selected. The 'Default word length' is set to 14, and the 'Default fraction length' is set to 4. The 'Safety margin for simulation min/max (%)' is set to 4.

The 'Proposed Types' table is shown below, with columns for Design, Min, Max, IsInt, Type, RoundMode, and OverflowMode. The table lists various variables and their corresponding fixed-point data types and overflow modes.

Design	Min	Max	IsInt	Type	RoundMode	OverflowMode
a1	-1.9992893467997...	1.9977514492929604		sfix14_En11	floor	wrap
a2	-1.992314672599056	1.999807240482062		sfix14_En11	floor	wrap
a3	-1.996123539135293	1.9997334214929798		sfix14_En11	floor	wrap
a4	-1.9981269790184...	1.9999771889625523		sfix14_En11	floor	wrap
a5	-0.4349718363811...	0.4223737819616705		sfix14_En14	floor	wrap
a6	-1.2144314973019...	1.2178942850713204		sfix14_En12	floor	wrap
delayed_xout	-0.9999873669329...	1.0		sfix14_En12	floor	wrap
h_in1	-0.1339	-0.1339		sfix14_En15	floor	wrap
h_in2	-0.0838	-0.0838		sfix14_En16	floor	wrap
h_in3	0.2026	0.2026		ufix14_En16	floor	wrap
h_in4	0.4064	0.4064		ufix14_En15	floor	wrap
m1	-0.2674989196003...	0.26770484353649...		sfix14_En14	floor	wrap
m2	-0.1675838467523...	0.1669596956280...		sfix14_En15	floor	wrap
m3	-0.4023986290288...	0.4051459911944777		sfix14_En14	floor	wrap
m4	-0.8120428682721...	0.8127907295947876		sfix14_En13	floor	wrap
m5	-0.9999873669329...	1.0		sfix14_En12	floor	wrap
m6	-0.9999873669329...	1.0		sfix14_En12	floor	wrap
m7	-0.9999873669329...	1.0		sfix14_En12	floor	wrap
m8	-0.9999873669329...	1.0		sfix14_En12	floor	wrap
x_in	-0.9999873669329...	1.0		sfix14_En12	floor	wrap
y_out	-1.2151956482894...	1.2158941022153251		sfix14_En12	floor	wrap

You can edit the information in the table. The advisor highlights modified data in gray and stores the updated information in the HDL Coder project. You can revert an edited value to the proposed value by right-clicking the value and selecting **Remove Custom Setting**. You can revert edited values to the proposed values by clicking the **Clear Customizations** link.

<b>Conditions</b>	<b>Recommended Action</b>
Simulation output for generated code is not functionally equivalent to the operation of the original MATLAB algorithm	Modify proposed fixed-point data types
Operating range might be larger than the simulated range	Increase the simulation <b>Min</b> or <b>Max</b> settings

### Action Results

- Click **Clear Customizations** to revert edited values to the proposed values.
- Click **Show Types Report** to create a report that contains the instrumentation results.

## Generate Fixed-Point Code

Generate fixed-point MATLAB code for the MATLAB function and test bench.

### Input Parameters

#### List of Function Replacements

Specify **Function** and **Replacement** names for floating point MATLAB operators or functions you wish to replace with custom fixed-point MATLAB functions. The generated test bench automatically uses the resulting fixed-point design, and the input values are automatically converted to fixed-point types.

For example, to replace the MATLAB function `min` with a custom `my_compare` function, add an entry with the two function name strings. Remember to add the paths for custom functions to the MATLAB path.

**Default:** None

### Results and Recommended Actions

Conditions	Recommended Action
MATLAB can't find the custom function.	Add the path for the custom function to the MATLAB path.



## Verify Fixed-Point Design

Simulate the fixed-point code and verify its operation against the original MATLAB algorithm.

### Input Parameters

#### Skip this step

Optionally skip this step.

**Default:** Off

You must run this step at least once to verify that the fixed-point design is functionally equivalent to your original MATLAB algorithm. Select to skip this step only if you have already run it and have subsequently made only minor modifications to the design.

### Results and Recommended Actions

Conditions	Recommended Action
Fixed-point algorithm operation is not functionally equivalent to the operation of the original MATLAB algorithm.	Go back to the <b>Propose Fixed-Point Types</b> task, modify fixed-point types, and then rerun the task.

## MATLAB to HDL Code and Synthesis

### In this section...

“MATLAB to HDL Code Conversion” on page 6-14

“Code Generation: Target Tab” on page 6-14

“Code Generation: Coding Style Tab” on page 6-15

“Code Generation: Clocks and Ports Tab” on page 6-17

“Code Generation: Test Bench Tab” on page 6-19

“Code Generation: Optimizations Tab” on page 6-22

“Simulation and Verification” on page 6-23

“Synthesis and Analysis” on page 6-24

### MATLAB to HDL Code Conversion

The **MATLAB to HDL Workflow** task in the HDL Workflow Advisor generates HDL code from fixed-point MATLAB code, and simulates and verifies the HDL against the fixed-point algorithm. The coder then runs synthesis, and optionally runs place and route to generate a circuit description suitable for programming an ASIC or FPGA.

### Code Generation: Target Tab

Select target hardware and language and required outputs.

#### Input Parameters

##### Target

Target hardware. Select from the list:

Generic ASIC/FPGA

Xilinx

Altera

Simulation

**Language**

Select the language (VHDL or Verilog) in which code is generated. The selected language is referred to as the target language.

**Default:** VHDL

**Check HDL Conformance**

Enable HDL conformance checking.

**Default:** Off

**Generate HDL**

Enable generation of HDL code for the fixed-point MATLAB algorithm.

**Default:** On

**Generate HDL Test Bench**

Enable generation of HDL code for the fixed-point test bench.

**Default:** Off

**Generate EDA Scripts**

Enable generation of script files for third-party electronic design automation (EDA) tools. These scripts let you compile and simulate generated HDL code and synthesize generated HDL code.

**Default:** On

**Code Generation: Coding Style Tab**

Parameters that affect the style of the generated code.

**Input Parameters****Preserve MATLAB code comments**

Include MATLAB code comments in generated code.

**Default:** On

**Include MATLAB source code as comments**

Include MATLAB source code as comments in the generated code. The comments precede the associated generated code. Includes the function signature in the function banner.

**Default:** On

**Generate Report**

Enable a code generation report.

**Default:** Off

**VHDL File Extension**

Specify the file name extension for generated VHDL files.

**Default:** .vhd

**Verilog File Extension**

Specify the file name extension for generated Verilog files.

**Default:** .v

**Comment in header**

Specify comment lines in header of generated HDL and test bench files.

**Default:** None

Text entered in this field generates a comment line in the header of the generated code. The code generator adds leading comment characters for the target language. When newlines or linefeeds are included in the string, the code generator emits single-line comments for each newline.

**Package postfix**

The coder applies this option only if a package file is required for the design.

**Default:** \_pkg

**Entity conflict postfix**

Specify the string to resolve duplicate VHDL entity or Verilog module names in generated code.

**Default:** \_block

**Reserved word postfix**

Specify a string to append to value names, postfix values, or labels that are VHDL or Verilog reserved words.

**Default:** `_rsvd`

**Clocked process postfix**

Specify a string to append to HDL clock process names.

**Default:** `_process`

**Complex real part postfix**

Specify a string to append to real part of complex signal names.

**Default:** `'_re'`

**Complex imaginary part postfix**

Specify a string to append to imaginary part of complex signal names.

**Default:** `'_im'`

**Pipeline postfix**

Specify a string to append to names of input or output pipeline registers.

**Default:** `'_pipe'`

**Enable prefix**

Specify the base name string for internal clock enables and other flow control signals in generated code.

**Default:** `'enb'`

**Code Generation: Clocks and Ports Tab**

Clock and port settings

**Input Parameters****Reset type**

Specify whether to use asynchronous or synchronous reset logic when generating HDL code for registers.

**Default:** Asynchronous

### **Reset Asserted level**

Specify whether the asserted (active) level of reset input signal is active-high or active-low.

**Default:** Active-high

### **Reset input port**

Enter the name for the reset input port in generated HDL code.

**Default:** reset

### **Clock input port**

Specify the name for the clock input port in generated HDL code.

**Default:** clk

### **Clock enable input port**

Specify the name for the clock enable input port in generated HDL code.

**Default:** clk

### **Oversampling factor**

Specify frequency of global oversampling clock as a multiple of the design under test (DUT) base rate (1).

**Default:** 1

### **Input data type**

Specify the HDL data type for input ports.

For VHDL, the options are:

- `std_logic_vector`  
Specifies VHDL type `STD_LOGIC_VECTOR`
- `signed/unsigned`  
Specifies VHDL type `SIGNED` or `UNSIGNED`

**Default:** `std_logic_vector`

For Verilog, the options are:

- In generated Verilog code, the data type for all ports is 'wire'. Therefore, **Input data type** is disabled when the target language is Verilog.

**Default:** wire

### **Output data type**

Specify the HDL data type for output data types.

For VHDL, the options are:

- Same as input data type  
Specifies that output ports have the same type specified by Input data type.
- `std_logic_vector`  
Specifies VHDL type `STD_LOGIC_VECTOR`
- signed/unsigned  
Specifies VHDL type `SIGNED` or `UNSIGNED`

**Default:** Same as input data type

For Verilog, the options are:

- In generated Verilog code, the data type for all ports is 'wire'. Therefore, Output data type is disabled when the target language is Verilog.

**Default:** wire

### **Clock enable output port**

Specify the name for the clock enable input port in generated HDL code.

**Default:** `clk_enable`

## **Code Generation: Test Bench Tab**

Test bench settings.

## **Input Parameters**

### **Test bench name postfix**

Specify a string appended to names of reference signals generated in test bench code.

**Default:** `'_tb'`

### **Force clock**

Specify whether the test bench forces clock enable input signals.

**Default:** On

### **Clock High time (ns)**

Specify the period, in nanoseconds, during which the test bench drives clock input signals high (1).

**Default:** 5

### **Clock low time (ns)**

Specify the period, in nanoseconds, during which the test bench drives clock input signals low (0).

**Default:** 5

### **Hold time (ns)**

Specify a hold time, in nanoseconds, for input signals and forced reset input signals.

**Default:** 2 (given the default clock period of 10 ns)

### **Setup time (ns)**

Display setup time for data input signals.

**Default:** 0

### **Force clock enable**

Specify whether the test bench forces clock enable input signals.

**Default:** On



**Clock enable delay (in clock cycles)**

Define elapsed time (in clock cycles) between deassertion of reset and assertion of clock enable.

**Default:** 1

**Force reset**

Specify whether the test bench forces reset input signals.

**Default:** On

**Reset length (in clock cycles)**

Define length of time (in clock cycles) during which reset is asserted.

**Default:** 2

**Hold input data between samples**

Specify how long substrate signal values are held in valid state.

**Default:** On

**Initialize testbench inputs**

Specify initial value driven on test bench inputs before data is asserted to device under test (DUT).

**Default:** Off

**Multi file testbench**

Divide generated test bench into helper functions, data, and HDL test bench code files.

**Default:** Off

**Test bench data file name postfix**

Specify suffix added to test bench data file name when generating multi-file test bench.

**Default:** '\_data'

**Test bench reference post fix**

Specify a string appended to names of reference signals generated in test bench code.

**Default:** `'_ref'`

**Ignore data checking (number of samples)**

Specify number of samples during which output data checking is suppressed.

**Default:** 0

**Use `fiaccel` to accelerate test bench logging**

To generate a test bench, the coder simulates the original MATLAB code. Use the Fixed-Point Toolbox `fiaccel` function to accelerate this simulation and accelerate test bench logging.

**Default:** On

## **Code Generation: Optimizations Tab**

Optimization settings

### **Input Parameters**

**Map persistent array variables to RAMs**

Select to map persistent array variables to RAMs instead of mapping to shift registers.

**Default:** Off

Dependencies:

- **RAM Mapping Threshold**
- **Persistent variable names for RAM Mapping**

**RAM Mapping Threshold**

Specify the minimum RAM size required for mapping persistent array variables to RAMs.

**Default:** 256

**Persistent variable names for RAM Mapping**

Provide the names of the persistent variables to map to RAMs.

**Default:** None

**Input Pipelining**

Specify number of pipeline registers to insert at top level input ports. Can improve performance and help to meet timing constraints.

**Default:** 0

**Output Pipelining**

Specify number of pipeline registers to insert at top level output ports. Can improve performance and help to meet timing constraints.

**Default:** 0

**Distribute Pipeline Registers**

Reduces critical path by changing placement of registers in design. Operates on all registers, including those inserted using the **Input Pipelining** and **Output Pipelining** parameters, and internal design registers.

**Default:** Off

**Sharing Factor**

Number of additional sources that can share a single resource, such as a multiplier. To share resources, set **Sharing Factor** to 2 or higher; a value of 0 or 1 turns off sharing.

In a design that performs identical multiplication operations, the coder can reduce the number of multipliers by the sharing factor. This can significantly reduce area.

**Default:** 0

**Simulation and Verification**

Simulates the generated HDL code using the selected simulation tool.

**Input Parameters**

Simulation tool

Lists the available simulation tools.

**Default:** None

**Skip this step**

**Default:** Off

## Results and Recommended Actions

Conditions	Recommended Action
No simulation tool available on system path.	Add your simulation tool path to the MATLAB system path, then restart MATLAB. For more information, see “Setting Up the Synthesis Tool Path”.

## Synthesis and Analysis

This folder contains tasks to create a synthesis project for the HDL code. The task then runs the synthesis and, optionally, runs place and route to generate a circuit description suitable for programming an ASIC or FPGA.

### Input Parameters

**Skip this step**

**Default:** Off

Skip this step if you are interested only in simulation or you do not have a synthesis tool.

### Create Project

Create synthesis project for supported synthesis tool.

**Description.** This task creates a synthesis project for the selected synthesis tool and loads the project with the HDL code generated for your MATLAB algorithm.

You can select the family, device, package, and speed that you want.

When the project creation is complete, the HDL Workflow Advisor displays a link to the project in the right pane. Click this link to view the project in the synthesis tool's project window.

## Input Parameters.

### Synthesis Tool

Select from the list:

- Altera Quartus II

Generate a synthesis project for Altera® Quartus II. When you select this option, the coder sets:

- **Chip Family** to Stratix II
  - **Device Name** to EP2S60F1020C4
- You can manually change these settings.

- Xilinx ISE

Generate a synthesis project for Xilinx ISE. When you select this option, the coder:

- Sets **Chip Family** to Virtex4
  - Sets **Device Name** to xc4vsx35
  - Sets **Package Name** to ff6...
  - Sets **Speed Value** to ...
- You can manually change these settings.

### Default: No Synthesis Tool Specified

When you select No Synthesis Tool Specified, the coder does not generate a synthesis project. It clears and disables the fields in the **Synthesis Tool Selection** pane.

### Chip Family

Target device family.

**Default:** None

### Device Name

Specific target device, within selected family.

**Default:** None

**Package Name**

Available package choices. The family and device determine these choices.

**Default:** None

**Speed Value**

Available speed choices. The family, device, and package determine these choices.

**Default:** None

**Results and Recommended Actions.**

Conditions	Recommended Action
Synthesis tool fails to create project.	Read the error message returned by synthesis tool, then check the synthesis tool version, and check that you have write permission for the project folder.
Synthesis tool does not appear in dropdown list.	Add your synthesis tool path to the MATLAB system path, then restart MATLAB. For more information, see “Setting Up the Synthesis Tool Path”.

**Run Logic Synthesis**

Launch selected synthesis tool and synthesize the generated HDL code.

**Description.** This task:

- Launches the synthesis tool in the background.
- Opens the previously generated synthesis project, compiles HDL code, synthesizes the design, and emits netlists and related files.
- Displays a synthesis log in the **Result** subpane.

## Results and Recommended Actions.

Conditions	Recommended Action
Synthesis tool fails when running place and route.	Read the error message returned by the synthesis tool, modify the MATLAB code, then rerun from the beginning of the HDL Coder workflow.

## Run Place and Route

Launches the synthesis tool in the background and runs a Place and Route process.

**Description.** This task:

- Launches the synthesis tool in the background.
- Runs a Place and Route process that takes the circuit description produced by the previous mapping process, and emits a circuit description suitable for programming an FPGA.
- Displays a log in the Result subpane.

## Input Parameters.

### Skip this step

If you select **Skip this step**, the HDL Workflow Advisor executes the workflow, but omits the Perform Place and Route, marking it Passed. You might want to select **Skip this step** if you prefer to do place and route work manually.

**Default:** Off

**Results and Recommended Actions.**

<b>Conditions</b>	<b>Recommended Action</b>
Synthesis tool fails when running place and route.	Read the error message returned by the synthesis tool, modify the MATLAB code, then rerun from the beginning of the HDL Coder workflow.



# HDL Code Generation from Simulink

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- Chapter 7, “Code Generation Options in the HDL Coder Dialog Boxes”
- Chapter 8, “Specifying Block Implementations and Parameters for HDL Code Generation”
- Chapter 9, “Guide to Supported Blocks and Block Implementations”
- Chapter 10, “Generating HDL Code for Multirate Models”
- Chapter 11, “The `hdldemo1ib` Block Library”
- Chapter 12, “Generating Bit-True Cycle-Accurate Models”
- Chapter 13, “Optimization”
- Chapter 14, “Code Generation Reports, HDL Compatibility Checker, Block Support Library, and Code Annotation”
- Chapter 15, “Interfacing Subsystems and Models to HDL Code”
- Chapter 16, “Stateflow HDL Code Generation Support”
- Chapter 17, “Generating HDL Code with the MATLAB Function Block”
- Chapter 18, “Generating Scripts for HDL Simulators and Synthesis Tools”
- Chapter 19, “Using the HDL Workflow Advisor”
- Chapter 20, “FPGA Board Customization”
- Chapter 21, “HDL Workflow Advisor Tasks”
- Chapter 22, “Code Generation Control Files”
- Chapter 23, “Properties — Alphabetical List”

- Chapter 24, “Property Reference”
- Chapter 25, “Functions — Alphabetical List”
- Chapter 26, “Function Reference”

# Code Generation Options in the HDL Coder Dialog Boxes

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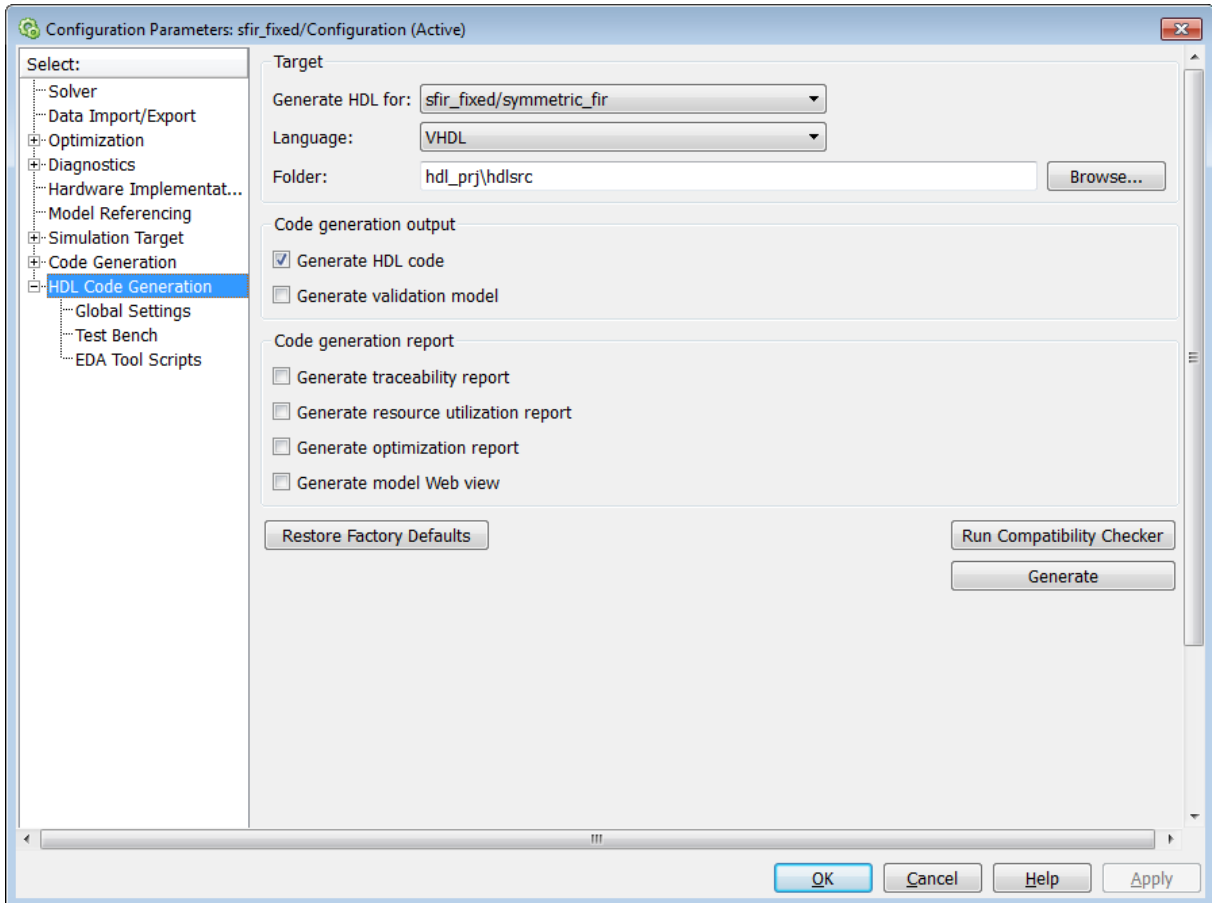
- “Set HDL Code Generation Options” on page 7-2
- “HDL Code Generation Pane: General” on page 7-8
- “HDL Code Generation Pane: Global Settings” on page 7-21
- “HDL Code Generation Pane: Test Bench” on page 7-72
- “HDL Code Generation Pane: EDA Tool Scripts” on page 7-99

## Set HDL Code Generation Options

In this section...
“HDL Code Generation Options in the Configuration Parameters Dialog Box” on page 7-2
“HDL Code Generation Options in the Model Explorer” on page 7-3
“Code Menu” on page 7-4
“HDL Code Options in the Block Context Menu” on page 7-5
“The HDL Block Properties Dialog Box” on page 7-6

### **HDL Code Generation Options in the Configuration Parameters Dialog Box**

The following figure shows the top-level **HDL Code** pane in the Configuration Parameters dialog box. To open this dialog box, select **Simulation > Model Configuration Parameters** in the Simulink window. Then select **HDL Code** from the list on the left.



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**Note** When the **HDL Code Generation** pane of the Model Configuration Parameters dialog box appears, clicking the **Help** button displays general help for the Model Configuration Parameters dialog box.

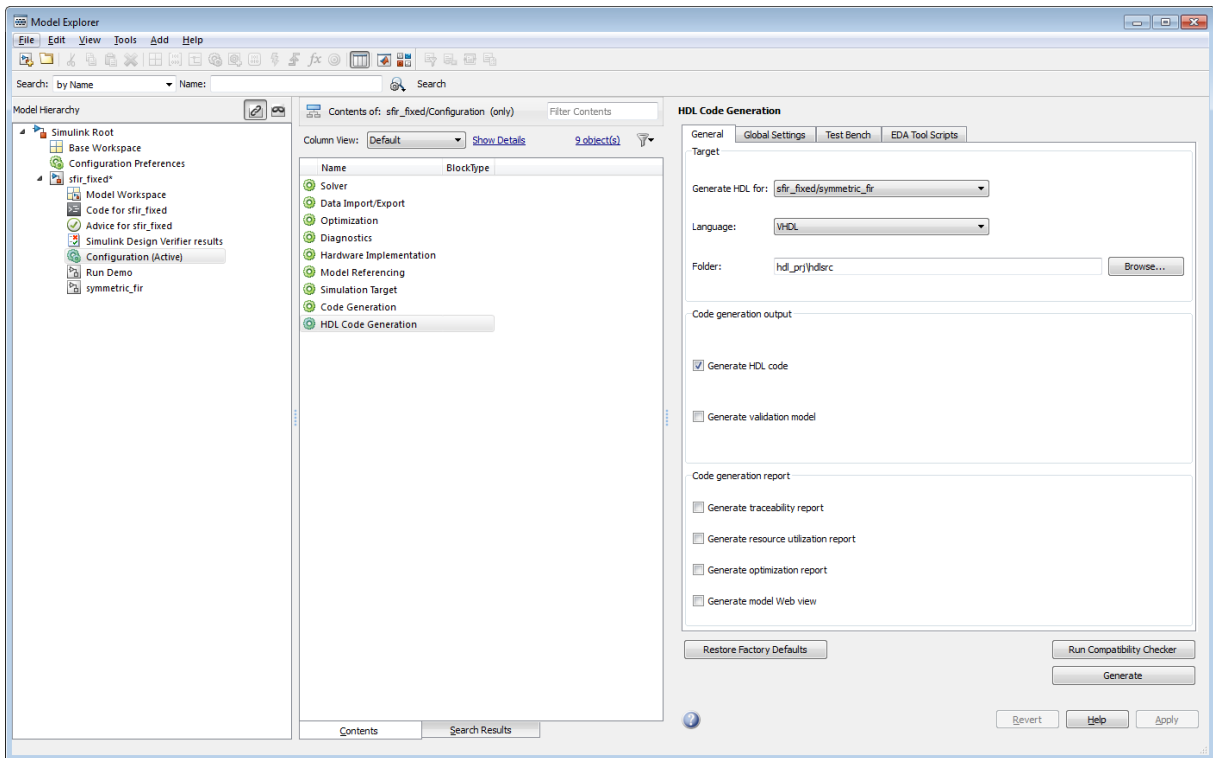
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## HDL Code Generation Options in the Model Explorer

The following figure shows the top-level **HDL Code** pane as displayed in the Contents pane of the Model Explorer.

To view this dialog box:

- 1 Open the Model Explorer.
- 2 Select your model's active configuration set in the **Model Hierarchy** tree on the left.
- 3 Select **HDL Code Generation** from the list in the Contents pane.



### Code Menu

The **Code > HDL Code** submenu provides shortcuts to the HDL code generation options. You can also use this submenu to initiate code generation.

Options include:

- **HDL Workflow Advisor:** Open the HDL Workflow Advisor.
- **Options:** Open the **HDL Code Generation** pane in the Configuration Parameters dialog box.
- **Generate HDL:** Initiate HDL code generation; equivalent to the **Generate** button in the Model Configuration Parameters dialog box or Model Explorer.
- **Generate Test Bench:** Initiate test bench code generation; equivalent to the **Generate Test Bench** button in the Model Configuration Parameters dialog box or Model Explorer. If you do not select a subsystem in the **Generate HDL for** menu, the **Generate Test Bench** menu option is not available.
- **Add HDL Coder Configuration to Model or Remove HDL Coder Configuration from Model:** The *HDL configuration component* is internal data that the coder creates and attaches to a model. This component lets you view the HDL Code pane in the Model Configurations Parameters dialog box, and use the **HDL Code** pane to set HDL code generation options. If you need to add or remove the **HDL Code** configuration component to or from a model, use this option to do so. For more information, see “Add or Remove the HDL Configuration Component” on page 14-39.

## HDL Code Options in the Block Context Menu

When you right-click a block that the coder supports, the context menu for the block includes an **HDL Code** submenu. The coder enables items in the submenu according to:

- The block type: for subsystems, the menu enables some options that are specific to subsystems.
- Whether or not code and traceability information has been generated for the block or subsystem.

The following summary describes the **HDL Code** submenu options.

<b>Option</b>	<b>Description</b>	<b>Availability</b>
<b>Check Subsystem Compatibility</b>	Runs the HDL compatibility checker (checkhdl) on the subsystem.	Available only for subsystems.
<b>Generate HDL for Subsystem</b>	Runs the HDL code generator (makehdl) and generates code for the subsystem.	Available only for subsystems.
<b>HDL Coder Properties</b>	Opens the Model Configuration Parameters dialog box, with the top-level HDL Code pane selected.	Available for blocks or subsystems.
<b>HDL Block Properties</b>	Opens a block properties dialog box for the block or subsystem. See “The HDL Block Properties Dialog Box” on page 7-6 for more information.	Available for blocks or subsystems.
<b>HDL Workflow Advisor</b>	Opens the HDL Workflow Advisor for the subsystem.	Available only for subsystems.
<b>Navigate to Code</b>	Activates the HTML code generation report window, displaying the beginning of the code generated for the selected block or subsystem. See “Tracing from Model to Code” on page 14-18 for more information.	Enabled when both code and a traceability report have been generated for the block or subsystem.

## The HDL Block Properties Dialog Box

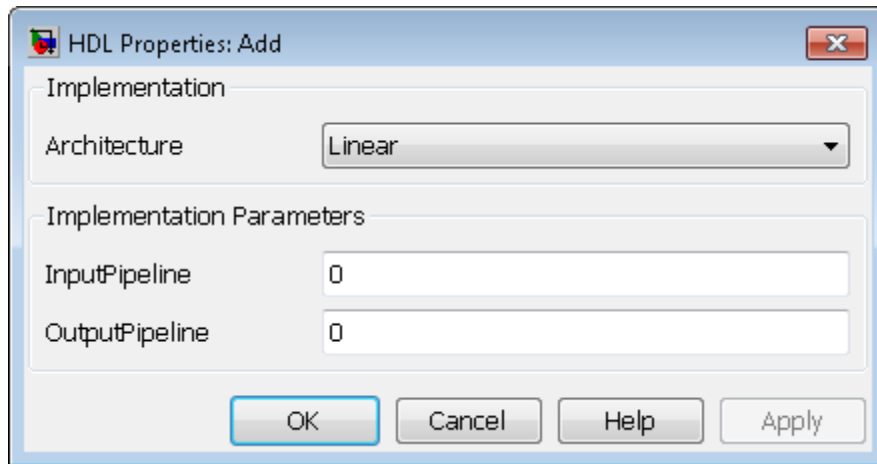
The coder provides selectable alternate *block implementations* for many block types. Each implementation is optimized for different characteristics, such



as speed or chip area. The HDL Properties dialog box lets you choose the implementation for a selected block.

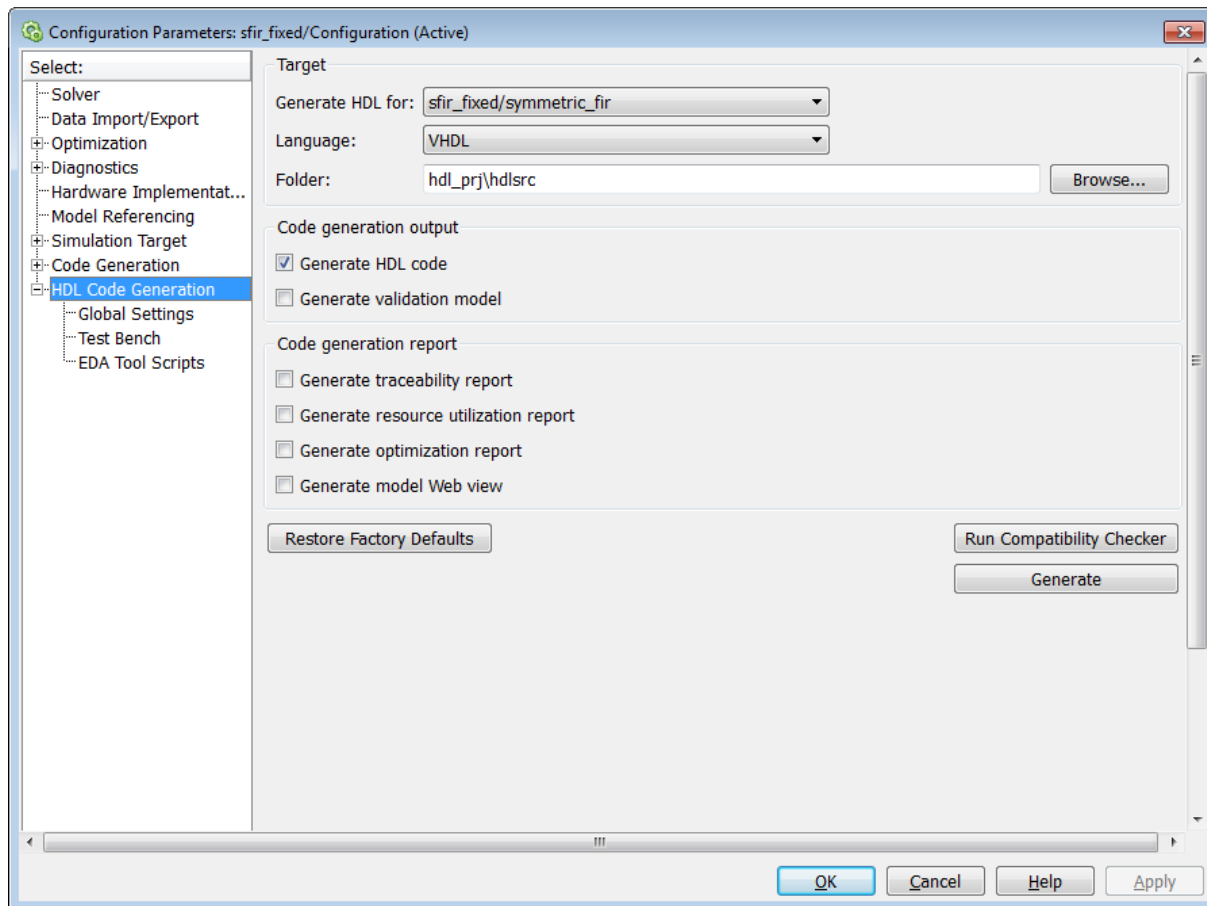
Most block implementations support a number of *implementation parameters* that let you control further details of code generation for the block. The HDL Properties dialog box lets you set implementation parameters for a block.

The following figure shows the HDL Properties dialog box for a block.



There are a number of ways to specify implementations and implementation parameters for individual blocks or groups of blocks. See “Set and View HDL Block Parameters” on page 8-2 for detailed information.

## HDL Code Generation Pane: General



### In this section...

“HDL Code Generation Top-Level Pane Overview” on page 7-10

“Generate HDL for” on page 7-12

“Language” on page 7-13

“Folder” on page 7-14

“Generate HDL code” on page 7-15

**In this section...**

“Generate validation model” on page 7-16

“Generate traceability report” on page 7-17

“Generate resource utilization report” on page 7-18

“Generate optimization report” on page 7-19

“Generate model Web view” on page 7-20

### **HDL Code Generation Top-Level Pane Overview**

The top-level **HDL Code Generation** pane contains buttons that initiate code generation and compatibility checking, and sets code generation parameters.

### **Buttons in the HDL Code Generation Top-Level Pane**

The buttons in the **HDL Code Generation** pane perform functions related to code generation. These buttons are:

**Generate:** Initiates code generation for the system selected in the **Generate HDL for** menu. See also `makehdl`.

**Run Compatibility Checker:** Invokes the compatibility checker to examine the system selected in the **Generate HDL for** menu for compatibility problems. See also `checkhdl`.

**Browse:** Lets you navigate to and select the target folder to which generated code and script files are written. The path to the target folder is entered into the **Folder** field.

**Restore Factory Defaults:** sets model parameters to their default values; also (if the model has a control file linked to it) unlinks the control file from the model.



### **Generate HDL for**

Select the subsystem or model from which code is generated. The list includes the path to the root model and to subsystems in the model.

### **Settings**

**Default:** The root model is selected.

### **Command-Line Information**

Pass in the path to the model or subsystem for which code is to be generated as the first argument to `makehdl`.

### **See Also**

`makehdl`

## Language

Select the language (VHDL or Verilog) in which code is generated. The selected language is referred to as the target language.

## Settings

**Default:** VHDL

VHDL

Generate VHDL code.

Verilog

Generate Verilog code.

## Command-Line Information

**Property:** TargetLanguage

**Type:** string

**Value:** 'VHDL' | 'Verilog'

**Default:** 'VHDL'

## See Also

- TargetLanguage
- makehdl

### Folder

Enter a path to the folder into which code is generated. Alternatively, click **Browse** to navigate to and select a folder. The selected folder is referred to as the target folder.

### Settings

**Default:** The default target folder is a subfolder of your working folder, named `hdlsrc`.

### Command-Line Information

**Property:** `TargetDirectory`

**Type:** `string`

**Value:** A valid path to your target folder

**Default:** `'hdlsrc'`

### See Also

- `TargetDirectory`
- `makehdl`



## Generate HDL code

Enable or disable HDL code generation for the model.

### Settings

**Default:** On



On

Generate HDL code.



Off

Do not generate HDL code.

### Command-Line Information

**Property:** GenerateHDLCode

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'on'

### See Also

GenerateHDLCode

### Generate validation model

Enable or disable generation of a validation model that verifies the functional equivalence of the original model with the generated model. The validation model contains both the original and the generated DUT models.

If you enable generation of a validation model, also enable delay balancing to keep the generated DUT model synchronized with the original DUT model. Validation fails when there is a mismatch between delays in the original DUT model and delays in the generated DUT model.

#### Settings

**Default:** Off



On

Generate the validation model.



Off

Do not generate the validation model.

#### Command-Line Information

**Property:** `GenerateValidationModel`

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'off'

#### See Also

`GenerateValidationModel`, `BalanceDelays`

## Generate traceability report

Enable or disable generation of an HTML code generation report with hyperlinks from code to model and model to code.

### Settings

**Default:** Off



On

Create and display an HTML code generation report. See [Creating and Using a Code Generation Report](#).



Off

Do not create an HTML code generation report.

### Command-Line Information

**Property:** Traceability

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'off'

### See Also

Traceability

### Generate resource utilization report

Enable or disable generation of an HTML resource utilization report

#### Settings

**Default:** Off

On

Create and display an HTML resource utilization report. The report contains information about the number of hardware resources (multipliers, adders, registers) used in the generated HDL code. The report includes hyperlinks to the referenced blocks in the model. See [Creating and Using a Code Generation Report](#).

Off

Do not create an HTML resource utilization report.

#### Command-Line Information

**Property:** ResourceReport

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'off'

#### See Also

ResourceReport

## Generate optimization report

Enable or disable generation of an HTML optimization report

### Settings

**Default:** Off



On

Create and display an HTML optimization report. The report contains information about the results of streaming, sharing, and distributed pipelining optimizations that were implemented in the generated code. The report includes hyperlinks back to referenced blocks, subsystems, or validation models. See [Creating and Using a Code Generation Report](#).



Off

Do not create an HTML optimization report.

### Command-Line Information

**Property:** OptimizationReport

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'off'

### See Also

OptimizationReport

### Generate model Web view

Include the model Web view in the code generation report to navigate between the code and model within the same window. You can share your model and generated code outside of the MATLAB environment. You must have a Simulink Report Generator™ license to include a Web view of the model in the code generation report.

#### Settings

**Default:** Off



On

Include model Web view in the code generation report.



Off

Omit model Web view in the code generation report.

#### Command-Line Information

**Parameter:** GenerateWebview

**Type:** string

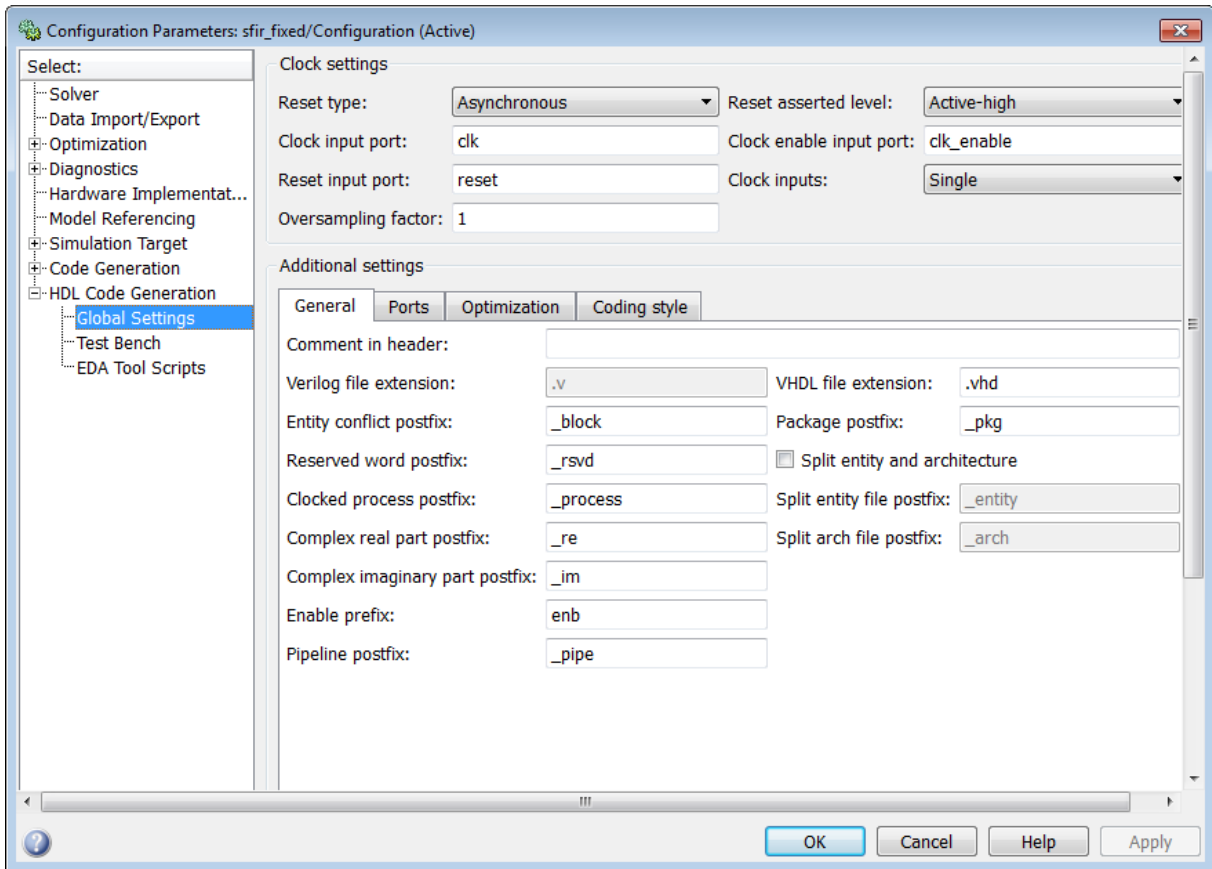
**Value:** 'on' | 'off'

**Default:** 'off'

#### See Also

GenerateWebview

## HDL Code Generation Pane: Global Settings



### In this section...

“Global Settings Overview” on page 7-24

“Reset type” on page 7-25

“Reset asserted level” on page 7-26

“Clock input port” on page 7-27

“Clock enable input port” on page 7-28

### **In this section...**

- “Reset input port” on page 7-29
- “Clock inputs” on page 7-30
- “Oversampling factor” on page 7-31
- “Comment in header” on page 7-32
- “Verilog file extension” on page 7-33
- “VHDL file extension” on page 7-34
- “Entity conflict postfix” on page 7-35
- “Package postfix” on page 7-36
- “Reserved word postfix” on page 7-37
- “Split entity and architecture” on page 7-38
- “Split entity file postfix” on page 7-40
- “Split arch file postfix” on page 7-41
- “Clocked process postfix” on page 7-42
- “Enable prefix” on page 7-43
- “Pipeline postfix” on page 7-44
- “Complex real part postfix” on page 7-45
- “Complex imaginary part postfix” on page 7-46
- “Input data type” on page 7-47
- “Output data type” on page 7-48
- “Clock enable output port” on page 7-50
- “Balance delays” on page 7-51
- “Hierarchical distributed pipelining” on page 7-52
- “Optimize timing controller” on page 7-53
- “Minimize clock enables” on page 7-55
- “RAM mapping threshold (bits)” on page 7-57
- “Represent constant values by aggregates” on page 7-58



**In this section...**

“Use rising\_edge for registers” on page 7-59

“Loop unrolling” on page 7-60

“Cast before sum” on page 7-61

“Use Verilog `timescale directives” on page 7-62

“Inline VHDL configuration” on page 7-63

“Concatenate type safe zeros” on page 7-64

“Emit time/date stamp in header” on page 7-65

“Scalarize vector ports” on page 7-66

“Minimize intermediate signals” on page 7-67

“Include requirements in block comments” on page 7-68

“Inline MATLAB Function block code” on page 7-69

“Generate parameterized HDL code from masked subsystem” on page 7-70

“RAM Architecture” on page 7-71

### **Global Settings Overview**

The **Global Settings** pane enables you to specify detailed characteristics of the generated code, such as HDL element naming and whether certain optimizations are applied.

## Reset type

Specify whether to use asynchronous or synchronous reset logic when generating HDL code for registers.

### Settings

**Default:** Asynchronous

Asynchronous

Use asynchronous reset logic.

Synchronous

Use synchronous reset logic.

### Command-Line Information

**Property:** ResetType

**Type:** string

**Value:** 'async' | 'sync'

**Default:** 'async'

### See Also

ResetType

## **Reset asserted level**

Specify whether the asserted (active) level of reset input signal is active-high or active-low.

### **Settings**

**Default:** Active-high

Active-high

Asserted (active) level of reset input signal is active-high (1).

Active-low

Asserted (active) level of reset input signal is active-low (0).

### **Command-Line Information**

**Property:** ResetAssertedLevel

**Type:** string

**Value:** 'active-high' | 'active-low'

**Default:** 'active-high'

### **See Also**

ResetAssertedLevel

## Clock input port

Specify the name for the clock input port in generated HDL code.

### Settings

**Default:** `clk`

Enter a string value to be used as the clock signal name in generated HDL code. If you specify a string that is a VHDL or Verilog reserved word, the code generator appends a reserved word postfix string to form a valid VHDL or Verilog identifier. For example, if you specify the reserved word `signal`, the resulting name string would be `signal_rsvd`.

### Command-Line Information

**Property:** `ClockInputPort`

**Type:** `string`

**Value:** A valid identifier in the target language

**Default:** `'clk'`

### See Also

`ClockInputPort`

## **Clock enable input port**

Specify the name for the clock enable input port in generated HDL code.

### **Settings**

**Default:** `clk_enable`

Enter a string value to be used as the clock enable input port name in generated HDL code. If you specify a string that is a VHDL or Verilog reserved word, the code generator appends a reserved word postfix string to form a valid VHDL or Verilog identifier. For example, if you specify the reserved word `signal`, the resulting name string would be `signal_rsvd`.

### **Tip**

The clock enable input signal is asserted active-high (1). Thus, the input value must be high for the generated entity's registers to be updated.

### **Command-Line Information**

**Property:** `ClockEnableInputPort`

**Type:** `string`

**Value:** A valid identifier in the target language

**Default:** `'clk_enable'`

### **See Also**

`ClockEnableInputPort`

## Reset input port

Enter the name for the reset input port in generated HDL code.

### Settings

**Default:** reset

Enter a string value to be used as the reset input port name in generated HDL code. If you specify a string that is a VHDL or Verilog reserved word, the code generator appends a reserved word postfix string to form a valid VHDL or Verilog identifier. For example, if you specify the reserved word `signal`, the resulting name string would be `signal_rsvd`.

### Tip

If the reset asserted level is set to active-high, the reset input signal is asserted active-high (1) and the input value must be high (1) for the entity's registers to be reset. If the reset asserted level is set to active-low, the reset input signal is asserted active-low (0) and the input value must be low (0) for the entity's registers to be reset.

### Command-Line Information

**Property:** ResetInputPort

**Type:** string

**Value:** A valid identifier in the target language

**Default:** 'reset'

### See Also

ResetInputPort

### **Clock inputs**

Specify generation of single or multiple clock inputs.

#### **Settings**

**Default:** Single

##### Single

Generates a single clock input for the DUT. If the DUT is multirate, the input clock is the master clock rate, and a timing controller is synthesized to generate additional clocks as required.

##### Multiple

Generates a unique clock for each Simulink rate in the DUT. The number of timing controllers generated depends on the contents of the DUT.

### **Command-Line Information**

**Property:** ClockInputs

**Type:** string

**Value:** 'Single' | 'Multiple'

**Default:** 'Single'

### **See Also**

ClockInputs



## Oversampling factor

Specify frequency of global oversampling clock as a multiple of the model's base rate.

### Settings

**Default:** 1.

**Oversampling factor** specifies the *oversampling factor* of a global oversampling clock. The oversampling factor expresses the desired rate of the global oversampling clock as a multiple of your model's base rate. By default, the coder does not generate a global oversampling clock.

If you want to generate a global oversampling clock:

- The **Oversampling factor** must be an integer greater than or equal to 1.
- In a multirate DUT, other rates in the DUT must divide evenly into the global oversampling rate.

### Command-Line Information

**Property:** Oversampling

**Type:** int

**Value:** integer greater than or equal to 1

**Default:** 1

### See Also

Generating a Global Oversampling Clock  
Oversampling

### **Comment in header**

Specify comment lines in header of generated HDL and test bench files.

#### **Settings**

**Default:** None

Text entered in this field generates a comment line in the header of generated model and test bench files. The code generator adds leading comment characters for the target language. When newlines or linefeeds are included in the string, the code generator emits single-line comments for each newline.

#### **Command-Line Information**

**Property:** UserComment

**Type:** string

#### **See Also**

UserComment

## Verilog file extension

Specify the file name extension for generated Verilog files.

### Settings

**Default:** `.v`

This field specifies the file name extension for generated Verilog files.

### Dependency

This option is enabled when the target language (specified by the **Language** option) is Verilog.

### Command-Line Information

**Property:** `VerilogFileExtension`

**Type:** `string`

**Default:** `' .v '`

### See Also

`VerilogFileExtension`

## **VHDL file extension**

Specify the file name extension for generated VHDL files.

### **Settings**

**Default:** .vhd

This field specifies the file name extension for generated VHDL files.

### **Dependencies**

This option is enabled when the target language (specified by the **Language** option) is VHDL.

### **Command-Line Information**

**Property:** VHDLFileExtension

**Type:** string

**Default:** '.vhd'

### **See Also**

VHDLFileExtension

## Entity conflict postfix

Specify the string used to resolve duplicate VHDL entity or Verilog module names in generated code.

### Settings

**Default:** `_block`

The specified postfix resolves duplicate VHDL entity or Verilog module names. For example, in the default case, if the coder detects two entities with the name `MyFilt`, the coder names the first entity `MyFilt` and the second instance `MyFilt_entity`.

### Command-Line Information

**Property:** `EntityConflictPostfix`

**Type:** `string`

**Value:** A valid string in the target language

**Default:** `'_block'`

### See Also

`EntityConflictPostfix`

### Package postfix

Specify a string to append to the model or subsystem name to form name of a package file.

#### Settings

**Default:** `_pkg`

The coder applies this option only if a package file is required for the design.

#### Dependency

This option is enabled when:

The target language (specified by the **Language** option) is VHDL.

The target language (specified by the **Language** option) is Verilog, and the **Multi-file test bench** option is selected.

#### Command-Line Information

**Property:** `PackagePostfix`

**Type:** `string`

**Value:** A string that is legal in a VHDL package file name

**Default:** `'_pkg'`

#### See Also

`PackagePostfix`

## Reserved word postfix

Specify a string to append to value names, postfix values, or labels that are VHDL or Verilog reserved words.

### Settings

**Default:** `_rsvd`

The reserved word postfix is applied to identifiers (for entities, signals, constants, or other model elements) that conflict with VHDL or Verilog reserved words. For example, if your generating model contains a signal named `mod`, the coder adds the postfix `_rsvd` to form the name `mod_rsrd`.

### Command-Line Information

**Property:** `ReservedWordPostfix`

**Type:** `string`

**Default:** `'_rsrd'`

### See Also

`ReservedWordPostfix`

### Split entity and architecture

Specify whether generated VHDL entity and architecture code is written to a single VHDL file or to separate files.

#### Settings

**Default:** Off



On

VHDL entity and architecture definitions are written to separate files.



Off

VHDL entity and architecture code is written to a single VHDL file.

#### Tips

The names of the entity and architecture files derive from the base file name (as specified by the generating model or subsystem name). By default, postfix strings identifying the file as an entity (`_entity`) or architecture (`_arch`) are appended to the base file name. You can override the default and specify your own postfix string.

For example, instead of all generated code residing in `MyFIR.vhd`, you can specify that the code reside in `MyFIR_entity.vhd` and `MyFIR_arch.vhd`.

#### Dependencies

This option is enabled when the target language (specified by the **Language** option) is Verilog.

Selecting this option enables the following parameters:

- **Split entity file postfix**
- **Split architecture file postfix**

#### Command-Line Information

**Property:** `SplitEntityArch`

**Type:** `string`

**Value:** `'on' | 'off'`



**Default:** 'off'

**See Also**

SplitEntityArch

### **Split entity file postfix**

Enter a string to be appended to the model name to form the name of a generated VHDL entity file.

#### **Settings**

Default: `_entity`

#### **Dependencies**

This parameter is enabled by **Split entity and architecture**.

#### **Command-Line Information**

Property: `SplitEntityFilePostfix`

Type: `string`

Default: `'_entity'`

#### **See Also**

`SplitEntityFilePostfix`

## Split arch file postfix

Enter a string to be appended to the model name to form the name of a generated VHDL architecture file.

### Settings

Default: `_arch`

### Dependency

This parameter is enabled by **Split entity and architecture**.

### Command-Line Information

Property: `SplitArchFilePostfix`

Type: `string`

Default: `'_arch'`

### See Also

`SplitArchFilePostfix`

### **Clocked process postfix**

Specify a string to append to HDL clock process names.

#### **Settings**

**Default:** `_process`

The coder uses process blocks for register operations. The label for each of these blocks is derived from a register name and the postfix `_process`. For example, the coder derives the label `delay_pipeline_process` from the register name `delay_pipeline` and the default postfix string `_process`.

#### **Command-Line Information**

**Property:** `ClockProcessPostfix`

**Type:** `string`

**Default:** `'_process'`

#### **See Also**

`ClockProcessPostfix`

## Enable prefix

Specify the base name string for internal clock enables and other flow control signals in generated code.

### Settings

**Default:** 'enb'

Where only a single clock enable is generated, **Enable prefix** specifies the signal name for the internal clock enable signal.

In some cases, multiple clock enables are generated (for example, when a cascade block implementation for certain blocks is specified). In such cases, **Enable prefix** specifies a base signal name for the first clock enable that is generated. For other clock enable signals, numeric tags are appended to **Enable prefix** to form unique signal names. For example, the following code fragment illustrates two clock enables that were generated when **Enable prefix** was set to 'test\_clk\_enable':

```
COMPONENT mysys_tc
  PORT( clk           : IN   std_logic;
        reset        : IN   std_logic;
        clk_enable    : IN   std_logic;
        test_clk_enable : OUT  std_logic;
        test_clk_enable_5_1_0 : OUT  std_logic
  );
END COMPONENT;
```

### Command-Line Information

**Property:** EnablePrefix

**Type:** string

**Default:** 'enb'

### See Also

EnablePrefix

### **Pipeline postfix**

Specify string to append to names of input or output pipeline registers generated for pipelined block implementations.

#### **Settings**

**Default:** `'_pipe'`

You can specify a generation of input and/or output pipeline registers for selected blocks. The **Pipeline postfix** option defines a string that the coder appends to names of input or output pipeline registers.

#### **Command-Line Information**

**Property:** PipelinePostfix

**Type:** string

**Default:** `'_pipe'`

#### **See Also**

PipelinePostfix

## Complex real part postfix

Specify string to append to real part of complex signal names.

### Settings

**Default:** `'_re'`

Enter a string to be appended to the names generated for the real part of complex signals.

### Command-Line Information

**Property:** `ComplexRealPostfix`

**Type:** `string`

**Default:** `'_re'`

### See Also

`ComplexRealPostfix`

## **Complex imaginary part postfix**

Specify string to append to imaginary part of complex signal names.

### **Settings**

**Default:** `'_im'`

Enter a string to be appended to the names generated for the imaginary part of complex signals.

### **Command-Line Information**

**Property:** `ComplexImagPostfix`

**Type:** `string`

**Default:** `'_im'`

### **See Also**

`ComplexImagPostfix`



## Input data type

Specify the HDL data type for the model's input ports.

### Settings

For VHDL, the options are:

**Default:** `std_logic_vector`

`std_logic_vector`

Specifies VHDL type `STD_LOGIC_VECTOR`.

`signed/unsigned`

Specifies VHDL type `SIGNED` or `UNSIGNED`.

For Verilog, the options are:

**Default:** `wire`

In generated Verilog code, the data type for all ports is `'wire'`. Therefore, **Input data type** is disabled when the target language is Verilog.

### Dependency

This option is enabled when the target language (specified by the **Language** option) is VHDL.

### Command-Line Information

**Property:** `InputType`

**Type:** `string`

**Value:** (for VHDL) `'std_logic_vector'` | `'signed/unsigned'`  
(for Verilog) `'wire'`

**Default:** (for VHDL) `'std_logic_vector'`  
(for Verilog) `'wire'`

### See Also

`InputType`

### Output data type

Specify the HDL data type for the model's output ports.

#### Settings

For VHDL, the options are:

**Default:** Same as input data type

Same as input data type

Specifies that output ports have the same type specified by **Input data type**.

`std_logic_vector`

Specifies VHDL type `STD_LOGIC_VECTOR`.

`signed/unsigned`

Specifies VHDL type `SIGNED` or `UNSIGNED`.

For Verilog, the options are:

**Default:** `wire`

In generated Verilog code, the data type for all ports is `'wire'`. Therefore, **Output data type** is disabled when the target language is Verilog.

#### Dependency

This option is enabled when the target language (specified by the **Language** option) is VHDL.

#### Command-Line Information

**Property:** `OutputType`

**Type:** `string`

**Value:** (for VHDL) `'std_logic_vector'` | `'signed/unsigned'`  
(for Verilog) `'wire'`

**Default:** If the property is left unspecified, output ports have the same type specified by `InputType`.

**See Also**

OutputType

## **Clock enable output port**

Specify the name for the generated clock enable output.

### **Settings**

**Default:** `ce_out`

A clock enable output is generated when the design requires one.

### **Command-Line Information**

**Property:** `ClockEnableOutputPort`

**Type:** `string`

**Default:** `'ce_out'`

### **See Also**

`ClockEnableOutputPort`

## Balance delays

Enable delay balancing.

### Settings

**Default:** On



On

If the coder detects introduction of new delays along one path, matching delays are inserted on the other paths. When delay balancing is enabled, the generated model is functionally equivalent to the original model.



Off

The latency along signal paths might not be balanced, and the generated model might not be functionally equivalent to the original model.

### Command-Line Information

**Property:** BalanceDelays

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'on'

### See Also

Delay Balancing

### Hierarchical distributed pipelining

Specify that retiming be applied across a subsystem hierarchy.

#### Settings

**Default:** Off

- On  
Enable retiming across a subsystem hierarchy. The coder applies retiming hierarchically down, until it reaches a subsystem where **DistributedPipelining** is off.
- Off  
Distribute pipelining only within a subsystem.

#### Command-Line Information

**Property:** HierarchicalDistPipelining

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'off'

#### See Also

- Effects of Hierarchical Distributed Pipelining
- HierarchicalDistPipelining
- DistributedPipelining

## Optimize timing controller

Optimize timing controller entity for speed and code size by implementing separate counters per rate.

### Settings

**Default:** On



On

The coder generates multiple counters (one counter for each rate in the model) in the timing controller code. The benefit of this optimization is that it generates faster logic, and the size of the generated code is usually much smaller.



Off

The coder generates a timing controller that uses one counter to generate all rates in the model.

### Tip

A timing controller code file is generated if required by the design, for example:

- When code is generated for a multirate model
- When a cascade block implementation for certain blocks is specified

This file contains a module defining timing signals (clock, reset, external clock enable inputs and clock enable output) in a separate entity or module. In a multirate model, the timing controller entity generates the required rates from a single master clock using one or more counters and multiple clock enables.

The timing controller name derives from the name of the subsystem that is selected for code generation (the DUT), and the current value of the string property `TimingControllerPostfix`. For example, if the name of your DUT is `my_test`, in the default case the coder adds the `TimingControllerPostfix` `_tc` to form the timing controller name `my_test_tc`.

### Command-Line Information

**Property:** `OptimizeTimingController`

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'on'

**See Also**

OptimizeTimingController



## Minimize clock enables

Omit generation of clock enable logic for single-rate designs.

### Settings

**Default:** Off

On

For single-rate models, omit generation of clock enable logic wherever possible. The following VHDL code example does not define or examine a clock enable signal. When the clock signal (clk) goes high, the current signal value is output.

```
Unit_Delay_process : PROCESS (clk, reset)
BEGIN
    IF reset = '1' THEN
        Unit_Delay_out1 <= to_signed(0, 32);
    ELSIF clk'EVENT AND clk = '1' THEN
        Unit_Delay_out1 <= In1_signed;
    END IF;
END PROCESS Unit_Delay_process;
```

Off

Generate clock enable logic. The following VHDL code extract represents a register with a clock enable (enb)

```
Unit_Delay_process : PROCESS (clk, reset)
BEGIN
    IF reset = '1' THEN
        Unit_Delay_out1 <= to_signed(0, 32);
    ELSIF clk'EVENT AND clk = '1' THEN
        IF enb = '1' THEN
            Unit_Delay_out1 <= In1_signed;
        END IF;
    END IF;
END PROCESS Unit_Delay_process;
```

### Exceptions

In some cases, the coder emits clock enables even when **Minimize clock enables** is selected. These cases are:

- Registers inside Enabled, State-Enabled, and Triggered subsystems.
- Multirate models.
- The coder always emits clock enables for the following blocks:
  - commseqgen2/PN Sequence Generator
  - dspsigops/NCO
  - dspsrcs4/Sine Wave
  - hdl demolib/HDL FFT
  - built-in/DiscreteFIR
  - dspmlti4/CIC Decimation
  - dspmlti4/CIC Interpolation
  - dspmlti4/FIR Decimation
  - dspmlti4/FIR Interpolation
  - dspadpt3/LMS Filter
  - dsparch4/Biquad Filter
  - dsparch4/Digital Filter

### Command-Line Information

**Property:** MinimizeClockEnables

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'off'

### See Also

MinimizeClockEnables

## RAM mapping threshold (bits)

Specify the minimum RAM size for mapping to block RAMs instead of to registers.

### Settings

**Default:** 256

The RAM mapping threshold must be an integer greater than or equal to zero. The coder uses the threshold to determine whether or not to map the following elements to block RAMs instead of to registers:

- Delay blocks
- Persistent arrays in MATLAB Function blocks

### Command-Line Information

**Property:** RAMMappingThreshold

**Type:** integer

**Value:** integer greater than or equal to 0

**Default:** 256

### See Also

- RAMMappingThreshold
- UseRAM
- MapPersistentVarsToRAM

### Represent constant values by aggregates

Specify whether constants in VHDL code are represented by aggregates, including constants that are less than 32 bits.

#### Settings

**Default:** Off



On

The coder represents constants as aggregates. The following VHDL constant declarations show a scalar less than 32 bits represented as an aggregate:

```
GainFactor_gainparam <= (14 => '1', OTHERS => '0');
```



Off

The coder represents constants less than 32 bits as scalars and constants greater than or equal to 32 bits as aggregates. The following VHDL code was generated by default for a value less than 32 bits:

```
GainFactor_gainparam <= to_signed(16384, 16);
```

#### Dependencies

This option is enabled when the target language (specified by the **Language** option) is VHDL.

#### Command-Line Information

**Property:** UseAggregatesForConst

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'off'

#### See Also

UseAggregatesForConst

## Use rising\_edge for registers

Specify whether or not generated code uses the VHDL `rising_edge` function to check for rising edges when operating on registers.

### Settings

**Default:** Off



On

Generated code uses the VHDL `rising_edge` function to check for rising edges when operating on registers.



Off

Generated code checks for clock events when operating on registers.

### Dependencies

This option is enabled when the target language (specified by the **Language** option) is VHDL.

### Command-Line Information

**Property:** `UseRisingEdge`

**Type:** `string`

**Value:** `'on' | 'off'`

**Default:** `'off'`

### See Also

`UseRisingEdge`

### Loop unrolling

Specify whether VHDL FOR and GENERATE loops are unrolled and omitted from generated VHDL code.

#### Settings

**Default:** Off



On

Unroll and omit FOR and GENERATE loops from the generated VHDL code. (In Verilog code, loops are always unrolled.)



Off

Include FOR and GENERATE loops in the generated VHDL code.

#### Tip

If you are using an electronic design automation (EDA) tool that does not support GENERATE loops, select this option to omit loops from your generated VHDL code.

#### Dependency

This option is enabled when the target language (specified by the **Language** option) is VHDL.

#### Command-Line Information

**Property:** LoopUnrolling

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'off'

#### See Also

LoopUnrolling

## Cast before sum

Specify whether operands in addition and subtraction operations are type cast to the result type before executing the operation.

### Settings

**Default:** On



On

Typecast input values in addition and subtraction operations to the result type before operating on the values.



Off

Preserve the types of input values during addition and subtraction operations and then convert the result to the result type.

### Command-Line Information

**Property:** CastBeforeSum

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'on'

### See Also

CastBeforeSum

### Use Verilog ``timescale` directives

Specify use of compiler ``timescale` directives in generated Verilog code.

#### Settings

**Default:** On



On

Use compiler ``timescale` directives in generated Verilog code.



Off

Suppress the use of compiler ``timescale` directives in generated Verilog code.

#### Tip

The ``timescale` directive provides a way of specifying different delay values for multiple modules in a Verilog file. This setting does not affect the generated test bench.

#### Dependency

This option is enabled when the target language (specified by the **Language** option) is Verilog.

#### Command-Line Information

**Property:** UseVerilogTimescale

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'on'

#### See Also

UseVerilogTimescale



## Inline VHDL configuration

Specify whether generated VHDL code includes inline configurations.

### Settings

**Default:** On



On

Include VHDL configurations in files that instantiate a component.



Off

Suppress the generation of configurations and require user-supplied external configurations. Use this setting if you are creating your own VHDL configuration files.

### Tip

HDL configurations can be either inline with the rest of the VHDL code for an entity or external in separate VHDL source files. By default, the coder includes configurations for a model within the generated VHDL code. If you are creating your own VHDL configuration files, suppress the generation of inline configurations.

### Dependencies

This option is enabled when the target language (specified by the **Language** option) is VHDL.

### Command-Line Information

**Property:** InlineConfigurations

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'on'

### See Also

InlineConfigurations

### Concatenate type safe zeros

Specify use of syntax for concatenated zeros in generated VHDL code.

#### Settings

**Default:** On



On

Use the type-safe syntax, '0' & '0', for concatenated zeros. Typically, this syntax is preferred.



Off

Use the syntax "000000..." for concatenated zeros. This syntax can be easier to read and more compact, but it can lead to ambiguous types.

#### Dependencies

This option is enabled when the target language (specified by the **Language** option) is VHDL.

#### Command-Line Information

**Property:** SafeZeroConcat

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'on'

#### See Also

SafeZeroConcat

## Emit time/date stamp in header

Specify whether or not to include time and date information in the generated HDL file header.

### Settings

Default: On



On

Include time/date stamp in the generated HDL file header.

```
-----  
--  
-- File Name:hdlsrc\symmetric_fir.vhd  
-- Created: 2011-02-14 07:21:36  
--
```



Off

Omit time/date stamp in the generated HDL file header.

```
-----  
--  
-- File Name:hdlsrc\symmetric_fir.vhd  
--
```

By omitting the time/date stamp in the file header, you can more easily determine if two HDL files contain identical code. You can also avoid redundant revisions of the same file when checking in HDL files to a source code management (SCM) system.

### Command-Line Information

**Property:** DateComment

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'on'

### See Also

DateComment

### Scalarize vector ports

Flatten vector ports into a structure of scalar ports in VHDL code

#### Settings

**Default:** Off



On

When generating code for a vector port, generate a structure of scalar ports.



Off

When generating code for a vector port, generate a type definition and port declaration for the vector port.

#### Dependencies

This option is enabled when the target language (specified by the **Language** option) is VHDL.

#### Command-Line Information

**Property:** ScalarizePorts

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'off'

#### See Also

ScalarizePorts

## Minimize intermediate signals

Specify whether to optimize HDL code for debuggability or code coverage.

### Settings

**Default:** Off



Optimize for code coverage by minimizing intermediate signals. For example, suppose that the generated code with this setting *off* is:

```
const3 <= to_signed(24, 7);  
subtractor_sub_cast <= resize(const3, 8);  
subtractor_sub_cast_1 <= resize(delayout, 8);  
subtractor_sub_temp <= subtractor_sub_cast - subtractor_sub_cast_1;
```

With this setting *on*, the coder optimizes the output to:

```
subtractor_sub_temp <= 24 - (resize(delayout, 8));
```

The coder removes the intermediate signals `const3`, `subtractor_sub_cast`, and `subtractor_sub_cast_1`.



Optimize for debuggability by preserving intermediate signals.

### Command-Line Information

**Property:** MinimizeIntermediateSignals

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'off'

### See Also

MinimizeIntermediateSignals

### Include requirements in block comments

Enable or disable generation of requirements comments as comments in code or code generation reports

#### Settings

**Default:** On



On

If the model contains requirements comments, include them as comments in code or code generation reports. See “Requirements Comments and Hyperlinks” on page 14-28.



Off

Do not include requirements as comments in code or code generation reports.

#### Command-Line Information

**Property:** RequirementComments

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'on'

#### See Also

RequirementComments

## Inline MATLAB Function block code

Inline HDL code for MATLAB Function blocks.

### Settings

**Default:** Off



On

Inline HDL code for MATLAB Function blocks to avoid instantiation of code for custom blocks.



Off

Instantiate HDL code for MATLAB Function blocks and do not inline.

### Command-Line Information

**Property:** InlineMATLABBlockCode

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'off'

### See Also

InlineMATLABBlockCode

## Generate parameterized HDL code from masked subsystem

Generate reusable HDL code for subsystems with the same tunable mask parameters, but with different values.

### Settings

Default: Off



On

Generate one HDL file for multiple masked subsystems with different values for tunable mask parameters. The coder automatically detects atomic subsystems with tunable mask parameters that are shareable.

Inside the subsystem, you can use the mask parameter only in the following blocks and parameters.

Block	Parameter	Limitation
Constant	<b>Constant value</b> on the <b>Main</b> tab of the dialog box	None
Gain	<b>Gain</b> on the <b>Main</b> tab of the dialog box	<b>Parameter data type</b> must be the same for all Gain blocks.



Off

Generate a separate HDL file for each masked subsystem.

### Command-Line Information

**Property:** MaskParameterAsGeneric

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'off'



**See Also**

MaskParameterAsGeneric

**RAM Architecture**

Select RAM architecture with clock enable, or without clock enable, for all RAMs in DUT subsystem.

**Settings**

**Default:** RAM with clock enable

Select one of the following options from the menu:

- RAM with clock enable: Generate RAMs with clock enable.
- Generic RAM without clock enable: Generate RAMs without clock enable.

**Command-Line Information**

**Property:** RAMArchitecture

**Type:** string

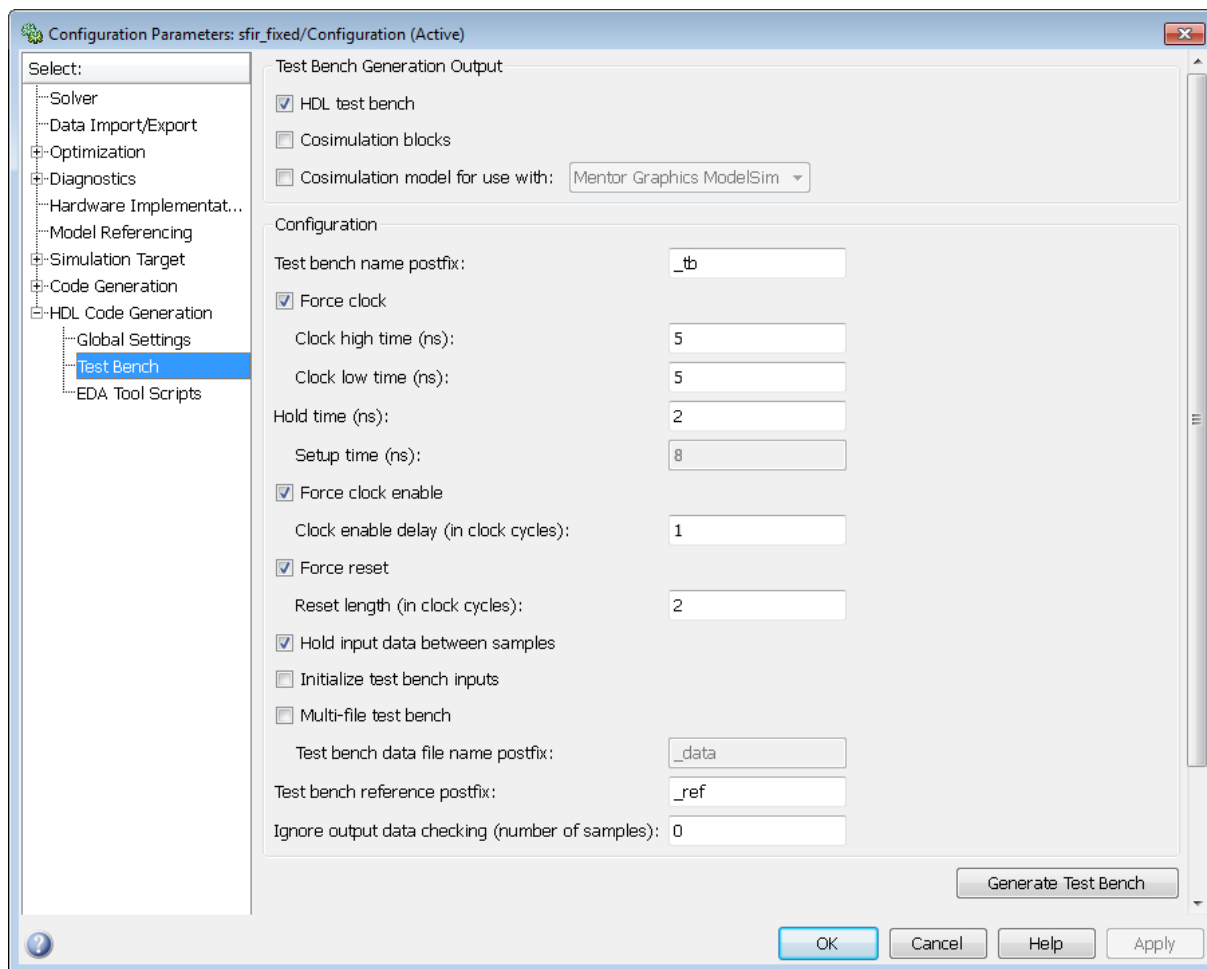
**Value:** 'WithClockEnable' | 'WithoutClockEnable'

**Default:** 'WithClockEnable'

**See Also**

RAMArchitecture

## HDL Code Generation Pane: Test Bench



### In this section...

"Test Bench Overview" on page 7-74

"HDL test bench" on page 7-75

"Cosimulation blocks" on page 7-76

**In this section...**

“Cosimulation model for use with:” on page 7-78

“Test bench name postfix” on page 7-79

“Force clock” on page 7-80

“Clock high time (ns)” on page 7-81

“Clock low time (ns)” on page 7-82

“Hold time (ns)” on page 7-83

“Setup time (ns)” on page 7-84

“Force clock enable” on page 7-85

“Clock enable delay (in clock cycles)” on page 7-86

“Force reset” on page 7-88

“Reset length (in clock cycles)” on page 7-89

“Hold input data between samples” on page 7-91

“Initialize test bench inputs” on page 7-92

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“Test bench reference postfix” on page 7-95

“Test bench data file name postfix” on page 7-96

“Ignore output data checking (number of samples)” on page 7-97

### **Test Bench Overview**

The **Test Bench** pane lets you set options that determine characteristics of generated test bench code.

### **Generate Test Bench Button**

The **Generate Test Bench** button initiates test bench generation for the system selected in the **Generate HDL for** menu. See also `makehdltb`.

## HDL test bench

Enable or disable HDL test bench generation.

### Settings

**Default:** On



On

Enable generation of HDL test bench code that can interface to the DUT.



Off

Suppress generation of HDL test bench code.

### Dependencies

This check box enables the options in the **Configuration** section of the **Test Bench** pane.

### See Also

Generating VHDL Test Bench Code

### Cosimulation blocks

Generate a model containing HDL Cosimulation block(s) for use in testing the DUT.

#### Settings

**Default:** Off



On

When you select this option, the coder generates and opens a model that contains one or more HDL Cosimulation blocks. The coder generates cosimulation blocks if your installation includes one or more of the following:

- HDL Verifier™ for use with Mentor Graphics® ModelSim®
- HDL Verifier for use with Cadence Incisive®

The coder configures the generated HDL Cosimulation blocks to conform to the port and data type interface of the DUT selected for code generation. By connecting an HDL Cosimulation block to your model in place of the DUT, you can cosimulate your design with the desired simulator.



Off

Do not generate HDL Cosimulation blocks.

### Dependencies

This check box enables the other options in the **Configuration** section of the **Test Bench** pane.

### Command-Line Information

**Property:** GenerateCoSimBlock

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'off'

**See Also**

GenerateCoSimBlock

### Cosimulation model for use with:

Generate model containing HDL Cosimulation block for cosimulation

#### Settings

**Default:** Off

On

Selecting this option enables the dropdown menu to the right of the check box. Select one of the following options from the menu:

- **Mentor Graphics ModelSim:** This option is the default. If your installation includes HDL Verifier for use with Mentor Graphics ModelSim, the coder generates and opens a Simulink model that contains an HDL Cosimulation block for Mentor Graphics ModelSim.
- **Cadence Incisive:** If your installation includes HDL Verifier for use with Cadence Incisive, the coder generates and opens a Simulink model that contains an HDL Cosimulation block for Cadence Incisive.

Off

Do not generate HDL Cosimulation model.

#### Command-Line Information

**Property:** GenerateCosimModel

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'off'

#### See Also

GenerateCoSimModel



## Test bench name postfix

Specify a suffix appended to the test bench name.

### Settings

**Default:** `_tb`

For example, if the name of your DUT is `my_test`, the coder adds the default postfix `_tb` to form the name `my_test_tb`.

### Command-Line Information

**Property:** `TestBenchPostFix`

**Type:** `string`

**Default:** `'_tb'`

### See Also

`TestBenchPostFix`

### Force clock

Specify whether the test bench forces clock input signals.

#### Settings

**Default:** On



On

The test bench forces the clock input signals. When this option is selected, the clock high and low time settings control the clock waveform.



Off

A user-defined external source forces the clock input signals.

#### Dependencies

This property enables the **Clock high time** and **Clock high time** options.

#### Command-Line Information

**Property:** ForceClock

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'on'

#### See Also

ForceClock

## Clock high time (ns)

Specify the period, in nanoseconds, during which the test bench drives clock input signals high (1).

### Settings

**Default:** 5

The **Clock high time** and **Clock low time** properties define the period and duty cycle for the clock signal. Using the defaults, the clock signal is a square wave (50% duty cycle) with a period of 10 ns.

### Dependency

This parameter is enabled when **Force clock** is selected.

### Command-Line Information

**Property:** ClockHighTime

**Type:** integer

**Value:** A positive integer

**Default:** 5

### See Also

ClockHighTime

### **Clock low time (ns)**

Specify the period, in nanoseconds, during which the test bench drives clock input signals low (0).

#### **Settings**

**Default:** 5

The **Clock high time** and **Clock low time** properties define the period and duty cycle for the clock signal. Using the defaults, the clock signal is a square wave (50% duty cycle) with a period of 10 ns.

#### **Dependency**

This parameter is enabled when **Force clock** is selected.

#### **Command-Line Information**

**Property:** ClockLowTime

**Type:** integer

**Value:** A positive integer

**Default:** 5

#### **See Also**

ClockLowTime

## Hold time (ns)

Specify a hold time, in nanoseconds, for input signals and forced reset input signals.

### Settings

**Default:** 2 (given the default clock period of 10 ns)

The hold time defines the number of nanoseconds that reset input signals and input data are held past the clock rising edge. The hold time is expressed as a positive integer or double (with a maximum of 6 significant digits after the decimal point).

### Tips

- The specified hold time must be less than the clock period (specified by the **Clock high time** and **Clock low time** properties).
- This option applies to reset input signals only if **Force reset** is selected.

### Command-Line Information

**Property:** HoldTime

**Type:** integer

**Value:** A positive integer

**Default:** 2

### See Also

HoldTime

### **Setup time (ns)**

Display setup time for data input signals.

### **Settings**

**Default:** None

This is a display-only field, showing a value computed as (clock period - HoldTime) in nanoseconds.

### **Dependency**

The value displayed in this field depends on the clock rate and the values of the **Hold time** property.

### **Command-Line Information**

Because this is a display-only field, a corresponding command-line property does not exist.

### **See Also**

HoldTime

## Force clock enable

Specify whether the test bench forces clock enable input signals.

### Settings

**Default:** On



On

The test bench forces the clock enable input signals to active-high (1) or active-low (0), depending on the setting of the clock enable input value.



Off

A user-defined external source forces the clock enable input signals.

### Dependencies

This property enables the **Clock enable delay (in clock cycles)** option.

### Command-Line Information

**Property:** ForceClockEnable

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'on'

### See Also

ForceClockEnable

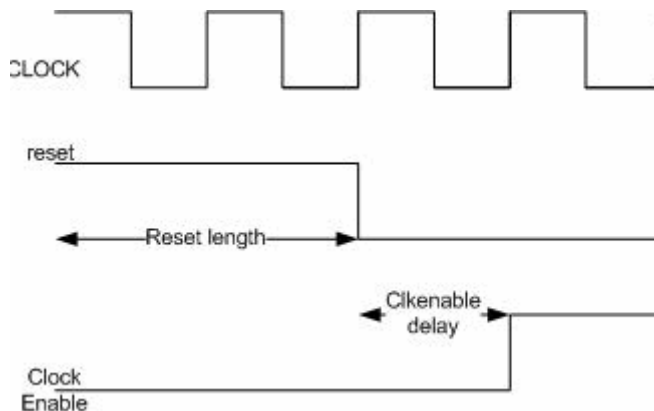
## Clock enable delay (in clock cycles)

Define elapsed time (in clock cycles) between deassertion of reset and assertion of clock enable.

### Settings

**Default:** 1

The **Clock enable delay (in clock cycles)** property defines the number of clock cycles elapsed between the time the reset signal is deasserted and the time the clock enable signal is first asserted. In the figure below, the reset signal (active-high) deasserts after 2 clock cycles and the clock enable asserts after a clock enable delay of 1 cycle (the default).



### Dependency

This parameter is enabled when **Force clock enable** is selected.

### Command-Line Information

**Property:** TestBenchClockEnableDelay

**Type:** integer

**Default:** 1



**See Also**

TestBenchClockEnableDelay

### Force reset

Specify whether the test bench forces reset input signals.

#### Settings

**Default:** On



On

The test bench forces the reset input signals.



Off

A user-defined external source forces the reset input signals.

#### Tips

If you select this option, you can use the **Hold time** option to control the timing of a reset.

#### Command-Line Information

**Property:** ForceReset

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'on'

#### See Also

ForceReset

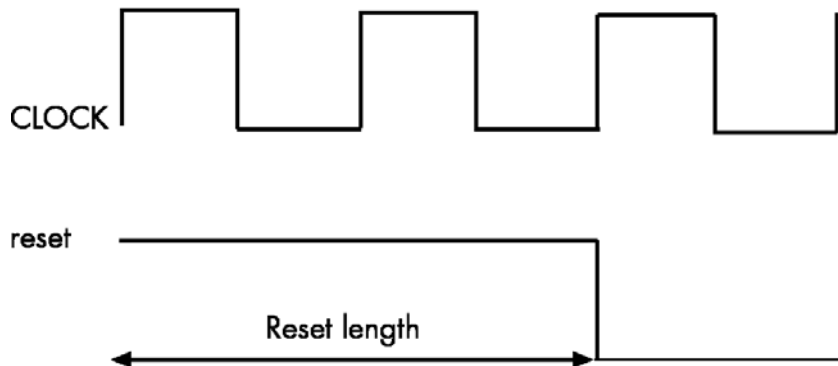
## Reset length (in clock cycles)

Define length of time (in clock cycles) during which reset is asserted.

### Settings

**Default:** 2

The **Reset length (in clock cycles)** property defines the number of clock cycles during which reset is asserted. **Reset length (in clock cycles)** must be an integer greater than or equal to 0. The following figure illustrates the default case, in which the reset signal (active-high) is asserted for 2 clock cycles.



### Dependency

This parameter is enabled when **Force reset** is selected.

### Command-Line Information

**Property:** Resetlength  
**Type:** integer  
**Default:** 2

**See Also**

ResetLength

## Hold input data between samples

Specify how long subrate signal values are held in valid state.

### Settings

**Default:** On



On

Data values for subrate signals are held in a valid state across N base-rate clock cycles, where N is the number of base-rate clock cycles that elapse per subrate sample period. (N is  $\geq 2$ .)



Off

Data values for subrate signals are held in a valid state for only one base-rate clock cycle. For the subsequent base-rate cycles, data is in an unknown state (expressed as 'X') until leading edge of the next subrate sample period.

### Tip

In most cases, the default (On) is the best setting for **Hold input data between samples**. This setting matches the behavior of a Simulink simulation, in which subrate signals are held valid through each base-rate clock period.

In some cases (for example modeling memory or memory interfaces), it is desirable to clear **Hold input data between samples**. In this way you can obtain diagnostic information about when data is in an invalid ('X') state.

### Command-Line Information

**Property:** HoldInputDataBetweenSamples

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'on'

### See Also

HoldInputDataBetweenSamples

## Initialize test bench inputs

Specify initial value driven on test bench inputs before data is asserted to DUT.

### Settings

**Default:** Off



On

Initial value driven on test bench inputs is '0'.



Off

Initial value driven on test bench inputs is 'X' (unknown).

### Command-Line Information

**Property:** InitializeTestBenchInputs

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'off'

### See Also

InitializeTestBenchInputs

## Multi-file test bench

Divide generated test bench into helper functions, data, and HDL test bench code files.

### Settings

**Default:** Off



On

Write separate files for test bench code, helper functions, and test bench data. The file names are derived from the name of the DUT, the **Test bench name postfix** property, and the **Test bench data file name postfix** property as follows:

*DUTname\_TestBenchPostfix\_TestBenchDataPostfix*

For example, if the DUT name is `symmetric_fir`, and the target language is VHDL, the default test bench file names are:

- `symmetric_fir_tb.vhd`: test bench code
- `symmetric_fir_tb_pkg.vhd`: helper functions package
- `symmetric_fir_tb_data.vhd`: data package

If the DUT name is `symmetric_fir` and the target language is Verilog, the default test bench file names are:

- `symmetric_fir_tb.v`: test bench code
- `symmetric_fir_tb_pkg.v`: helper functions package
- `symmetric_fir_tb_data.v`: test bench data



Off

Write a single test bench file containing the HDL test bench code, helper functions, and test bench data.

### Dependency

When this property is selected, **Test bench data file name postfix** is enabled.

### **Command-Line Information**

**Property:** MultifileTestBench

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'off'

### **See Also**

MultifileTestBench



## Test bench reference postfix

Specify a string appended to names of reference signals generated in test bench code.

### Settings

**Default:** `'_ref'`

Reference signal data is represented as arrays in the generated test bench code. The string specified by **Test bench reference postfix** is appended to the generated signal names.

### Command-Line Information

**Parameter:** `TestBenchReferencePostFix`

**Type:** `string`

**Default:** `'_ref'`

### See Also

`TestBenchReferencePostFix`

### Test bench data file name postfix

Specify suffix added to test bench data file name when generating multi-file test bench.

#### Settings

**Default:** '\_data'

The coder applies the **Test bench data file name postfix** string only when generating a multi-file test bench (i.e., when **Multi-file test bench** is selected).

For example, if the name of your DUT is `my_test`, and **Test bench name postfix** has the default value `_tb`, the coder adds the postfix `_data` to form the test bench data file name `my_test_tb_data`.

#### Dependency

This parameter is enabled by **Multi-file test bench**.

#### Command-Line Information

**Property:** TestBenchDataPostFix

**Type:** string

**Default:** '\_data'

#### See Also

TestBenchDataPostFix

## Ignore output data checking (number of samples)

Specify number of samples during which output data checking is suppressed.

### Settings

**Default:** 0

The value must be a positive integer.

When the value N of **Ignore output data checking (number of samples)** is greater than zero, the test bench suppresses output data checking for the first N output samples after the clock enable output (`ce_out`) is asserted.

When using pipelined block implementations, output data may be in an invalid state for some number of samples. To avoid spurious test bench errors, determine this number and set **Ignore output data checking (number of samples)** accordingly.

Be careful to specify N as a number of samples, not as a number of clock cycles. For a single-rate model, these are equivalent, but they are not equivalent for a multirate model.

You should use **Ignore output data checking (number of samples)** in cases where there is a state (register) initial condition in the HDL code that does not match the Simulink state, including the following specific cases:

- When you specify the `'DistributedPipelining', 'on'` parameter for the MATLAB Function block (see “Distributed Pipeline Insertion for MATLAB Function Blocks” on page 17-42)
- When you specify the `{ 'ResetType', 'None' }` parameter for the following block types:
  - `commcnvintrlv2/Convolutional Deinterleaver`
  - `commcnvintrlv2/Convolutional Interleaver`
  - `commcnvintrlv2/General Multiplexed Deinterleaver`
  - `commcnvintrlv2/General Multiplexed Interleaver`
  - `dpsigops/Delay`

- simulink/Additional Math & Discrete/Additional Discrete/Unit Delay Enabled
- simulink/Commonly Used Blocks/Unit Delay
- simulink/Discrete/Delay
- simulink/Discrete/Memory
- simulink/Discrete/Tapped Delay
- simulink/User-Defined Functions/MATLAB Function
- sflib/Chart
- sflib/Truth Table
- When generating a black box interface to existing manually written HDL code

### Command-Line Information

**Property:** IgnoreDataChecking

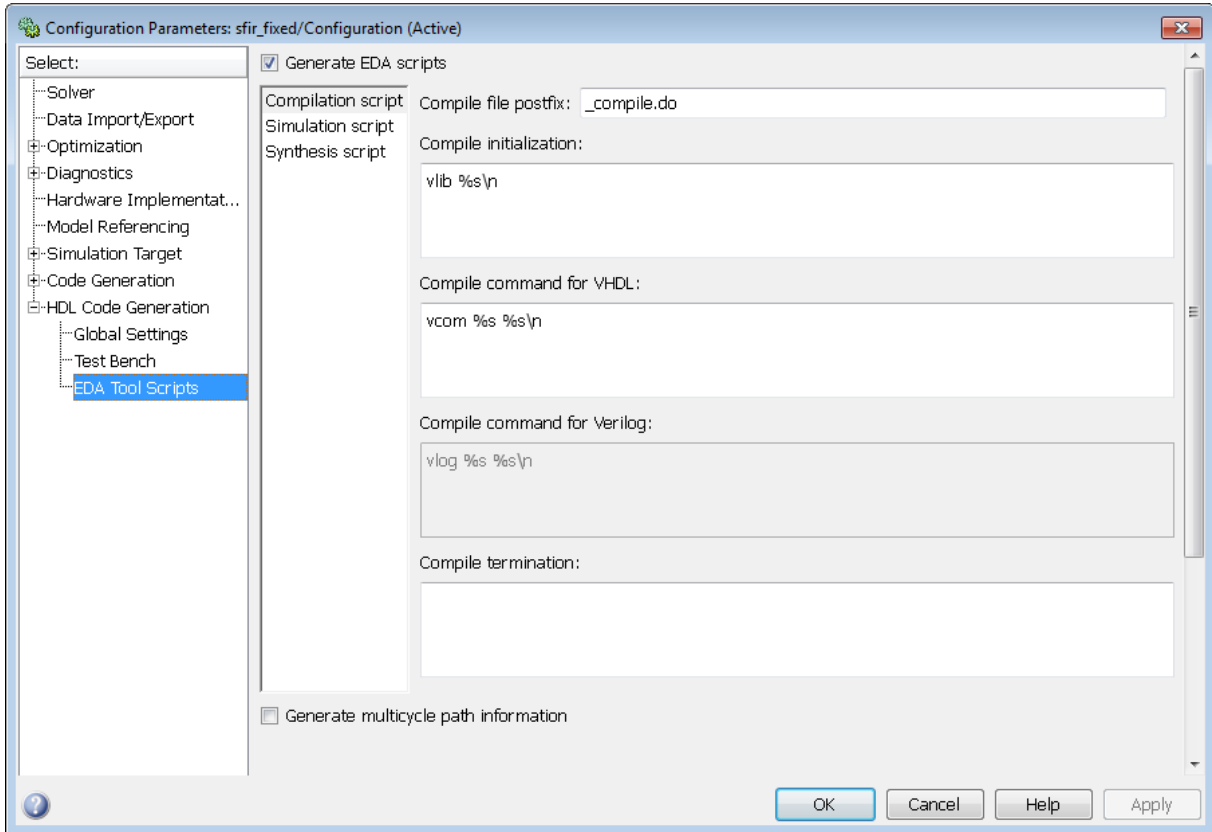
**Type:** integer

**Default:** 0

### See Also

IgnoreDataChecking

## HDL Code Generation Pane: EDA Tool Scripts



### In this section...

“EDA Tool Scripts Overview” on page 7-101

“Generate EDA scripts” on page 7-102

“Generate multicycle path information” on page 7-103

“Compile file postfix” on page 7-104

“Compile initialization” on page 7-105

“Compile command for VHDL” on page 7-106

**In this section...**

“Compile command for Verilog” on page 7-107

“Compile termination” on page 7-108

“Simulation file postfix” on page 7-109

“Simulation initialization” on page 7-110

“Simulation command” on page 7-111

“Simulation waveform viewing command” on page 7-112

“Simulation termination” on page 7-113

“Choose synthesis tool” on page 7-114

“Synthesis file postfix” on page 7-116

“Synthesis initialization” on page 7-117

“Synthesis command” on page 7-118

“Synthesis termination” on page 7-119

## **EDA Tool Scripts Overview**

The **EDA Tool Scripts** pane lets you set the options that control generation of script files for third-party HDL simulation and synthesis tools.

### Generate EDA scripts

Enable generation of script files for third-party electronic design automation (EDA) tools. These scripts let you compile and simulate generated HDL code and/or synthesize generated HDL code.

#### Settings

**Default:** On



On

Generation of script files is enabled.



Off

Generation of script files is disabled.

#### Command-Line Information

**Parameter:** EDAScriptGeneration

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'on'

#### See Also

- Controlling Script Generation with the EDA Tool Scripts GUI Pane
- EDAScriptGeneration



## Generate multicycle path information

Generate a file that reports multicycle path constraint information.

### Settings

**Default:** Off



On

Generate a text file that reports multicycle path constraint information, for use with synthesis tools.



Off

Do not generate a multicycle path information file.

### Command-Line Information

**Parameter:** MulticyclePathInfo

**Type:** string

**Value:** 'on' | 'off'

**Default:** 'off'

### See Also

- Generating a Multicycle Path Information File
- MulticyclePathInfo

### Compile file postfix

Specify a postfix string appended to the DUT or test bench name to form the compilation script file name.

#### Settings

**Default:** `_compile.do`

For example, if the name of the device under test or test bench is `my_design`, the coder adds the postfix `_compile.do` to form the name `my_design_compile.do`.

#### Command-Line Information

**Property:** `HDLCompileFilePostfix`

**Type:** `string`

**Default:** `'_compile.do'`

#### See Also

- Controlling Script Generation with the EDA Tool Scripts GUI Pane
- `HDLCompileFilePostfix`

## Compile initialization

Specify a format string passed to `fprintf` to write the Init section of the compilation script.

### Settings

**Default:** `vlib %s\n`

The Init phase of the script performs required setup actions, such as creating a design library or a project file.

The argument `%s` is the contents of the `'VHDLLibraryName'` property, which defaults to `'work'`. You can override the default Init string (`'vlib work\n'`) by changing the value of `'VHDLLibraryName'`.

### Command-Line Information

**Property:** `HDLCompileInit`

**Type:** `string`

**Default:** `'vlib %s\n'`

### See Also

- Controlling Script Generation with the EDA Tool Scripts GUI Pane
- `HDLCompileInit`

### Compile command for VHDL

Specify a format string passed to `fprintf` to write the `Cmd` section of the compilation script for VHDL files.

#### Settings

**Default:** `vcom %s %s\n`

The command-per-file phase (`Cmd`) of the script is called iteratively, once per generated HDL file or once per signal. On each call, a different file or signal name is passed in.

The two arguments in the compile command are the contents of the `SimulatorFlags` property and the file name of the current entity or module. To omit the flags, set `SimulatorFlags` to `' '` (the default).

#### Command-Line Information

**Property:** `HDLCompileVHDLCmd`

**Type:** `string`

**Default:** `'vcom %s %s\n'`

#### See Also

- Controlling Script Generation with the EDA Tool Scripts GUI Pane
- `HDLCompileVHDLCmd`

## Compile command for Verilog

Specify a format string passed to `fprintf` to write the `Cmd` section of the compilation script for Verilog files.

### Settings

**Default:** `vlog %s %s\n`

The command-per-file phase (`Cmd`) of the script is called iteratively, once per generated HDL file or once per signal. On each call, a different file or signal name is passed in.

The two arguments in the compile command are the contents of the `SimulatorFlags` property and the file name of the current entity or module. To omit the flags, set `SimulatorFlags` property to `' '` (the default).

### Command-Line Information

**Property:** `HDLCompileVerilogCmd`

**Type:** `string`

**Default:** `'vlog %s %s\n'`

### See Also

- Controlling Script Generation with the EDA Tool Scripts GUI Pane
- `HDLCompileVerilogCmd`

### Compile termination

Specify a format string passed to `fprintf` to write the termination portion of the compilation script.

#### Settings

**Default:** empty string

The termination phase (`Term`) is the final execution phase of the script. One application of this phase is to execute a simulation of HDL code that was compiled in the `Cmd` phase. The `Term` phase does not take arguments.

#### Command-Line Information

**Property:** `HDLCompileTerm`

**Type:** `string`

**Default:** `''`

#### See Also

- Controlling Script Generation with the EDA Tool Scripts GUI Pane
- `HDLCompileTerm`

## Simulation file postfix

Specify a postfix string appended to the DUT or test bench name to form the simulation script file name.

### Settings

**Default:** `_sim.do`

For example, if the name of the device under test or test bench is `my_design`, the coder adds the postfix `_sim.do` to form the name `my_design_sim.do`.

### Command-Line Information

**Property:** `HDLSimFilePostfix`

**Type:** `string`

**Default:** `'_sim.do'`

### See Also

- Controlling Script Generation with the EDA Tool Scripts GUI Pane
- `HDLSimFilePostfix`

### Simulation initialization

Specify a format string passed to `fprintf` to write the initialization section of the simulation script.

#### Settings

**Default:** The default string is

```
['onbreak resume\nonerror resume\n']
```

The `Init` phase of the script performs required setup actions, such as creating a design library or a project file.

#### Command-Line Information

**Property:** HDLSimInit

**Type:** string

**Default:** ['onbreak resume\nonerror resume\n']

#### See Also

- Controlling Script Generation with the EDA Tool Scripts GUI Pane
- HDLSimInit



## Simulation command

Specify a format string passed to `fprintf` to write the simulation command.

### Settings

**Default:** `vsim -novopt work.%s\n`

The implicit argument is the top-level module or entity name.

### Command-Line Information

**Property:** HDLSimCmd

**Type:** string

**Default:** `'vsim -novopt work.%s\n'`

### See Also

- Controlling Script Generation with the EDA Tool Scripts GUI Pane.
- HDLSimCmd

## **Simulation waveform viewing command**

Specify the waveform viewing command written to simulation script.

### **Settings**

**Default:** `add wave sim:%s\n`

The implicit argument is the top-level module or entity name.

### **Command-Line Information**

**Property:** HDLSimViewWaveCmd

**Type:** string

**Default:** 'add wave sim:%s\n'

### **See Also**

- Controlling Script Generation with the EDA Tool Scripts GUI Pane
- HDLSimViewWaveCmd

## Simulation termination

Specify a format string passed to `fprintf` to write the termination portion of the simulation script.

### Settings

**Default:** `run -all\n`

The termination phase (`Term`) is the final execution phase of the script. One application of this phase is to execute a simulation of HDL code that was compiled in the `Cmd` phase. The `Term` phase does not take arguments.

### Command-Line Information

**Property:** `HDLSimTerm`

**Type:** `string`

**Default:** `'run -all\n'`

### See Also

- Controlling Script Generation with the EDA Tool Scripts GUI Pane
- `HDLSimTerm`

### Choose synthesis tool

Enable or disable generation of synthesis scripts, and select the synthesis tool for which the coder generates scripts.

#### Settings

**Default:** None

##### None

When you select None, the coder does not generate a synthesis script. The coder clears and disables the fields in the **Synthesis script** pane.

##### Altera Quartus II

Generate a synthesis script for Altera Quartus II. When you select this option, the coder:

- Enables the fields in the **Synthesis script** pane.
- Sets **Synthesis file postfix** to `_quartus.tcl`
- Fills in the **Synthesis initialization**, **Synthesis command** and **Synthesis termination** fields with TCL script code for the tool.

##### Mentor Graphics Precision

Generate a synthesis script for Mentor Graphics Precision. When you select this option, the coder:

- Enables the fields in the **Synthesis script** pane.
- Sets **Synthesis file postfix** to `_precision.tcl`
- Fills in the **Synthesis initialization**, **Synthesis command** and **Synthesis termination** fields with TCL script code for the tool.

##### Synopsys Synplify Pro

Generate a synthesis script for Synopsys® Synplify Pro®. When you select this option, the coder:

- Enables the fields in the **Synthesis script** pane.
- Sets **Synthesis file postfix** to `_synplify.tcl`
- Fills in the **Synthesis initialization**, **Synthesis command** and **Synthesis termination** fields with TCL script code for the tool.

### Xilinx ISE

Generate a synthesis script for Xilinx ISE. When you select this option, the coder:

- Enables the fields in the **Synthesis script** pane.
- Sets **Synthesis file postfix** to `_ise.tcl`
- Fills in the **Synthesis initialization**, **Synthesis command** and **Synthesis termination** fields with TCL script code for the tool.

### Command-Line Information

**Property:** HDLSynthTool

**Type:** string

**Value:** 'None' | 'ISE' | 'Precision' | 'Quartus' | 'Synplify'

**Default:** 'None'

### See Also

HDLSynthTool

### Synthesis file postfix

Specify a postfix string appended to file name for generated synthesis scripts.

#### Settings

**Default:** None.

Your choice of synthesis tool (from the **Choose synthesis tool** pulldown menu) sets the postfix for generated synthesis file names to one of the following:

```
_ise.tcl  
_precision.tcl  
_quartus.tcl  
_synplify.tcl
```

For example, if the DUT name is `my_design` and the choice of synthesis tool is Synopsys Synplify Pro, the coder adds the postfix `_synplify.tcl` to form the name `my_design_synplify.tcl`.

#### Command-Line Information

**Property:** HDLSynthFilePostfix

**Type:** string

**Default:** none

#### See Also

- Controlling Script Generation with the EDA Tool Scripts GUI Pane
- HDLSynthFilePostfix

## Synthesis initialization

Specify a format string passed to `fprintf` to write the initialization section of the synthesis script.

### Settings

**Default:** none.

Your choice of synthesis tool (from the **Choose synthesis tool** pulldown menu) sets the **Synthesis initialization** string. The default string is a format string passed to `fprintf` to write the `Init` section of the synthesis script. The default string is a synthesis project creation command. The implicit argument is the top-level module or entity name. The content of the string is specific to the selected synthesis tool.

### Command-Line Information

**Property:** HDLSynthInit

**Type:** string

**Default:** none

### See Also

- Controlling Script Generation with the EDA Tool Scripts GUI Pane
- HDLSynthInit

### Synthesis command

Specify a format string passed to `fprintf` to write the synthesis command.

#### Settings

**Default:** none.

Your choice of synthesis tool (from the **Choose synthesis tool** pulldown menu) sets the **Synthesis command** string. The default string is a format string passed to `fprintf` to write the `Cmd` section of the synthesis script. The argument is the filename of the entity or module. The content of the string is specific to the selected synthesis tool.

#### Command-Line Information

**Property:** HDLSynthCmd

**Type:** string

**Default:** none

#### See Also

- Controlling Script Generation with the EDA Tool Scripts GUI Pane
- HDLSynthCmd



## Synthesis termination

Specify a format string passed to `fprintf` to write the termination portion of the synthesis script.

### Settings

**Default:** none

Your choice of synthesis tool (from the **Choose synthesis tool** pulldown menu) sets the **Synthesis termination** string. The default string is a format string passed to `fprintf` to write the `Term` section of the synthesis script. The termination string does not take arguments. The content of the string is specific to the selected synthesis tool.

### Command-Line Information

**Property:** HDLSynthTerm

**Type:** string

**Default:** none

### See Also

- Controlling Script Generation with the EDA Tool Scripts GUI Pane
- HDLSynthTerm



# Specifying Block Implementations and Parameters for HDL Code Generation

---

- “Set and View HDL Block Parameters” on page 8-2
- “Set HDL Block Parameters for Multiple Blocks” on page 8-5
- “View HDL Model Parameters” on page 8-7

## Set and View HDL Block Parameters

In this section...
“Set HDL Block Parameters from the GUI” on page 8-2
“Set HDL Block Parameters from the Command Line” on page 8-2
“View All HDL Block Parameters” on page 8-3
“View Non-Default HDL Block Parameters” on page 8-4

### Set HDL Block Parameters from the GUI

You can view and set HDL-related block properties, such as implementation and implementation parameters, at the individual block level. To open the HDL Properties dialog box:

- 1 Right-click the block.
- 2 Select **HDL Code**.
- 3 Select **HDL Block Properties**.

The HDL Properties dialog box opens.

- 4 Modify the block properties as desired.
- 5 Click OK.

### Set HDL Block Parameters from the Command Line

`hdlset_param(path,Name,Value)` sets HDL-related parameters in the block or model referenced by `path`. One or more `Name,Value` pair arguments specify the parameters to be set, and their values. You can specify several name and value pair arguments in any order as `Name1,Value1, ,NameN,ValueN`.

For example, to set the sharing factor to 2 and the architecture to `Tree` for a block in your model:

- 1 Open the model and select the block.
- 2 Enter the following at the command line:

```
hdlsetparam (gcb, 'SharingFactor', 2, 'Architecture', 'Tree')
```

To view the architecture for the same block, enter the following at the command line:

```
hdlget_param(gcb,'Architecture')
```

You can also assign the returned HDL block parameters to a cell array. In the following example, `hdlget_param` returns all HDL block parameters and values to the cell array `p`.

```
p = hdlget_param(gcb,'all')

p =

    'Architecture'    'Linear'    'InputPipeline'    [0]    'OutputPipeline'    [0]
```

See also `hdlset_param` and `hdlget_param`.

## View All HDL Block Parameters

`hdldispblkparams` displays the HDL block parameters available for a specified block.

The following example displays HDL block parameters and values for the currently selected block.

```
hdldispblkparams(gcb,'all')

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
HDL Block Parameters ('simplevectorsum/vsum/Sum of
Elements')
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

Implementation

Architecture : Linear

Implementation Parameters

InputPipeline : 0
```

```
OutputPipeline : 0
```

See also `hdldispblkparams`.

### View Non-Default HDL Block Parameters

The following example displays only HDL block parameters that have non-default values for the currently selected block.

```
hdldispblkparams(gcb)
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%  
HDL Block Parameters ('simplevectorsum/vsum/Sum of  
Elements')  
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
Implementation
```

```
Architecture : Linear
```

```
Implementation Parameters
```

```
OutputPipeline : 3
```

See also `hdldispblkparams`.

## Set HDL Block Parameters for Multiple Blocks

For models that contain a large number of blocks, using the **HDL Block Properties** dialog box to select block implementations or set implementation parameters for individual blocks may not be practical. It is more efficient to set HDL-related model or block parameters for multiple blocks programmatically. You can use the `find_system` function to locate the blocks of interest. Then, use a loop to call `hdlset_param` to set the desired parameters for each block.

See the Simulink documentation for detailed information about `find_system`.

The following example uses the `sfir_fixed` model to demonstrate how to locate a group of blocks in a subsystem and specify the same output pipeline depth for all the blocks.

- 1** Open the `sfir_fixed` model.
- 2** Click on the `sfir_fixed/symmetric_fir` subsystem to select it.
- 3** Locate all Product blocks within the subsystem as follows:

```
prodblocks = find_system(gcf, 'BlockType', 'Product')

prodblocks =

    'sfir_fixed/symmetric_fir/Product'
    'sfir_fixed/symmetric_fir/Product1'
    'sfir_fixed/symmetric_fir/Product2'
    'sfir_fixed/symmetric_fir/Product3'
```

- 4** Set the output pipeline depth to 2 for all selected blocks.

```
for ii=1:length(prodblocks), hdlset_param(prodblocks{ii}, 'OutputPipeline', 2), end;
```

- 5** To verify the settings, display the value of the `OutputPipeline` parameter for the blocks .

```
for ii=1:length(prodblocks), hdlget_param(prodblocks{ii}, 'OutputPipeline'), end;

ans =
```

2

ans =

2

ans =

2

ans =

2



## View HDL Model Parameters

The coder provides several utility functions to help you obtain HDL-related settings at both the model and block level.

### Obtaining Model-level HDL Settings

To display the names and values of HDL-related properties in a model, use the `hdldispmdlparams` function.

The following example displays HDL-related properties and values of the current model, in alphabetical order by property name.

```
hdldispmdlparams(bdroot, 'all')

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
HDL CodeGen Parameters
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

AddPipelineRegisters           : 'off'
Backannotation                 : 'on'
BlockGenerateLabel            : '_gen'
CheckHDL                      : 'off'
ClockEnableInputPort          : 'clk_enable'
.
.
.
VerilogFileExtension           : '.v'
```

The following example displays only HDL-related properties that have non-default values.

```
hdldispmdlparams(bdroot)

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
HDL CodeGen Parameters (non-default)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

CodeGenerationOutput           : 'GenerateHDLCodeAndDisplayGeneratedModel'
HDLSubsystem                   : 'simplevectorsum/vsum'
```

```
ResetAssertedLevel      : 'Active-low'  
Traceability            : 'on'
```

# Guide to Supported Blocks and Block Implementations

---

- “Generate a Supported Blocks Report” on page 9-2
- “Blocks Supported for HDL Code Generation” on page 9-3
- “Blocks with Multiple Implementations” on page 9-14
- “Block-Specific Usage, Requirements, and Restrictions” on page 9-29
- “Block Implementation Parameters” on page 9-49
- “Blocks That Support Complex Data” on page 9-109
- “Blocks That Support Buses” on page 9-114
- “Lookup Table Block Support” on page 9-119

## Generate a Supported Blocks Report

To generate an HTML table that summarizes blocks supported for HDL Code generation:

- 1** Enter the following at the MATLAB command line:

```
hdl1lib('html');
```

After `hdl1lib` creates the `hdl1supported` library, you see the following:

```
### HDL Supported Block List hdlblklist.html
```

- 2** Click the `hdlblklist.html` link to see the generated block list.

See also “Create a Supported Blocks Library” on page 14-34.

## Blocks Supported for HDL Code Generation

The following table summarizes blocks that the coder supports for HDL code generation.

See “Set and View HDL Block Parameters” on page 8-2 to learn how to set block implementations and parameters in the GUI or the command line.

<b>Simulink Block</b>
commblkcod2/Integer-Input RS Encoder HDL Optimized
commblkcod2/Integer-Output RS Decoder HDL Optimized
commcnvcod2/ Convolutional Encoder (See “Convolutional Encoder Block Requirements and Restrictions” on page 9-32)
commcnvcod2/ Viterbi Decoder (See and .)
commcnvintrlv2/ Convolutional Deinterleaver (See “Convolutional Interleaver and Deinterleaver Block Requirements and Restrictions” on page 9-33.)
commcnvintrlv2/ Convolutional Interleaver (See “Convolutional Interleaver and Deinterleaver Block Requirements and Restrictions” on page 9-33.)

**Simulink Block**

commcnvintrlv2/  
General Multiplexed Deinterleaver

(See “General Multiplexed Interleaver and Deinterleaver Block Requirements and Restrictions” on page 9-37.)

commcnvintrlv2/  
General Multiplexed Interleaver

(See “General Multiplexed Interleaver and Deinterleaver Block Requirements and Restrictions” on page 9-37.)

commcrc2/General CRC Generator HDL Optimized

commcrc2/General CRC Syndrome Detector HDL Optimized

commdigbbndpm3/BPSK Demodulator Baseband

commdigbbndpm3/BPSK Modulator Baseband

commdigbbndpm3/M-PSK Demodulator Baseband

commdigbbndpm3/M-PSK Modulator Baseband

commdigbbndpm3/  
Rectangular QAM Demodulator Baseband

See “Rectangular QAM Demodulator Baseband Block Requirements and Restrictions” on page 9-41

commdigbbndpm3/  
Rectangular QAM Modulator Baseband

See “Rectangular QAM Modulator Baseband Block Requirements and Restrictions” on page 9-41

commdigbbndpm3/  
QPSK Demodulator Baseband

<b>Simulink Block</b>
commdigbbndpm3/QPSK Modulator Baseband
commseqgen2/PN Sequence Generator (See “PN Sequence Generator Block Requirements and Restrictions” on page 9-40.)
dspadpt3/LMS Filter (See “LMS Filter Usage and Restrictions” on page 9-37.)
dsparch4/Biquad Filter (See “Biquad Filter Block Requirements and Restrictions” on page 9-29 , “Pipelining Implementation Parameters for Filter Blocks” on page 9-86, and “CoeffMultipliers” on page 9-52)
dsparch4/Digital Filter (See “Digital Filter Block Requirements and Restrictions” on page 9-34 and “CoeffMultipliers” on page 9-52, “Distributed Arithmetic Implementation Parameters for Digital Filter Blocks” on page 9-54 , “Pipelining Implementation Parameters for Filter Blocks” on page 9-86, and “Speed vs. Area Optimizations for FIR Filter Implementations” on page 9-101.)
dspindex/Multiport Selector
dspindex/Variable Selector
dspmlti4/CIC Decimation (See “Multirate CIC Decimation and Multirate FIR Decimation Blocks Requirements and Restrictions” on page 9-38.) , and “Pipelining Implementation Parameters for Filter Blocks” on page 9-86
dspmlti4/CIC Interpolation (See “Multirate CIC Decimation and Multirate FIR Decimation Blocks Requirements and Restrictions” on page 9-38 “Multirate CIC Interpolation and Multirate FIR Interpolation Blocks Requirements and Restrictions” on page 9-39 , and “Pipelining Implementation Parameters for Filter Blocks” on page 9-86.)

<b>Simulink Block</b>
<p>dspmlti4/FIR Decimation</p> <p>(See “Multirate CIC Decimation and Multirate FIR Decimation Blocks Requirements and Restrictions” on page 9-38 , “CoeffMultipliers” on page 9-52 , “Distributed Arithmetic Implementation Parameters for Digital Filter Blocks” on page 9-54, and “Speed vs. Area Optimizations for FIR Filter Implementations” on page 9-101 and “Pipelining Implementation Parameters for Filter Blocks” on page 9-86</p>
<p>dspmlti4/FIR Interpolation</p> <p>(See “Multirate CIC Interpolation and Multirate FIR Interpolation Blocks Requirements and Restrictions” on page 9-39, “Pipelining Implementation Parameters for Filter Blocks” on page 9-86, “CoeffMultipliers” on page 9-52, “Distributed Arithmetic Implementation Parameters for Digital Filter Blocks” on page 9-54, and “Speed vs. Area Optimizations for FIR Filter Implementations” on page 9-101)</p>
<p>dspsigattribs/Convert 1-D to 2-D</p>
<p>dspsigattribs/Data Type Conversion</p> <p>(See “Data Type Conversion Block Requirements and Restrictions” on page 9-34..)</p>
<p>dspsigattribs/Frame Conversion</p>
<p>dspsigops/Delay</p>
<p>dspsigops/Repeat</p>
<p>dspsigops/Downsample</p>
<p>dspsigops/Upsample</p>
<p>dspsigops/NCO</p> <p>(See “NCO Block Requirements and Restrictions” on page 9-40.)</p>
<p>dspsnks4/Matrix Viewer</p>
<p>dspsnks4/Signal To Workspace</p>
<p>dspsnks4/Spectrum Scope</p>
<p>dspsnks4/Time Scope</p>
<p>dspsnks4/Vector Scope</p>



<b>Simulink Block</b>
dspsnks4/Waterfall
dspsrcs4/DSP Constant
dspsrcs4/Sine Wave (See “Sine Wave Block Requirements and Restrictions” on page 9-42.)
dspstat3/Maximum
dspstat3/Minimum
hlddemolib/Bit Concat (See “Bitwise Operators” on page 11-51.)
hlddemolib/Bit Reduce (See “Bitwise Operators” on page 11-51.)
hlddemolib/Bit Rotate (See “Bitwise Operators” on page 11-51.)
hlddemolib/Bit Shift (See “Bitwise Operators” on page 11-51.)
hlddemolib/Bit Slice (See “Bitwise Operators” on page 11-51.)
hlddemolib/Dual Port RAM (See “Dual Port RAM Block” on page 11-4.)
hlddemolib/HDL Counter (See “HDL Counter” on page 11-16.)
hlddemolib/HDL FFT (See “HDL FFT” on page 11-28.)
hlddemolib/HDL FIFO See “HDL FIFO” on page 11-37.)

<b>Simulink Block</b>
hdlldemolib/HDL Streaming FFT (See “HDL Streaming FFT” on page 11-41.)
hdlldemolib/Simple Dual Port RAM (See “Simple Dual Port RAM Block” on page 11-7.)
hdlldemolib/Single Port RAM (See “Single Port RAM Block” on page 11-8.)
lfilelib/HDL Cosimulation
modelsimlib/HDL Cosimulation
modelsimlib/To VCD File
sflib/Chart
sflib/Truth Table
Signal Routing/From
Signal Routing/Go To
simulink/Additional Math & Discrete/Additional Discrete/Unit Delay Enabled
simulink/Additional Math & Discrete/Additional Discrete/Unit Delay Enabled Resettable
simulink/Additional Math & Discrete/Additional Discrete/Unit Delay Resettable
simulink/Additional Math & Discrete/ Additional Math: Increment - Decrement/Decrement Real World
simulink/Additional Math & Discrete/ Additional Math: Increment - Decrement/Increment Real World
simulink/Additional Math & Discrete/ Additional Math: Increment - Decrement/Decrement Stored Integer
simulink/Additional Math & Discrete/ Additional Math: Increment - Decrement/Increment Stored Integer
simulink/Commonly Used Blocks/Constant

**Simulink Block**

simulink/Commonly Used Blocks/Data Type Conversion

(See “Data Type Conversion Block Requirements and Restrictions” on page 9-34.)

simulink/Commonly Used Blocks/  
Discrete-Time Integrator

(See “Discrete-Time Integrator Requirements and Restrictions” on page 9-36.)

simulink/Commonly Used Blocks/Demux

simulink/Commonly Used Blocks/Gain

simulink/Commonly Used Blocks/Ground

simulink/Commonly Used Blocks/In1

simulink/Commonly Used Blocks/Logical Operator

simulink/Commonly Used Blocks/Mux

simulink/Commonly Used Blocks/Out1

simulink/Commonly Used Blocks/Product

simulink/Commonly Used Blocks/Relational Operator

simulink/Commonly Used Blocks/Saturation

simulink/Commonly Used Blocks/Scope

simulink/Commonly Used Blocks/Sum

simulink/Commonly Used Blocks/Switch

simulink/Commonly Used Blocks/Terminator

simulink/Commonly Used Blocks/Unit Delay

simulink/Discontinuities/  
Saturation Dynamic

<b>Simulink Block</b>
simulink/Discrete/ Discrete FIR Filter  (See “CoeffMultipliers” on page 9-52, “Distributed Arithmetic Implementation Parameters for Digital Filter Blocks” on page 9-54 , “Pipelining Implementation Parameters for Filter Blocks” on page 9-86 , and “Speed vs. Area Optimizations for FIR Filter Implementations” on page 9-101.)
simulink/Discontinuities/ Saturation
simulink/Discrete/Delay
simulink/Discrete/Discrete Transfer Fcn
simulink/Discrete/Memory
simulink/Discrete/Tapped Delay
simulink/Discrete/ Zero-Order Hold
simulink/Logic and Bit Operations/Bit Clear
simulink/Logic and Bit Operations/Bit Set
simulink/Logic and Bit Operations/Bitwise Operator
simulink/Logic and Bit Operations/Compare To Constant
simulink/Logic and Bit Operations/Extract Bits
simulink/Logic and Bit Operations/Compare To Zero
simulink/Logic and Bit Operations/Shift Arithmetic
simulink/Lookup Tables/Direct Lookup Table (n-D) (See “Lookup Table Block Support” on page 9-119)
simulink/Lookup Tables/1-D Lookup Table (See “Lookup Table Block Support” on page 9-119.)
simulink/Lookup Tables/n-D Lookup Table (See “Lookup Table Block Support” on page 9-119)

<b>Simulink Block</b>
simulink/Lookup Tables/Prelookup (See “Lookup Table Block Support” on page 9-119)
simulink/Math Operations/Abs
simulink/Math Operations/Add
simulink/Math Operations/Assignment
simulink/Math Operations/Complex to Real-Imag
simulink/Math Operations/Divide The reciprocal operation is a special case, supporting two implementations, as described in “Divide Block Implementations” on page 9-26.)
simulink/Math Operations/ Magnitude-Angle to Complex
simulink/Math Operations/Math Function (sqrt, reciprocal, conj, hermitian, transpose)
simulink/Math Operations/Matrix Concatenate
simulink/Math Operations/MinMax
simulink/Math Operations/Product of Elements
simulink/Math Operations/Real-Imag to Complex
simulink/Math Operations/Reciprocal Sqrt (See “Reciprocal Sqrt Block Requirements and Restrictions” on page 9-41.)
simulink/Math Operations/Reshape
simulink/Math Operations/Sign
simulink/Math Operations/Sqrt
simulink/Math Operations/Subtract
simulink/Math Operations/Sum of Elements
simulink/Math Operations/Trigonometric Function — sin, cos, cos + jsin, and sincos supported, only if you select the CORDIC approximation method. (See “Trigonometric Function Block Requirements and Restrictions” on page 9-42.)

<b>Simulink Block</b>
simulink/Math Operations/Unary Minus
simulink/Math Operations/Vector Concatenate
simulink/Model Verification/Assertion
simulink/Model Verification/Check Discrete Gradient
simulink/Model Verification/Check Dynamic Gap
simulink/Model Verification/Check Dynamic Lower Bound
simulink/Model Verification/Check Dynamic Range
simulink/Model Verification/Check Dynamic Upper Bound
simulink/Model Verification/Check Input Resolution
simulink/Model Verification/Check Static Gap
simulink/Model Verification/Check Static Lower Bound
simulink/Model Verification/Check Static Range
simulink/Model Verification/Check Static Upper Bound
simulink/Model-Wide Utilities/DocBlock
simulink/Model-Wide Utilities/Model Info
simulink/Ports & Subsystems/Enable (See “Generate Code for Enabled and Triggered Subsystems” on page 15-18.)
simulink/Ports & Subsystems/Trigger (See “Generate Code for Enabled and Triggered Subsystems” on page 15-18.)
simulink/Ports & Subsystems/Model
simulink/Signal Attributes/Data Type Duplicate
simulink/Signal Attributes/Data Type Propagation
simulink/Signal Attributes/Rate Transition
simulink/Signal Attributes/Signal Conversion
simulink/Signal Attributes/Signal Specification

<b>Simulink Block</b>
simulink/Signal Routing/Bus Creator
simulink/Signal Routing/Bus Selector
simulink/Signal Routing/Index Vector
simulink/Signal Routing/Multiport Switch
simulink/Signal Routing/Selector
simulink/Sinks/Display
simulink/Sinks/Floating Scope
simulink/Sinks/Stop Simulation
simulink/Sinks/To File
simulink/Sinks/To Workspace
simulink/Sinks/XY Graph
simulink/Sources/Counter Free-Running
simulink/Sources/Counter Limited
simulink/User-Defined Functions/MATLAB Function

## Blocks with Multiple Implementations

In this section...
“Overview” on page 9-14
“Implementations for Commonly Used Blocks” on page 9-15
“Math Function Block Implementations” on page 9-21
“Divide Block Implementations” on page 9-26
“Subsystem Interfaces and Special-Purpose Implementations” on page 9-27
“A Note on Cascade Implementations” on page 9-28

### Overview

The tables in this section summarize the block types that have multiple implementations. The Table columns are

- *Implementations*: This column gives the implementation name.
- *Description*: This column summarizes the tradeoffs involved in choosing different implementations.

The coder provides a default HDL block implementation for supported blocks. If you want to use the default implementation, you do not usually need to specify it explicitly.

See “Set and View HDL Block Parameters” on page 8-2 to learn how to set block implementations and parameters in the GUI or the command line.



## Implementations for Commonly Used Blocks

### Built-In/Constant

Implementations	Parameters	Description
default Constant	Unspecified	This implementation emits the value of the Constant block.
	{'OutputPipeline', NStages}	See “OutputPipeline” on page 9-85.
Logic Value	Unspecified	By default, this implementation emits the character 'Z' for each bit in the signal. For example, for a 4-bit signal, the implementation would emit 'ZZZZ'.
	{'Value', 'Z'}	Use this parameter value if the signal is in a high-impedance state. This implementation emits the character 'Z' for each bit in the signal. For example, for a 4-bit signal, the implementation would emit 'ZZZZ'.
	{'Value', 'X'}	Use this parameter value if the signal is in an unknown state. This implementation emits the character 'X' for each bit in the signal. For example, for a 4-bit signal, the implementation would emit 'XXXX'.
	{'OutputPipeline', NStages}	See “OutputPipeline” on page 9-85.

### Note

The Logic Value implementation does not support the double data type. If you specify this implementation for a Constant of type double, a code-generation error occurs.

**Built-In/Gain**

Implementations	Parameters	Description
default	'ConstMultiplierOptimization', 'none' (Default)	By default, the coder does not perform CSD or FCSD optimizations. Code generated for the Gain block retains multiplier operations.
	'ConstMultiplierOptimization', 'CSD'	When you specify this option, the generated code decreases the area used by the model while maintaining or increasing clock speed, using canonic signed digit (CSD) techniques. CSD replaces multiplier operations with add and subtract operations.  CSD minimizes the number of addition operations required for constant multiplication by representing binary numbers with a minimum count of nonzero digits.
	'ConstMultiplierOptimization', 'FCSD'	This option uses factored CSD (FCSD) techniques, which replace multiplier operations with shift and add/subtract operations on certain factors of the operands. These factors are generally prime but can also be a number close to a power of 2, which favors area reduction. FCSD lets you achieve a greater area reduction than CSD, at the cost of decreasing clock speed.
	'ConstMultiplierOptimization', 'auto'	When you specify this option, the coder chooses between the CSD or FCSD optimizations. The coder chooses the optimization that yields the most area-efficient implementation, based on the number of adders required. When you specify 'auto', the coder does not use multipliers, unless

**Built-In/Gain (Continued)**

Implementations	Parameters	Description
		conditions are such that CSD or FCSD optimizations are not possible (for example, if the design uses floating-point arithmetic).

**Built-In/1-D Lookup Table**

Implementations	Description
default	Nonhierarchical lookup table.
Instantiate	This implementation generates an additional level of HDL hierarchy (which does not exist in the Simulink model) for the lookup table.

See also “Lookup Table Block Support” on page 9-119.

**DSP System Toolbox/Minimum**

Implementations	Parameters	Description
default Tree		The <b>Tree</b> implementation is large and slow but has minimal latency.
Cascade		This implementation is optimized for latency * area, with medium speed. See “A Note on Cascade Implementations” on page 9-28

**DSP System Toolbox/Maximum**

Implementations	Parameters	Description
default Tree		The Tree implementation is large and slow but has minimal latency.
Cascade		This implementation is optimized for latency * area, with medium speed. See “A Note on Cascade Implementations” on page 9-28

**Built-In/MinMax**

Implementations	Parameters	Description
default Tree		The Tree implementation is large and slow but has minimal latency.
Cascade		This implementation is optimized for latency * area, with medium speed. See “A Note on Cascade Implementations” on page 9-28

**Built-In/Product**

Implementations	Parameters	Description
default Linear		Generates a chain of N operations (multipliers) for N inputs.
	{'InputPipeline', NStages}	See “InputPipeline” on page 9-78.
	{'OutputPipeline', NStages}	See “OutputPipeline” on page 9-85.

**Built-In/Product (Continued)**

Implementations	Parameters	Description
Tree		<p>This implementation has minimal latency but is large and slow. It generates a tree-shaped structure of multipliers.</p> <p><b>Note:</b> Product blocks that have a vector input with two or more elements support Tree and Cascade.</p>
	{'InputPipeline', NStages}	See “InputPipeline” on page 9-78.
	{'OutputPipeline', NStages}	See “OutputPipeline” on page 9-85.
Cascade		<p>This implementation optimizes latency * area and is faster than the tree implementation. It computes partial products and cascades multipliers.</p> <p><b>Note:</b> Product blocks that have a vector input with two or more elements support Tree and Cascade.</p> <p>See “A Note on Cascade Implementations” on page 9-28</p>
	{'InputPipeline', NStages}	See “InputPipeline” on page 9-78.
	{'OutputPipeline', NStages}	See “OutputPipeline” on page 9-85

**Built-In/Product (Continued)**

Implementations	Parameters	Description
RecipNewton	{'Iterations', N}	When you compute a product, use iterative Newton method. The argument N specifies the number of iterations.  The default value for N is 3.  The recommended value for N is between 2 and 10. The coder generates a message if N is outside the recommended range.
	{'InputPipeline', NStages}	See “InputPipeline” on page 9-78.
	{'OutputPipeline', NStages}	See “OutputPipeline” on page 9-85

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**Note** When the Product block is in divide ( $\ast/$ ) mode, it supports only integer data types for HDL code generation.

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**Built-In/Sum**

Implementations	Parameters	Description
default Linear		Generates a chain of N operations (adders ) for N inputs.  <b>Note:</b> The coder supports Tree and Cascade for Sum blocks that have a single vector input with multiple elements.

**Built-In/Sum (Continued)**

Implementations	Parameters	Description
	{ 'InputPipeline', NStages}	See “InputPipeline” on page 9-78.
	{ 'OutputPipeline', NStages}	See “OutputPipeline” on page 9-85.
Tree		This implementation has minimal latency but is large and slow. Generates a tree-shaped structure of adders.
	{ 'InputPipeline', NStages}	See “InputPipeline” on page 9-78.
	{ 'OutputPipeline', NStages}	See “OutputPipeline” on page 9-85.
Cascade		This implementation optimizes latency * area and is faster than the tree implementation. It computes partial sums and cascades adders.  See “A Note on Cascade Implementations” on page 9-28.
	{ 'InputPipeline', NStages}	See “InputPipeline” on page 9-78.
	{ 'OutputPipeline', NStages}	See “OutputPipeline” on page 9-85.

**Math Function Block Implementations**

The coder supports the Math Function block `sqrt`, `reciprocal`, `conj`, `hermitian`, and `transpose` functions for HDL code generation.

By specifying an implementation and parameters, you can choose from among several algorithms for computing these functions. The following

tables summarize the available Math Function block implementations and parameters.

**simulink/Math Operations/Math Function (sqrt)**

Implementations	Parameters	Description
default SqrtBitset	'UseMultiplier', 'on'}	<i>(Default parameter)</i> : Compute sqrt using multiply/add algorithm (Simulink default algorithm).
	'UseMultiplier', 'off'}	Compute sqrt using bitset shift/addition algorithm.
	'InputPipeline', NStages}	See “InputPipeline” on page 9-78 .
	'OutputPipeline', NStages}	See “OutputPipeline” on page 9-85.
SqrtNewton	'Iterations', N}	Compute sqrt using iterative Newton method. The argument N specifies the number of iterations.  The default value for N is 5.  The recommended value for N is between 3 and 10. The coder generates a message if N is outside the recommended range.
	'InputPipeline', NStages}	See “InputPipeline” on page 9-78.
	'OutputPipeline', NStages}	See “OutputPipeline” on page 9-85.



When you use the `sqrt` implementations, consider the following:

- Input must be an unsigned scalar value.
- The output is a fixed-point scalar value.
- The Math Function block from the `hdl1lib` library has `sqrt` selected in its **Function** menu.

### **simulink/Math Operations/Math Function (reciprocal)**

<b>Implementations</b>	<b>Parameters</b>	<b>Description</b>
default Reciprocal	Unspecified ( <i>Default</i> )	Compute reciprocal as $1/N$ , using the HDL divide ( <code>/</code> ) operator to implement the division.
	{ 'InputPipeline', NStages }	See “InputPipeline” on page 9-78.
	{ 'OutputPipeline', NStages }	See “OutputPipeline” on page 9-85.
RecipNewton	{ 'Iterations', N }	Compute reciprocal using iterative Newton method. The argument <code>N</code> specifies the number of iterations.  The default value for <code>N</code> is 3.  The recommended value for <code>N</code> is between 2 and 10. The coder generates a message if <code>N</code> is outside the recommended range.
	{ 'InputPipeline', NStages }	See “InputPipeline” on page 9-78.
	{ 'OutputPipeline', NStages }	See “OutputPipeline” on page 9-85.

When you use a `reciprocal` implementation, consider the following:

- Input must be scalar and must have integer or fixed-point (signed or unsigned) data type.

- The output must be scalar and have integer or fixed-point (signed or unsigned) data type.
- Only the Zero rounding mode is supported.
- The **Saturate on integer overflow** option on the block must be selected.

**simulink/Math Operations/Math Function (conj)**

Implementations	Parameters	Description
ComplexConjugate	Unspecified ( <i>Default</i> )	Compute complex conjugate. See Math Function in the Simulink documentation.
	{ 'InputPipeline', NStages }	See “InputPipeline” on page 9-78.
	{ 'OutputPipeline', NStages }	See “OutputPipeline” on page 9-85.

**simulink/Math Operations/Math Function (hermitian)**

Implementations	Parameters	Description
Hermitian	Unspecified ( <i>Default</i> )	Compute hermitian. See Math Function in the Simulink documentation.
	{ 'InputPipeline', NStages }	See “InputPipeline” on page 9-78 .
	{ 'OutputPipeline', NStages }	See “OutputPipeline” on page 9-85.

**simulink/Math Operations/Math Function (transpose)**

Implementations	Parameters	Description
Transpose	Unspecified ( <i>Default</i> )	Compute array transpose. See Math Function in the Simulink documentation.
	{ 'InputPipeline', NStages }	See “InputPipeline” on page 9-78 .
	{ 'OutputPipeline', NStages }	See “OutputPipeline” on page 9-85.

**simulink/Math Operations/Math Function (parent class)**

Implementations	Parameters	Description
default Math	Unspecified ( <i>Default</i> )	Use the default implementation for the function (sqrt,reciprocal, or conj) selected on the block.
	{ 'UseMultiplier', 'on' } (use with sqrt only)	If the function selected on the block is sqrt, compute sqrt using multiply/add algorithm (Simulink default algorithm). If the function selected on the block is not sqrt, an error results.
	{ 'UseMultiplier', 'off' } (use with sqrt only)	If the function selected on the block is sqrt, compute sqrt using bitset shift/addition algorithm. If the function selected on the block is not sqrt, an error results.
	{ 'InputPipeline', NStages }	See “InputPipeline” on page 9-78.
	{ 'OutputPipeline', NStages }	See “OutputPipeline” on page 9-85.

## Divide Block Implementations

The Divide block normally supports the Linear, Tree and Cascade implementations.

However, the reciprocal operation of the Divide block is a special case. When you select the reciprocal operation, the Divide block supports the implementations described in the following table.

### simulink/Math Operations/Divide (reciprocal computation only)

Implementations	Parameters	Description
default Linear	Unspecified ( <i>Default</i> )	When you compute a reciprocal, compute $1/N$ using the HDL divide (/) operator to implement the division.
	{'InputPipeline', NStages}	See “InputPipeline” on page 9-78.
	{'OutputPipeline', NStages}	See “OutputPipeline” on page 9-85.
RecipNewton	{'Iterations', N}	When you compute a reciprocal, use iterative Newton method. The argument N specifies the number of iterations.  The default value for N is 3.  The recommended value for N is between 2 and 10. The coder generates a message if N is outside the recommended range.
	{'InputPipeline', NStages}	See “InputPipeline” on page 9-78.
	{'OutputPipeline', NStages}	See “OutputPipeline” on page 9-85.

When you use a reciprocal implementation, consider the following:

- Input must be scalar and must have integer or fixed-point (signed or unsigned) data type.
- The output must be scalar and have integer or fixed-point (signed or unsigned) data type.
- Only the Zero rounding mode is supported.
- The **Saturate on integer overflow** option on the block must be selected.

## Subsystem Interfaces and Special-Purpose Implementations

### Built-In/SubSystem

Implementation	Description
BlackBox	<p>This implementation generates a black-box interface for subsystems. That is, the generated HDL code includes only the input/output port definitions for the subsystem. In this way, you can use a subsystem in your model to generate an interface to existing manually written HDL code.</p> <p>The black-box interface generated for subsystems is similar to the interface generated for Model blocks, but without generation of clock signals.</p>
default No HDL	<p>This implementation completely removes the subsystem from the generated code. Thus, you can use a subsystem in simulation but treat it as a “no-op” in the HDL code.</p>

For more information on code generation for subsystems, see “External Component Interfaces”.

## Special-Purpose Implementations

Implementation	Description
Pass-through implementations	<p>Provides a pass-through implementation in which the block's inputs are passed directly to its outputs. The coder supports the following blocks with a pass-through implementation:</p> <ul style="list-style-type: none"> <li>• Convert 1-D to 2-D</li> <li>• Reshape</li> <li>• Signal Conversion</li> <li>• Signal Specification</li> </ul>
No HDL	<p>This implementation completely removes the block from the generated code. Thus, you can use the block in simulation but treat it as a “no-op” in the HDL code. This implementation is used for many blocks (such as Scopes and Assertions) that are significant in simulation but would be meaningless in HDL code.</p> <p>You can also use this implementation as an alternative implementation for subsystems.</p>

For more information related to special-purpose implementations, see “External Component Interfaces”.

### A Note on Cascade Implementations

The coder supports cascade implementations for the Sum of Elements, Product of Elements, and MinMax blocks. These implementations require multiple clock cycles to process their inputs; therefore, their inputs must be kept unchanged for their entire sample-time period. Generated test benches accomplish this by using a register to drive the inputs.

A recommended design practice, when integrating generated HDL code with other HDL code, is to provide registers at the inputs. While not strictly required, adding registers to the inputs improves timing and avoids problems with data stability for blocks that require multiple clock cycles to process their inputs.

## Block-Specific Usage, Requirements, and Restrictions

In this section...
“Block Usage, Requirements, and Restrictions” on page 9-29
“Restrictions on Use of Blocks in the Test Bench” on page 9-48

### Block Usage, Requirements, and Restrictions

This section discusses requirements and restrictions that apply to the use of specific block types in HDL code generation.

#### Biquad Filter Block Requirements and Restrictions

- “General Guidelines” on page 9-29
- “Programmable Filter Support” on page 9-29
- “Serial Architecture Support” on page 9-30

#### General Guidelines.

- Data vector and frame inputs are not supported for HDL code generation.
- **Initial conditions** must be set to zero. HDL code generation is not supported for nonzero initial states.
- **Optimize unity scale values** must be selected.

**Programmable Filter Support.** The coder supports programmable filters for Biquad Filters. Fully parallel and all applicable serial architectures are supported.

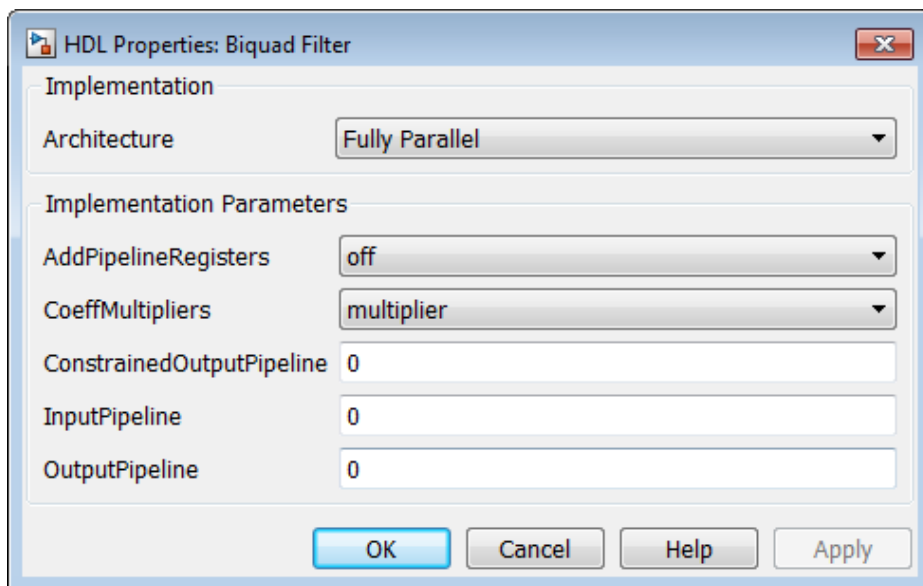
- 1 Select **Input port(s)** as coefficient source on the filter block mask.
- 2 Connect the coefficient port with a vector signal.
- 3 Specify the implementation architecture and parameters from the HDL Coder property interface.
- 4 Generate HDL code.

Programmable filters are not supported for:

- CoeffMultipliers as csd or factored-csd

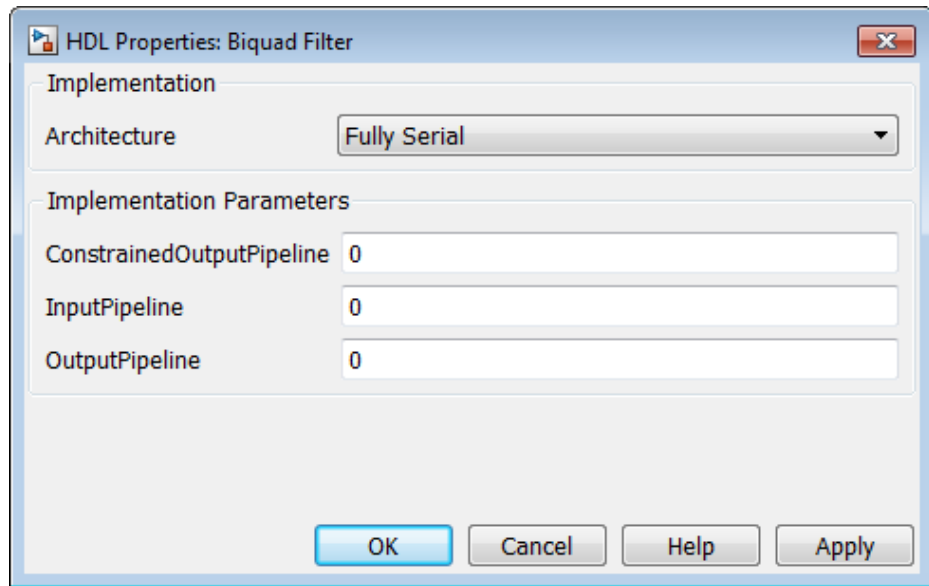
**Serial Architecture Support.** Biquad Filter block supports fully parallel, fully serial, and partly serial architectures.

- Fully Parallel (default): AddPipelineRegisters, CoeffMultipliers, ConstrainedOutputPipeline, InputPipeline, OutputPipeline

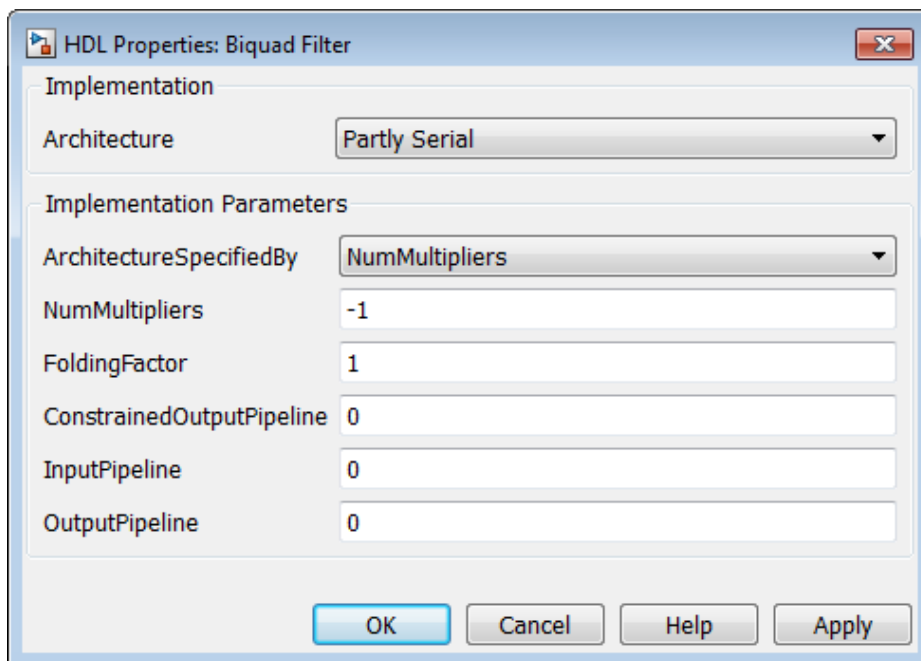


- Fully Serial: ConstrainedOutputPipeline, InputPipeline, OutputPipeline





- Partly Serial: ArchitectureSpecifiedBy, NumMultipliers, FoldingFactor, ConstrainedOutputPipeline, InputPipeline, OutputPipeline



### Convolutional Encoder Block Requirements and Restrictions

Input data requirements:

- Must be sample-based,
- Must have boolean or ufix1 data type.

The coder supports only the following coding rates:

- $\frac{1}{2}$  to  $\frac{1}{7}$
- $\frac{2}{3}$

The coder supports only constraint lengths for 3 to 9.

**Trellis structure** must be specified by the `poly2trellis` function.

The coder supports the following **Operation mode** settings:

- Continuous
- Reset on nonzero input via port

If you select this mode, you must select the **Delay reset action to next time step** option. When you select this option, the Convolutional Encoder block finishes its current computation before executing a reset.

## Convolutional Interleaver and Deinterleaver Block Requirements and Restrictions

**Shift Register Based Implementations.** The default implementations for the Convolutional Interleaver and Deinterleaver blocks are shift register based. If you want to suppress generation of reset logic, set the implementation parameter `ResetType` to 'none'.

Note that when you set `ResetType` to 'none', reset is not applied to the shift registers. Mismatches between Simulink and the generated code occur for some number of samples during the initial phase, when registers are not fully loaded. To avoid spurious test bench errors, determine the number of samples required to fully load the shift registers. Then, set the **Ignore output data checking (number of samples)** option accordingly. (You can use the `IgnoreDataChecking` property for this purpose, if you are using the command-line interface)

**RAM Based Implementations.** When you select the RAM implementation for a Convolutional Interleaver or Deinterleaver block, the coder uses RAM resources instead of shift registers. The implementation has the following limitations:

When you select the RAM implementation for a Convolutional Interleaver or Deinterleaver block, the coder uses RAM resources instead of shift registers.

- Double or single data types are not supported for either input or output signals.
- **Initial conditions** for the block must be set to zero.
- At least two rows of interleaving are required .

### **Data Type Conversion Block Requirements and Restrictions**

If you configure a Data Type Conversion block for double to fixed-point or fixed-point to double conversion, a warning displays during code generation.

### **Digital Filter Block Requirements and Restrictions**

- If you select the Digital Filter block **Discrete-time filter object** option, you must have the DSP System Toolbox software to generate code for the block.
- **Initial conditions** must be set to zero. HDL code generation is not supported for nonzero initial states.
- The coder does not support the Digital Filter block **Input port(s)** option for HDL code generation.
- The Digital Filter block supports complex data for all filter structures except decimators and interpolators. See “Complex Coefficients and Data Support for the Digital Filter and Biquad Filter Blocks” on page 9-113.

### **Discrete FIR Filter Requirements and Restrictions**

- “General Guidelines” on page 9-34
- “Multichannel Filter Support” on page 9-35
- “Programmable Filter Support” on page 9-35

#### **General Guidelines.**

- The coder does not support unsigned inputs for the Discrete FIR Filter block.
- **Initial conditions** must be set to zero. HDL code generation is not supported for nonzero initial states.
- The coder does not support the following options of the Discrete FIR Filter block:
  - **Filter Structure** : Lattice MA

**Multichannel Filter Support.** The coder supports the use of vector inputs for Discrete FIR Filters.

- 1 Connect vector signals to Discrete FIR block input port.
- 2 Specify **Input processing** as `Elements as channels` (sample based).
- 3 Specify architecture and implementation parameters.
- 4 Specify channel sharing option as on for fully parallel support.
- 5 Generate HDL code.

**Programmable Filter Support.** The coder supports programmable filters for Discrete FIR Filters. Fully parallel and all applicable serial architectures are supported.

- 1 Select **Input port(s)** as coefficient source on the filter block mask.
- 2 Connect the coefficient port with a vector signal.
- 3 Specify the implementation architecture and parameters from the HDL Coder property interface.
- 4 Generate HDL code.

Programmable filters are not supported for:

- Any implementation for which you specify the coefficients by dialog parameters (for example, complex input and coefficients with serial architecture)
- Distributed Arithmetic (DA)
- `CoeffMultipliers` as `csd` or `factored-csd`

For an example, see `Generate HDL Code for FIR Programmable Filter`.

### **Discrete Transfer Fcn Requirements and Restrictions**

The following limitations apply to HDL code generation from the Discrete Transfer Fcn block:

- You must use the **Inherit: Inherit via internal rule** option for data type propagation if, and only if, the input data type is double.
- Frame, matrix, and vector input data types are not supported.
- The leading denominator coefficient ( $a_0$ ) must be 1 or -1.

The Discrete Transfer Fcn block cannot participate in the following optimizations:

- Resource sharing
- Distributed pipelining

### **Discrete-Time Integrator Requirements and Restrictions**

- Use of state ports is not supported for HDL code generation. Clear the **Show state port** option.
- Use of external initial conditions is not supported for HDL code generation. Set **Initial condition source** to Internal.
- Width of input and output signals must not exceed 32 bits.

### **FIR Decimation Requirements and Restrictions**

**Initial conditions** must be set to zero. HDL code generation is not supported for nonzero initial states.

See also “Multirate CIC Decimation and Multirate FIR Decimation Blocks Requirements and Restrictions” on page 9-38.

### **FIR Interpolation Requirements and Restrictions**

**Initial conditions** must be set to zero. HDL code generation is not supported for nonzero initial states.

See also “Multirate CIC Interpolation and Multirate FIR Interpolation Blocks Requirements and Restrictions” on page 9-39.

## General Multiplexed Interleaver and Deinterleaver Block Requirements and Restrictions

**Shift Register Based Implementations.** The default implementations for the General Multiplexed Interleaver and Deinterleaver blocks are shift register based. If you want to suppress generation of reset logic, set the implementation parameter `ResetType` to 'none'.

Note that when you set `ResetType` to 'none', reset is not applied to the shift registers. Mismatches between Simulink and the generated code occur for some number of samples during the initial phase, when registers are not fully loaded. To avoid spurious test bench errors, determine the number of samples required to fully load the shift registers. Then, set the **Ignore output data checking (number of samples)** option accordingly. (You can use the `IgnoreDataChecking` property for this purpose, if you are using the command-line interface)

## LMS Filter Usage and Restrictions

By default, the LMS Filter implementation uses a linear sum for the FIR section of the filter.

The LMS Filter implements a tree summation (which has a shorter critical path) under the following conditions:

- The LMS Filter is used with real data
- The word length of the Accumulator  $W^u$  data type is at least  $\text{ceil}(\log_2(\text{filter length}))$  bits wider than the word length of the Product  $W^u$  data type
- The Accumulator  $W^u$  data type has the same fraction length as the Product  $W^u$  data type

The LMS Filter block has the following restrictions for HDL code generation:

- The coder does not support the Normalized LMS algorithm of the LMS Filter.
- The Reset port supports only Boolean and unsigned inputs.
- The Adapt port supports only Boolean inputs.

- **Filter length** must be greater than or equal to 2.

### **Magnitude-Angle to Complex Block Requirements and Restrictions**

The Magnitude-Angle to Complex block supports HDL code generation when you set **Approximation method** to CORDIC.

### **Multirate CIC Decimation and Multirate FIR Decimation Blocks Requirements and Restrictions**

The following requirements apply to both the Multirate CIC Decimation and Multirate FIR Decimation blocks:

- The coder supports both **Coefficient source** options (**Dialog parameters** or **Multirate filter object (MFILT)**).
- When you select **Multirate filter object (MFILT)**:
  - You can enter either a filter object name or a direct filter specification in the **Multirate filter variable** field.
- Vector and frame inputs are not supported for HDL code generation.

For the Multirate FIR Decimation block:

- When you select **Multirate filter object (MFILT)**, the filter object specified in the **Multirate filter variable** field must be either a `mfilt.firdecim` object or a `mfilt.firtdecim` object. If you specify some other type of filter object, an error will occur.
- When you select **Dialog parameters**, the following fixed-point options are not supported for HDL code generation:
  - Slope and Bias scaling
  - Inherit via internal rule

For the Multirate CIC Decimation block:

- When you select **Multirate filter object (MFILT)**, the filter object specified in the **Multirate filter variable** field must be a `mfilt.cicdecim` object. If you specify some other type of filter object, an error will occur.



- When you select **Dialog parameters**, the **Filter Structure** option Zero-latency decimator is not supported for HDL code generation. Select Decimator in the **Filter Structure** pulldown menu.

### **Multirate CIC Interpolation and Multirate FIR Interpolation Blocks Requirements and Restrictions**

The following requirements apply to both the Multirate CIC Interpolation and Multirate FIR Interpolation blocks:

- The coder supports both **Coefficient source** options (**Dialog parameters** or **Multirate filter object (MFILT)**).
- When you select **Multirate filter object (MFILT)**:
  - You can enter either a filter object name or a direct filter specification in the **Multirate filter variable** field.
- Vector and frame inputs are not supported for HDL code generation.

For the Multirate FIR Interpolation block:

- When you select **Multirate filter object (MFILT)**, the filter object specified in the **Multirate filter variable** field must be a `mfilt.firinterp` object. If you specify some other type of filter object, an error will occur.
- When you select **Dialog parameters**, the following fixed-point options are not supported for HDL code generation:
  - **Coefficients**: Slope and Bias scaling
  - **Product Output**: Inherit via internal rule

For the Multirate CIC Interpolation block:

- When you select **Multirate filter object (MFILT)**, the filter object specified in the **Multirate filter variable** field must be a `mfilt.cicinterp` object. If you specify some other type of filter object, an error will occur.
- When you select **Dialog parameters**, the **Filter Structure** option Zero-latency interpolator is not supported for HDL code generation. Select Interpolator in the **Filter Structure** dropdown menu.

## NCO Block Requirements and Restrictions

Inputs:

- The phase increment and phase offset support only integer or fixed-point data types.
- The phase increment and phase offset can be either scalar or vector values.

Outputs:

- The coder supports only fixed point data types for the quantization error (`Qerr`) port and output signals.

Parameters:

- The coder does not support **Add internal dither** for vector inputs
- If **Quantize phase** is selected, **Number of quantized accumulator bits** should be greater than or equal to 4. A `checkhdl` error occurs when there are fewer than 4 quantized accumulator bits.
- If **Quantize phase** is deselected, the accumulator **Word length** should be greater than or equal to 4. A `checkhdl` error occurs when there are fewer than 4 accumulator bits.

## PN Sequence Generator Block Requirements and Restrictions

Inputs:

- You can select `Input` port as the **Output mask source** on the block. However, in this case the `Mask` input signal must be a vector of data type `ufix1`.
- If **Reset on nonzero input** is selected, the input to the `Rst` port must have data type `Boolean`.

Outputs:

- Outputs of type `double` are not supported for HDL code generation. All other output types (including bit packed outputs) are supported.

## Reciprocal Sqrt Block Requirements and Restrictions

When using this block for HDL code generation, set the **Method** parameter to Newton-Raphson.

## Rectangular QAM Demodulator Baseband Block Requirements and Restrictions

The coder has the following requirements and restrictions for the Rectangular QAM Demodulator Baseband block:

- The block does not support single or double data types for HDL code generation.
- The coder supports the following **Output type** options:
  - Integer
  - Bit is supported only if the **Decision Type** selected is Hard decision.
- The coder requires that **Normalization Method** be set to Minimum Distance Between Symbols, with a **Minimum distance** of 2.
- The coder requires that **Phase offset (rad)** be set to a value that is multiple a of  $\pi/4$ .

## Rectangular QAM Modulator Baseband Block Requirements and Restrictions

The coder has the following requirements and restrictions for the Rectangular QAM Modulator Baseband block:

- The block does not support single or double data types for HDL code generation.
- When **Input Type** is set to Bit, the block does not support HDL code generation for input types other than `boolean` or `ufix1`.

The Rectangular QAM Modulator Baseband block does not support HDL code generation when the input type is set to Bit but the block input is actually multibit (uint16, for example).

### Sine Wave Block Requirements and Restrictions

For HDL code generation, you must select the following Sine Wave block settings:

- **Computation method:** Table lookup
- **Sample mode:** Discrete

Output:

- The output port cannot have data types single or double.

### Trigonometric Function Block Requirements and Restrictions

The Trigonometric Function block supports HDL code generation for the following functions:

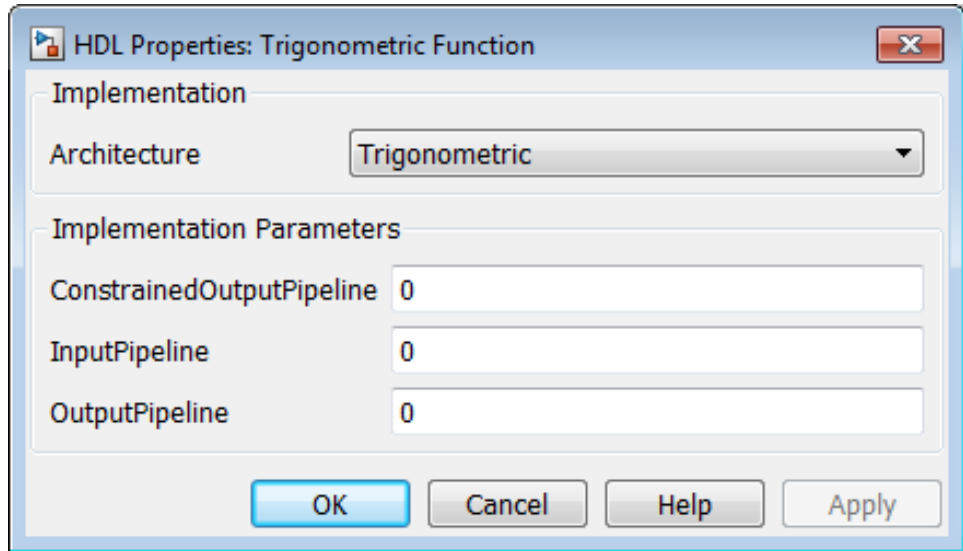
Trigonometric Function Block Implementation	Supported Functions	Supported Approximation Methods
default Trigonometric	sin	CORDIC
	cos	CORDIC
	cos + jsin	CORDIC
	sincos	CORDIC

For the `sin` and `cos` functions, unsigned data types are supported for CORDIC approximations.

The coder gives an error when:

- You select an unsupported function on the Trigonometric Function block.
- You select an **Approximation method** other than CORDIC.

Use the default implementation for the Trigonometric Function block, as shown in the following figure.



See also Trigonometric Function, `cordicsin`, `cordiccos`, and `cordicsincos`.

## Viterbi Decoder Block Requirements and Restrictions

- “General Guidelines” on page 9-43
- “Limitations” on page 9-44
- “Input and Output Data Types” on page 9-44
- “Pipelining the Traceback Unit” on page 9-45
- “RAM-Based Traceback” on page 9-45
- “Viterbi Decoder Example” on page 9-48

**General Guidelines.** The coder currently supports the following features of the Viterbi Decoder block:

- Non-recursive encoder/decoder with feed-forward trellis and simple shift register generation configuration
- Sample based input

- Decoder rates from 1/2 to 1/7
- Constraint length from 3 to 9

**Limitations.** When you generate code for the Viterbi Decoder block, observe the following limitations:

- **Punctured code:** Do not select this option. Punctured code requires frame-based input, which the coder does not support.
- **Decision type:** the coder does not support the Unquantized decision type.
- **Error if quantized input values are out of range:** The coder does not support this option.
- **Operation mode:** The coder supports only the Continuous mode.
- **Enable reset input port:** HDL support is provided when you enable both **Enable reset input port** and **Delay reset action to next time step**. You must select Continuous operation mode.

### Input and Output Data Types.

- When **Decision type** is set to `Soft decision`, the HDL implementation of the Viterbi Decoder block supports fixed-point inputs and output. For input, the fixed-point data type must be `ufixN`, where N is the number of soft decision bits. Signed built-in data types (`int8`, `int16`, `int32`) are not supported. For output, the HDL implementation of the Viterbi Decoder block supports block-supported output data types.
- When **Decision type** is set to `Hard decision`, the block supports input with data types `ufix1` and `Boolean`. For output, the HDL implementation of the Viterbi Decoder block supports block-supported output data types.
- The HDL implementation of the Viterbi Decoder block does not support double and single input data types are not supported. The block does not support floating point output for fixed-point inputs.

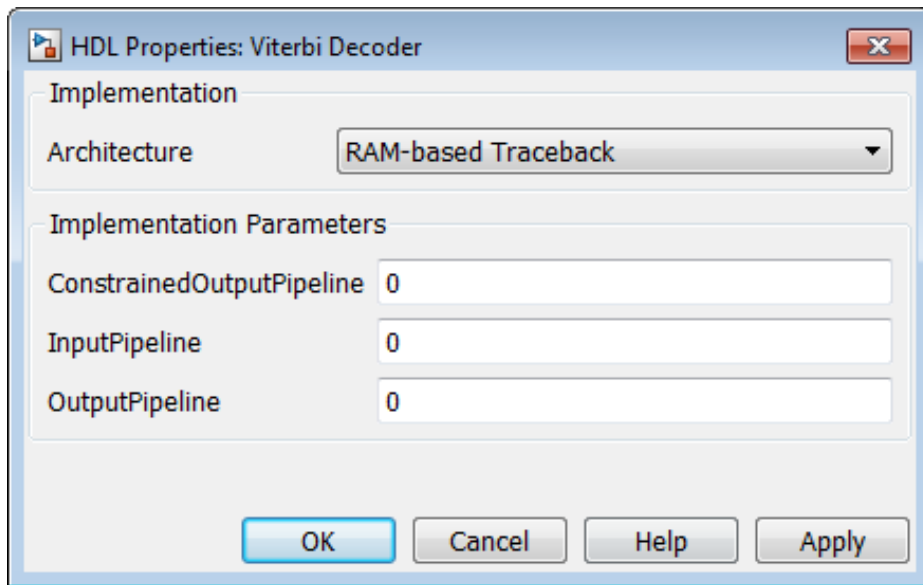
**Pipelining the Traceback Unit.** The Viterbi Decoder block decodes every bit by tracing back through a traceback depth that you define for the block. The block implements a complete traceback for each decision bit, using registers to store the minimum state index and branch decision in the traceback decoding unit. You can specify that the traceback decoding unit be pipelined in order to improve the speed of the generated circuit. You can add pipeline registers to the traceback unit by specifying the number of traceback stages per pipeline register. To do this, use the `TracebackStagesPerPipeline` implementation parameter.

The `TracebackStagesPerPipeline` implementation parameter lets you balance the circuit performance based on system requirements. A smaller parameter value indicates the requirement to add more registers to increase the speed of the traceback circuit. Increasing the number results in a lower number of registers along with a decrease in the circuit speed.

See the “HDL Code Generation for Viterbi Decoder” example model for an example using `TracebackStagesPerPipeline`.

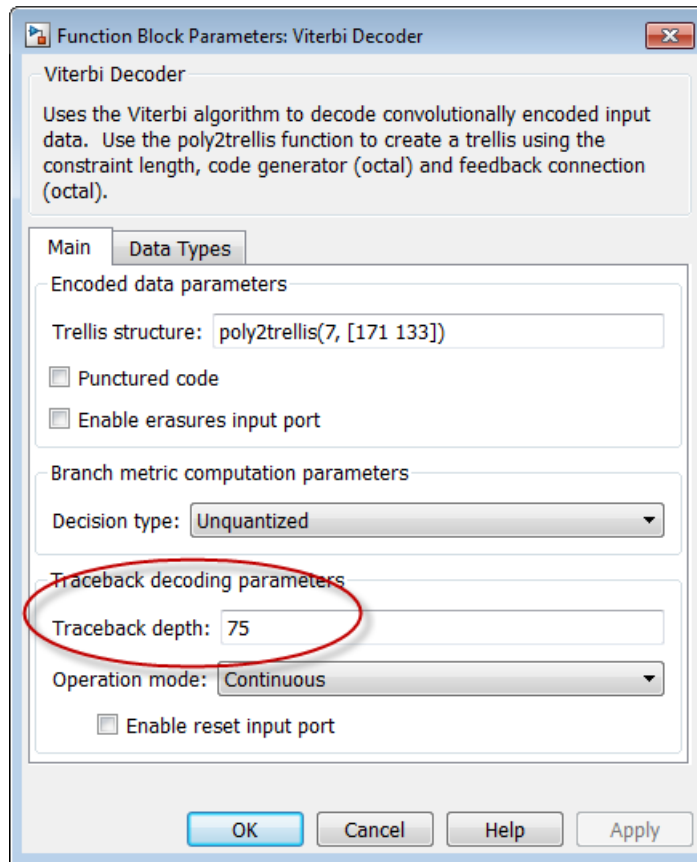
**RAM-Based Traceback.** Instead of using registers, you can choose to use RAMs to save the survivor branch information.

- 1 Set the HDL Architecture property of the Viterbi Decoder block to RAM-based Traceback.



2 Set the traceback depth on the Viterbi Decoder block mask.





RAM-based traceback and register-based traceback differ in the following ways:

- The RAM-based implementation traces back through one set of data to find the initial state to decode the previous set of data. The register-based implementation combines the traceback and decode operations into one step and uses the best state found from the minimum operation as the decoding initial state.
- RAM-based implementation traces back through  $M$  samples, decodes the previous  $M$  bits in reverse order, and releases one bit in order at each clock

cycle, whereas the register-based implementation decodes one bit after a complete traceback.

Because of the differences in the two traceback algorithms, the RAM-based implementation produces different numerical results than the register-based traceback. A longer traceback depth, for example, 10 times the constraint length, is recommended in the RAM-based traceback to achieve a similar bit error rate (BER) as the register-based implementation. The size of RAM required for the implementation depends on the trellis and the traceback depth.

See HDL Code Generation for Viterbi Decoder.

**Viterbi Decoder Example.** The “HDL Code Generation for Viterbi Decoder” example demonstrates HDL code generation for a fixed-point Viterbi Decoder block, with pipelined traceback decoding. To open the example, type the following command:

```
showdemo commviterbihdl_m
```

### Restrictions on Use of Blocks in the Test Bench

Blocks that belong to the blocksets and toolboxes in the following list should not be directly connected to the DUT. Instead, place them in a subsystem, and connect the subsystem to the DUT. This restriction applies to all blocks in the following products:

- SimRF™
- SimDriveline™
- SimEvents®
- SimMechanics™
- SimPowerSystems™
- Simscape™

## Block Implementation Parameters

### In this section...

“Overview” on page 9-49

“ConstMultiplierOptimization” on page 9-50

“CoeffMultipliers” on page 9-52

“Distributed Arithmetic Implementation Parameters for Digital Filter Blocks” on page 9-54

“DistributedPipelining” on page 9-66

“FlattenHierarchy” on page 9-77

“InputPipeline” on page 9-78

“LoopOptimization” on page 9-79

“MapPersistentVarsToRAM” on page 9-81

“OutputPipeline” on page 9-85

“Pipelining Implementation Parameters for Filter Blocks” on page 9-86

“RAM” on page 9-91

“ResetType” on page 9-92

“ShiftRegister” on page 9-94

“UseRAM” on page 9-96

“Speed vs. Area Optimizations for FIR Filter Implementations” on page 9-101

“Interface Generation Parameters” on page 9-108

### Overview

Block implementation parameters let you control details of the code generated for specific block implementations. See “Set and View HDL Block Parameters” on page 8-2 to learn how to select block implementations and parameters in the GUI or the command line.

Property names are strings. The data type of a property value is specific to the property. This section describes the syntax of each block implementation parameter and how the parameter affects generated code.

### ConstMultiplierOptimization

The ConstMultiplierOptimization implementation parameter lets you specify use of canonic signed digit (CSD) or factored CSD optimizations for processing coefficient multiplier operations in code generated for the following blocks:

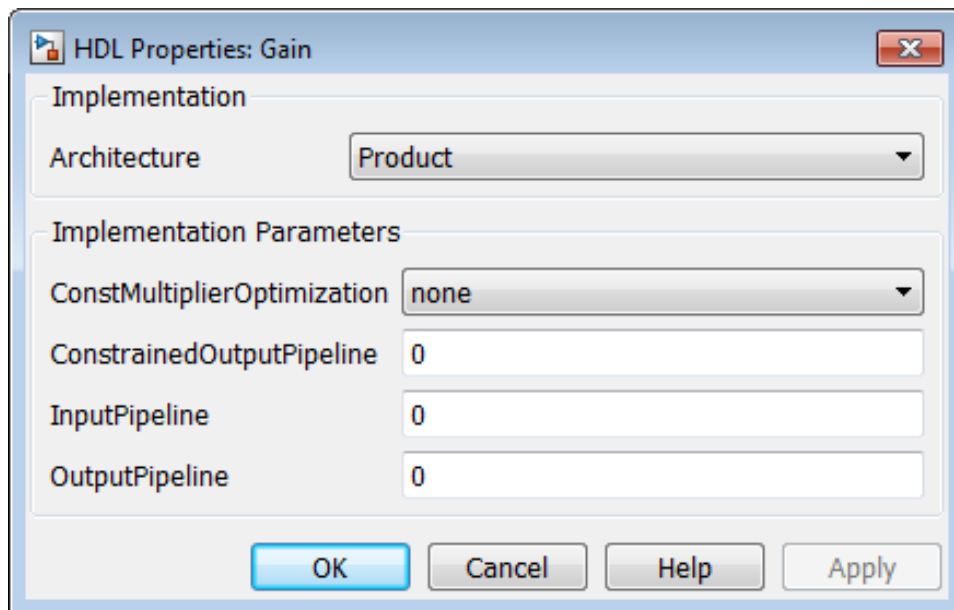
- Gain
- Stateflow® chart
- Truth Table
- MATLAB Function

The following table shows the ConstMultiplierOptimization parameter values.

Implementations	Parameters	Description
default	'ConstMultiplierOptimization', 'none' <i>(Default)</i>	By default, the coder does not perform CSD or FCSD optimizations. Code generated for the Gain block retains multiplier operations.
	'ConstMultiplierOptimization', 'CSD'	When you specify this option, the generated code decreases the area used by the model while maintaining or increasing clock speed, using canonic signed digit (CSD) techniques. CSD replaces multiplier operations with add and subtract operations. CSD minimizes
	'ConstMultiplierOptimization', 'FCSD'	This option uses factored CSD (FCSD) techniques, which replace multiplier operations with shift and add/subtract operations on certain factors of the operands. These factors are generally

Implementations	Parameters	Description
	'ConstMultiplierOptimization', 'auto'	<p>prime but can also be a number close to a power of 2, which favors area reduction. This option lets you achieve a greater area reduction than CSD, at the cost of decreasing clock speed.</p> <p>When you specify this option, the coder chooses between the CSD or FCSD optimizations. The coder chooses the optimization that yields the most area-efficient implementation, based on the number of adders required. When you specify 'auto', the coder does not use multipliers, unless conditions are such that CSD or FCSD optimizations are not possible (for example, if the design uses floating-point arithmetic).</p>

The following figure shows the ConstMultiplierOptimization option in the HDL Block properties dialog box.

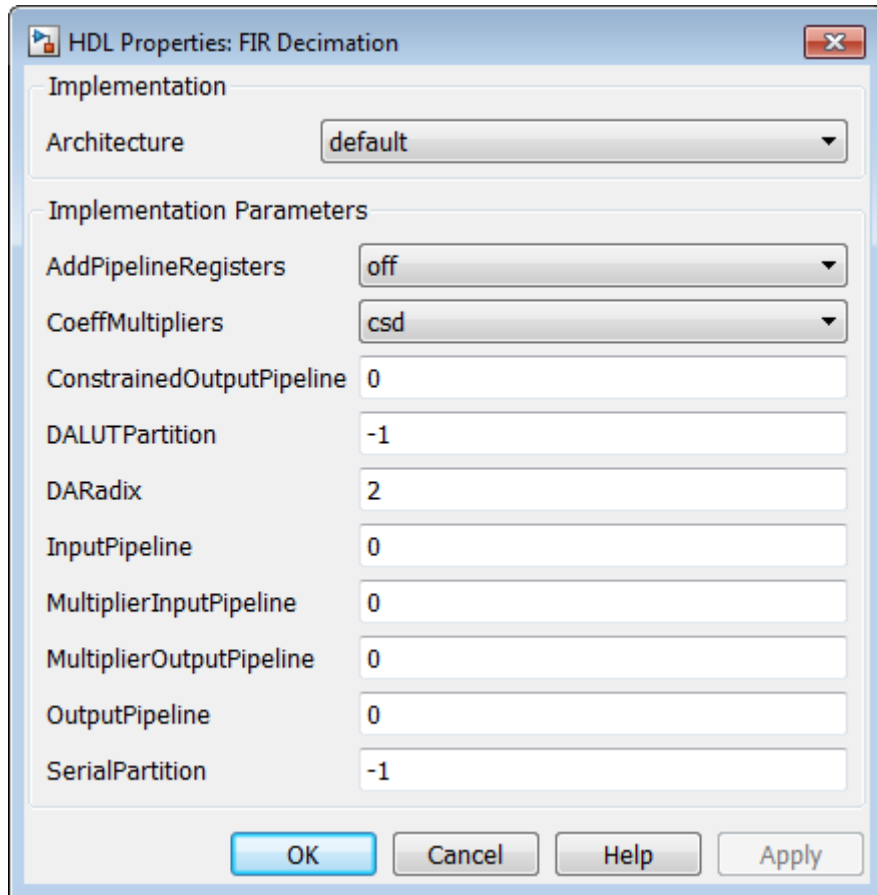


## CoeffMultipliers

The `CoeffMultipliers` implementation parameter lets you specify use of canonic signed digit (CSD) or factored CSD optimizations for processing coefficient multiplier operations in code generated for certain filter blocks. Specify the `CoeffMultipliers` parameter using one of the following options:

- `'csd'`: Use CSD techniques to replace multiplier operations with shift and add operations. CSD techniques minimize the number of addition operations required for constant multiplication by representing binary numbers with a minimum count of nonzero digits. This representation decreases the area used by the filter while maintaining or increasing clock speed.
- `'factored-csd'`: Use factored CSD techniques, which replace multiplier operations with shift and add operations on prime factors of the coefficients. This option lets you achieve a greater filter area reduction than CSD, at the cost of decreasing clock speed.
- `'multipliers'` (default): Retain multiplier operations.

In the following figure, the HDL Block Properties dialog box specifies that code generated for a FIR Decimation block in the model uses the CSD optimization.



The coder supports `CoeffMultipliers` for the filter block implementations shown in the following table.

Block	Implementation
dsparch4/Biquad Filter	default
dsparch4/Digital Filter	default

Block	Implementation
dspmlti4/FIR Decimation	default
dspmlti4/FIR Interpolation	default
simulink/Discrete/Discrete FIR Filter	default

## Distributed Arithmetic Implementation Parameters for Digital Filter Blocks

Distributed Arithmetic (DA) is a widely used technique for implementing sum-of-products computations without the use of multipliers. Designers frequently use DA to build efficient Multiply-Accumulate Circuitry (MAC) for filters and other DSP applications.

The main advantage of DA is its high computational efficiency. DA distributes multiply and accumulate operations across shifters, lookup tables (LUTs) and adders in such a way that conventional multipliers are not required.

The coder supports distributed arithmetic (DA) implementations for the blocks described in the following table.

Block	Implementation	FIR Structures That Support DA
dsparch4/Digital Filter	default	<ul style="list-style-type: none"> <li>• dfilt.dffir</li> <li>• dfilt.dfsymfir</li> <li>• dfilt.dfasymdir</li> </ul>
simulink/Discrete/Discrete FIR Filter	default	<ul style="list-style-type: none"> <li>• dfilt.dffir</li> <li>• dfilt.dfsymfir</li> <li>• dfilt.dfasymdir</li> </ul>



<b>Block</b>	<b>Implementation</b>	<b>FIR Structures That Support DA</b>
dspmlti4/FIR Decimation	default	mfilt.firdecim
dspmlti4/FIR Interpolation	Fully Parallel (default) Partly Serial Fully Serial Distributed Arithmetic (DA)	mfilt.firinterp

This section briefly summarizes the operation of DA. For references on the theoretical foundations of DA, see “Further References” on page 9-65.

In a DA realization of a FIR filter structure, a sequence of input data words of width  $W$  is fed through a parallel to serial shift register, producing a serialized stream of bits. The serialized data is then fed to a bit-wide shift register. This shift register serves as a delay line, storing the bit serial data samples.

The delay line is tapped (based on the input word size  $W$ ), to form a  $W$ -bit address that indexes into a lookup table (LUT). The LUT stores all possible sums of partial products over the filter coefficients space. The LUT is followed by a shift and adder (scaling accumulator) that adds the values obtained from the LUT sequentially.

A table lookup is performed sequentially for each bit (in order of significance starting from the LSB). On each clock cycle, the LUT result is added to the accumulated and shifted result from the previous cycle. For the last bit (MSB), the table lookup result is subtracted, accounting for the sign of the operand.

This basic form of DA is fully serial, operating on one bit at a time. If the input data sequence is  $W$  bits wide, then a FIR structure takes  $W$  clock cycles

to compute the output. Symmetric and asymmetric FIR structures are an exception, requiring  $W+1$  cycles, because one additional clock cycle is needed to process the carry bit of the preadders.

### Improving Performance with Parallelism

The inherently bit-serial nature of DA can limit throughput. To improve throughput, the basic DA algorithm can be modified to compute more than one bit sum at a time. The number of simultaneously computed bit sums is expressed as a power of two called the *DA radix*. For example, a DA radix of 2 ( $2^1$ ) indicates that one bit sum is computed at a time; a DA radix of 4 ( $2^2$ ) indicates that two bit sums are computed at a time, and so on.

To compute more than one bit sum at a time, the LUT is replicated. For example, to perform DA on 2 bits at a time (radix 4), the odd bits are fed to one LUT and the even bits are simultaneously fed to an identical LUT. The LUT results corresponding to odd bits are left-shifted before they are added to the LUT results corresponding to even bits. This result is then fed into a scaling accumulator that shifts its feedback value by 2 places.

Processing more than one bit at a time introduces a degree of parallelism into the operation, improving speed at the expense of area. You can control the degree of parallelism by specifying the *DARadix* implementation parameter. *DARadix* lets you specify the number of bits processed simultaneously in DA (see “*DARadix* Implementation Parameter” on page 9-63).

### Reducing LUT Size

The size of the LUT grows exponentially with the order of the filter. For a filter with  $N$  coefficients, the LUT must have  $2^N$  values. For higher order filters, LUT size must be reduced to reasonable levels. To reduce the size, you can subdivide the LUT into a number of LUTs, called *LUT partitions*. Each LUT partition operates on a different set of taps. The results obtained from the partitions are summed.

For example, for a 160-tap filter, the LUT size is  $(2^{160}) * W$  bits, where  $W$  is the word size of the LUT data. Dividing this into 16 LUT partitions, each taking 10 inputs (taps), the total LUT size is reduced to  $16 * (2^{10}) * W$  bits.

Although LUT partitioning reduces LUT size, more adders are required to sum the LUT data.

You control how the LUT is partitioned in DA by specifying the `DALUTPartition` implementation parameter (see “`DALUTPartition Implementation Parameter`” on page 9-57).

### **Requirements and Considerations for Generating Distributed Arithmetic Code**

You can control how DA code is generated by using the `DALUTPartition` and `DARadix` implementation parameters. Before using these parameters, review the following general requirements, restrictions, and other considerations for generation of DA code.

**Requirements Specific to Filter Type.** The `DALUTPartition` and `DARadix` parameters have certain requirements and restrictions that are specific to different filter types. These requirements are included in the discussions of each parameter:

- “`DALUTPartition Implementation Parameter`” on page 9-57
- “`DARadix Implementation Parameter`” on page 9-63

**Fixed-Point Quantization Required.** Generation of DA code is supported only for fixed-point filter designs.

**Specifying Filter Precision.** The data path in HDL code generated for the DA architecture is carefully optimized for full precision computations. The filter result is cast to the output data size only at the final stage when it is presented to the output.

Distributed arithmetic merges the product and accumulator operations and does computations at full precision. This approach ignores the **Product output** and **Accumulator** properties of the Digital Filter block and sets these properties to full precision.

### **DALUTPartition Implementation Parameter**

`DALUTPartition` enables DA code generation and specifies the number and size of LUT partitions used for DA.

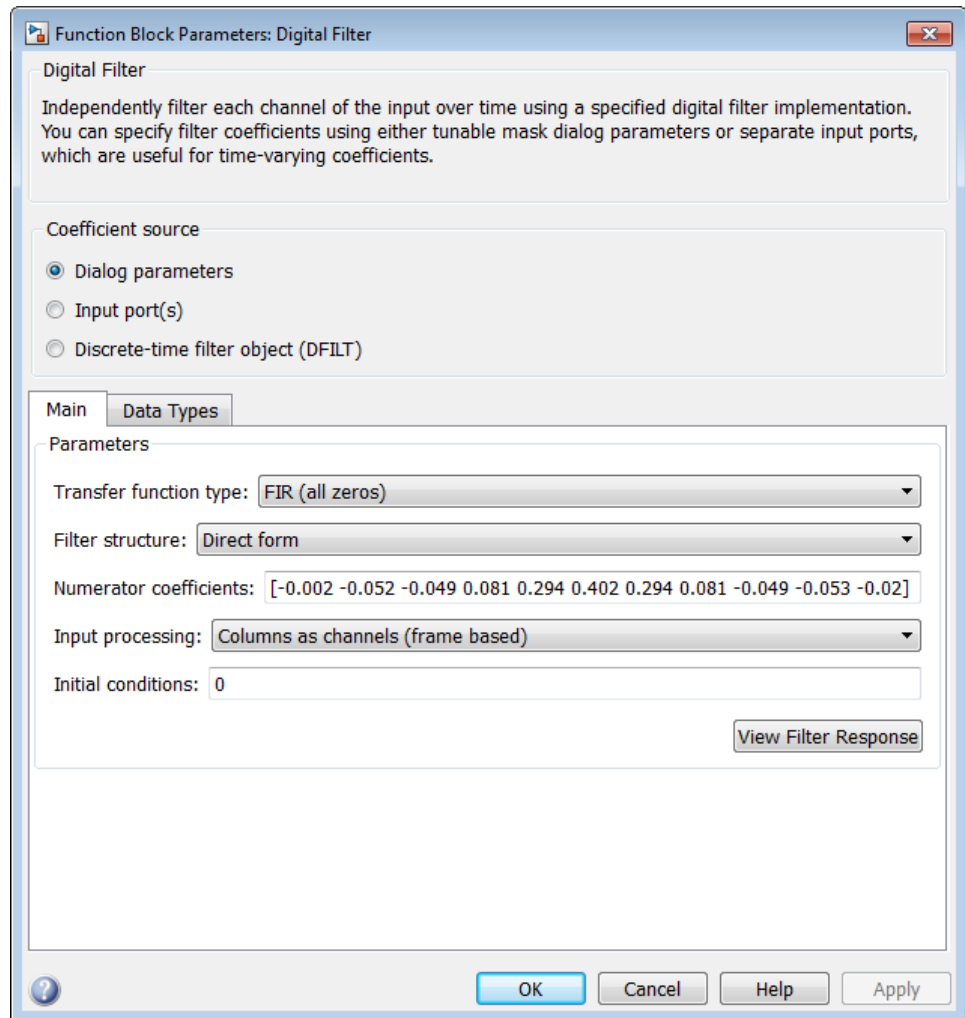
Specify LUT partitions as a vector of integers [p1 p2 . . . pN] where:

- N is the number of partitions.
- Each vector element specifies the size of a partition. The maximum size for an individual partition is 12.
- The sum of all vector elements equals the filter length FL. FL is calculated differently depending on the filter type (see “Specifying DALUTPartition for Single-Rate Filters” on page 9-58).

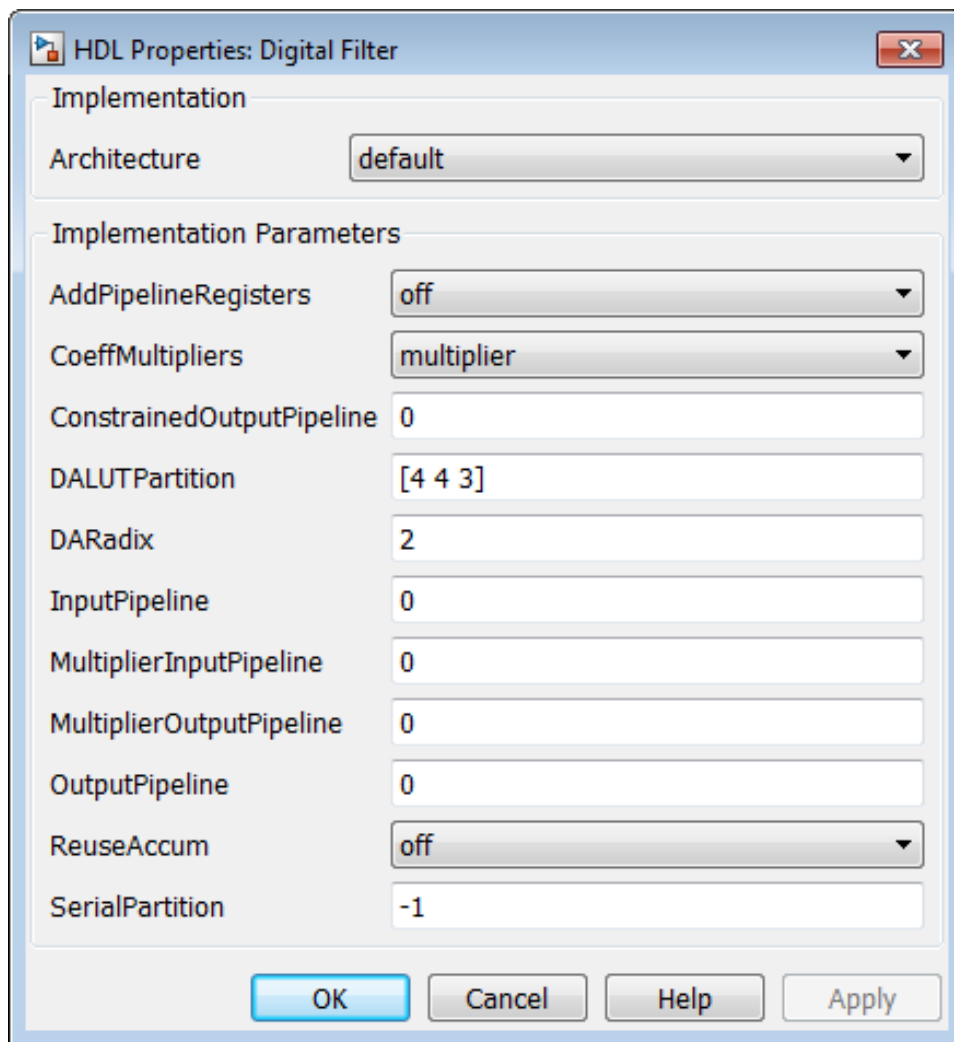
**Specifying DALUTPartition for Single-Rate Filters.** To determine the LUT partition for one of the supported single-rate filter types, calculate FL as shown in the following table. Then, specify the partition as a vector whose elements sum to FL.

Filter Type	Filter Length (FL) Calculation
dfilt.dffir	FL = length(find(Hd.numerator~= 0))
dfilt.dfsymfir dfilt.dfasymfir	FL = ceil(length(find(Hd.numerator~= 0))/2)

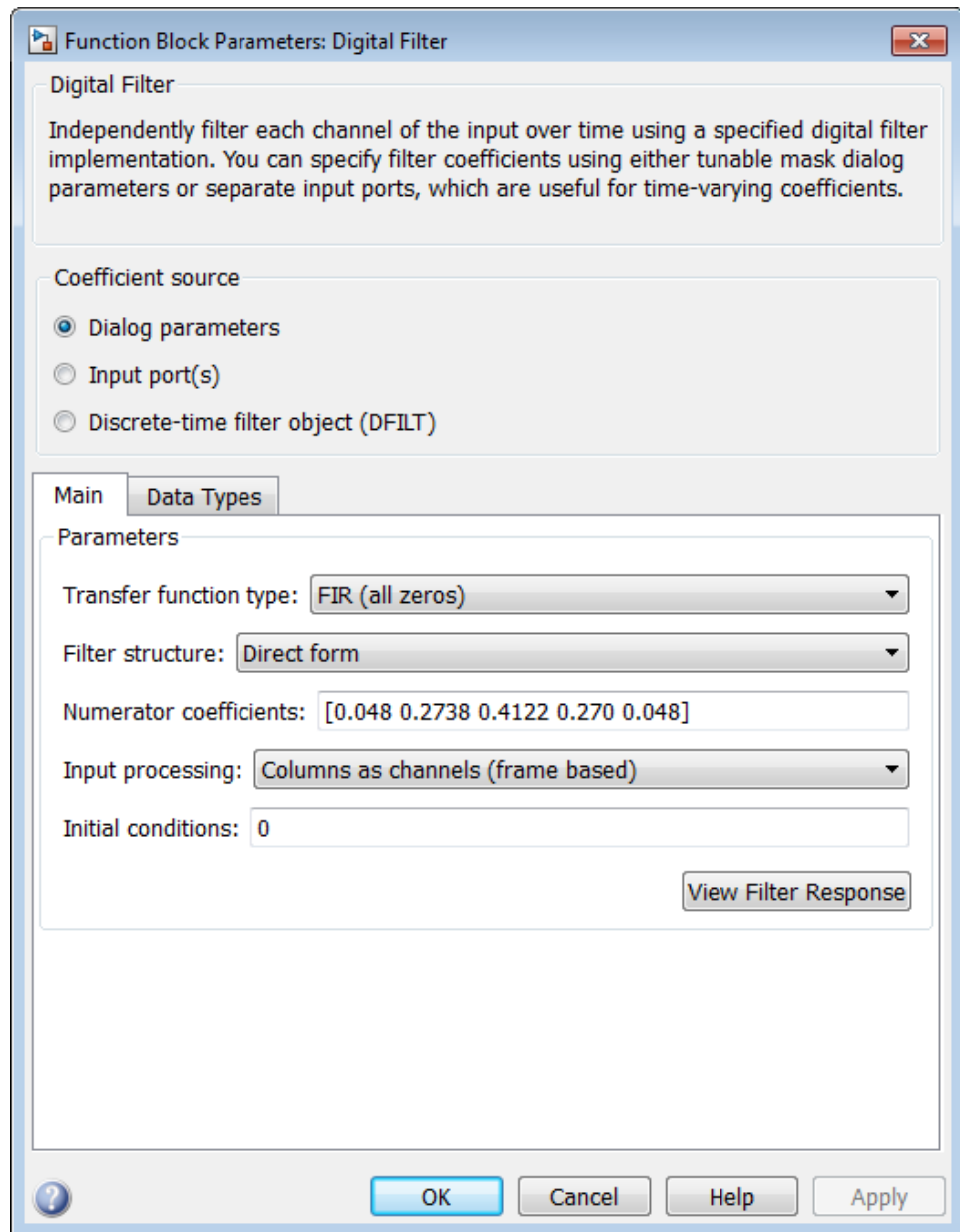
The following figure shows a Digital Filter configured for a direct form FIR filter of length 11.



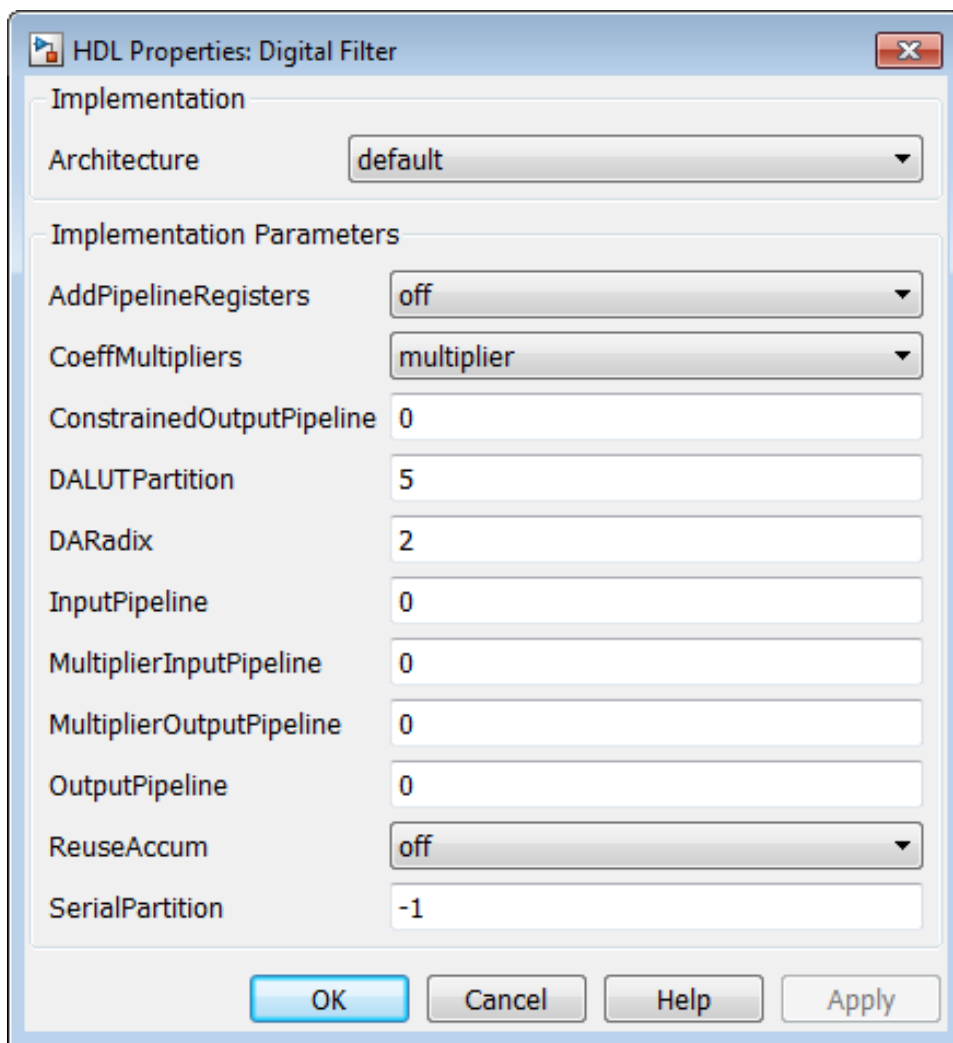
The following figure shows how to set one possible LUT partitioning for this filter:



You can also specify generation of DA code for your filter design without LUT partitioning. To do so, specify a vector of one element, whose value is equal to the filter length. For example, the following figure shows a Digital Filter configuration for a direct form FIR filter of length 5.



The following figure shows how to specify a partition that is equal to the filter length.



**Specifying DALUTPartition for Multirate Filters.** For supported multirate filters (`mfilt.firdecim` and `mfilt.firinterp`), you can specify the LUT partition as



- A vector defining a partition for LUTs for all polyphase subfilters.
- A matrix of LUT partitions, where each row vector specifies a LUT partition for a corresponding polyphase subfilter. In this case, the FL is uniform for all subfilters. This approach provides a fine control for partitioning each subfilter.

The following table shows the FL calculations for each type of LUT partition.

LUT Partition Specified As...	Filter Length (FL) Calculation
<i>Vector</i> : determine FL as shown in the <b>Filter Length (FL) Calculation</b> column to the right. Specify the LUT partition as a vector of integers whose elements sum to FL.	FL = size(polyphase(Hm), 2)
<i>Matrix</i> : determine the subfilter length FL <sub><i>i</i></sub> based on the polyphase decomposition of the filter, as shown in the <b>Filter Length (FL) Calculation</b> column to the right. Specify the LUT partition for each subfilter as a row vector whose elements sum to FL <sub><i>i</i></sub> .	<pre>p = polyphase(Hm); FL<sub><i>i</i></sub> = length(find(p(<i>i</i>,:)));</pre> <p>where <i>i</i> is the index to the <i>i</i>th row of the polyphase matrix of the multirate filter. The <i>i</i>th row of the matrix <i>p</i> represents the <i>i</i>th subfilter.</p>

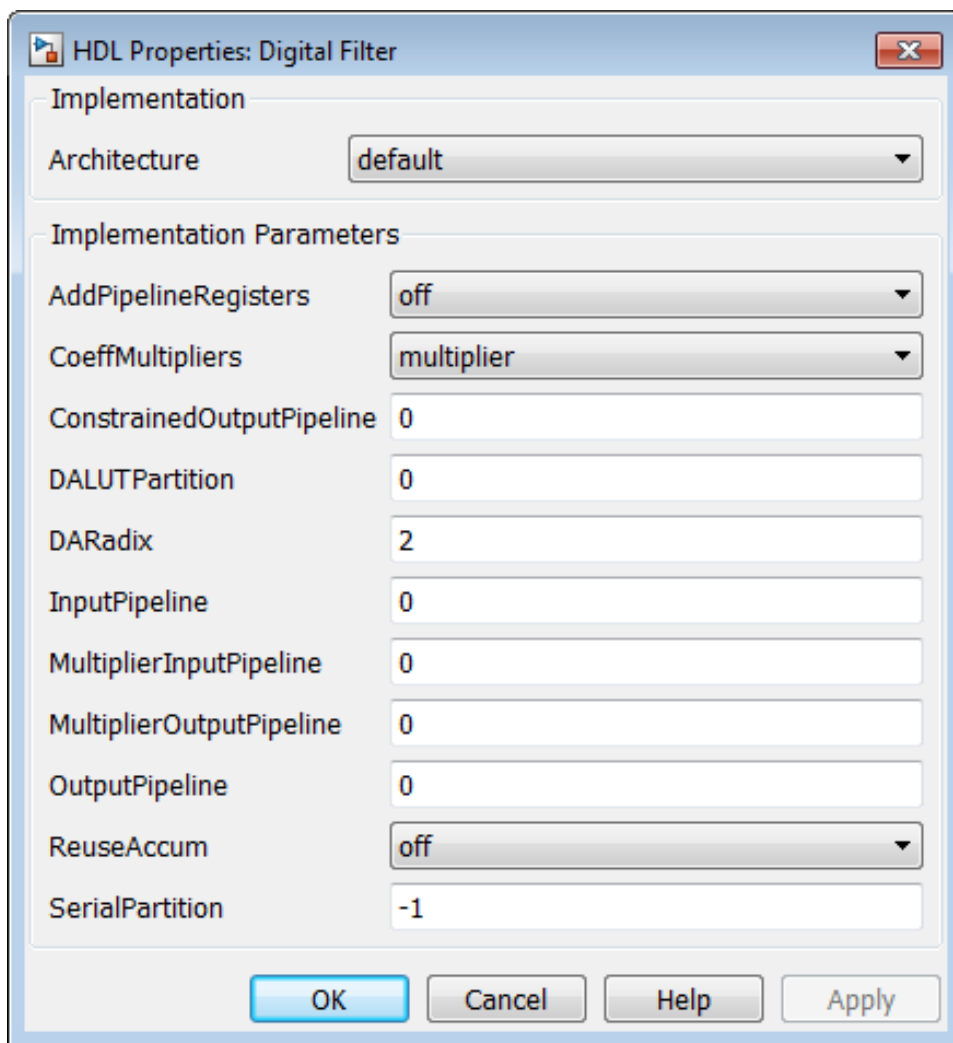
### DARadix Implementation Parameter

DARadix specifies the number of bits processed simultaneously in DA. The number of bits is expressed as *N*, which must be:

- A nonzero positive integer that is a power of two
- Such that  $\text{mod}(W, \log_2(N)) = 0$ , where *W* is the input word size of the filter

The default value for *N* is 2, specifying processing of one bit at a time, or fully serial DA, which is slow but low in area. The maximum value for *N* is  $2^W$ , where *W* is the input word size of the filter. This maximum specifies fully parallel DA, which is fast but high in area. Values of *N* between these extrema specify partly serial DA.

You can set the DARadix implementation parameter in the HDL Properties dialog for a filter block as shown in the following figure.



---

**Note** When setting a `DARadix` value for symmetrical (`dfilt.dfsymfir`) and asymmetrical (`dfilt.dfasymfir`) filters, see “Considerations for Symmetrical and Asymmetrical Filters” on page 9-65.

---

## Special Cases

**Coefficients with Zero Values.** DA ignores taps that have zero-valued coefficients and reduces the size of the DA LUT accordingly.

**Considerations for Symmetrical and Asymmetrical Filters.** For symmetrical (`dfilt.dfsymfir`) and asymmetrical (`dfilt.dfasymfir`) filters:

- A bit-level preadder or presubtractor is required to add tap data values that have coefficients of equal value and/or opposite sign. One extra clock cycle is required to compute the result because of the additional carry bit.
- The coder takes advantage of filter symmetry where possible. This reduces the DA LUT size substantially, because the effective filter length for these filter types is halved.

**Holding Input Data in a Valid State.** In filters with a DA architecture, data can be delivered to the outputs  $N$  cycles ( $N \geq 2$ ) later than the inputs. You can use the `HoldInputDataBetweenSamples` model property to determine how long (in terms of clock cycles) input data values are held in a valid state, as follows:

- When `HoldInputDataBetweenSamples` is set 'on' (the default), input data values are held in a valid state across  $N$  clock cycles.
- When `HoldInputDataBetweenSamples` is set 'off', data values are held in a valid state for only one clock cycle. For the next  $N-1$  cycles, data is in an unknown state (expressed as 'X') until the next input sample is clocked in.

**Further References.** Detailed discussions of the theoretical foundations of DA appear in the following publications:

- Meyer-Baese, U., *Digital Signal Processing with Field Programmable Gate Arrays*, Second Edition, Springer, pp 88–94, 128–143

- White, S.A., *Applications of Distributed Arithmetic to Digital Signal Processing: A Tutorial Review*. IEEE ASSP Magazine, Vol. 6, No. 3

## Distributed Pipelining

The DistributedPipelining implementation parameter supports *distributed pipeline insertion*, an optimization that lets you achieve higher clock rates in your HDL applications. (Higher clock rates come at the cost of some amount of latency due to the introduction of pipeline registers.)

You can apply distributed pipeline insertion when generating HDL code for the following blocks:

- Subsystems
- MATLAB Function blocks within a subsystem
- Stateflow charts within a subsystem

The coder performs distributed pipeline insertion when you specify both of the following implementation parameters for subsystems, MATLAB Function blocks, or Stateflow charts:

- {'OutputPipeline', nStages} : the number of pipeline stages (nStages) must be greater than zero.)
- {'DistributedPipelining', 'on'}: enables distributed pipeline insertion. (The default value for DistributedPipelining is 'off'.)

Under these conditions, the coder distributes pipeline stages in the generated code, rather than generating pipeline stages at the outputs of the HDL code. The nStages argument defines the number of pipeline stages to insert or distribute.

In a small number of cases, the coder generates conventional output pipeline registers, even if you specify {'DistributedPipelining', 'on'}. See “Limitations of Distributed Pipelining” on page 9-73.

The following table summarizes the combined effect of the DistributedPipelining and OutputPipeline parameters.

<b>DistributedPipelining</b>	<b>OutputPipeline, nStages</b>	<b>Result</b>
'off' (default)	Unspecified (nStages defaults to 0)	The coder does not insert pipeline registers.
	nStages > 0	The coder inserts nStages output registers at the output of the subsystem, MATLAB Function block, or Stateflow chart.
'on'	Unspecified (nStages defaults to 0)	The coder does not insert pipeline registers. DistributedPipelining has no effect.
	nStages > 0	The coder distributes nStages registers inside the subsystem, MATLAB Function block, or Stateflow chart, based on critical path analysis.

To achieve further optimization of code generated with distributed pipelining, perform retiming during RTL synthesis, if possible.

---

**Tip** When using pipelined block implementations, output data might be in an invalid state for some initial number of samples. To avoid spurious test bench errors, determine this number of samples. Then set the **Ignore output data checking (number of samples)** option (or the `IgnoreDataChecking` property, if you are using the command-line interface) accordingly. For more information see:

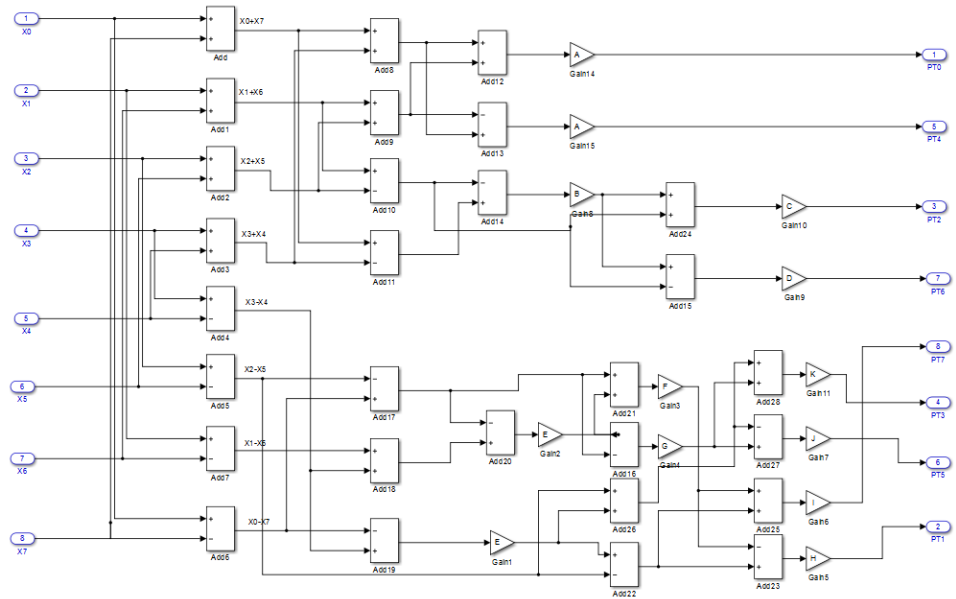
- “Ignore output data checking (number of samples)” on page 7-97
  - `IgnoreDataChecking`
- 

### **Example: Distributed Pipeline Insertion in a Subsystem**

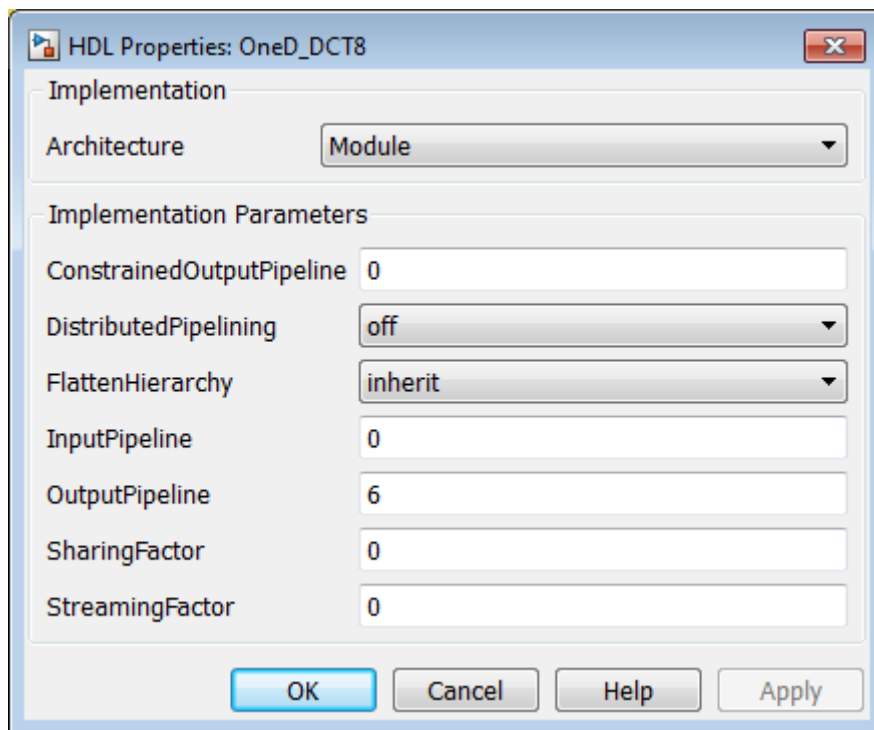
This example uses the `dct8_fixed` model to show how the coder distributes pipeline registers in a subsystem when you specify:

- Output pipelining
- Distributed pipeline insertion

Open the model by typing `dct8_fixed` at the MATLAB prompt. The DUT of the model (`dct8_fixed/OneD_DCT8`) looks like this figure.

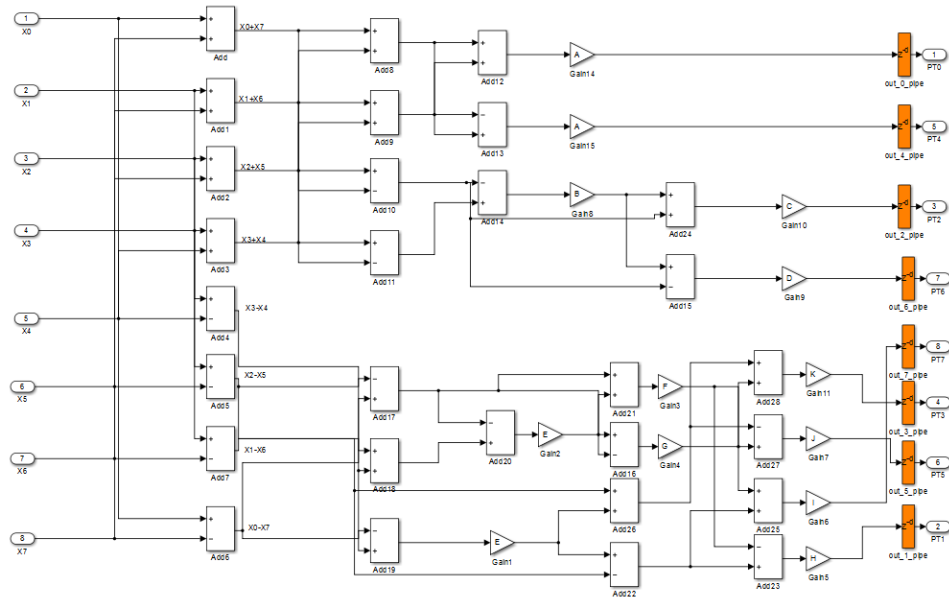


Setting **DistributedPipelining** to off and **OutputPipeline** to 6 specifies insertion of 6 pipeline stages at the outputs of the DUT.

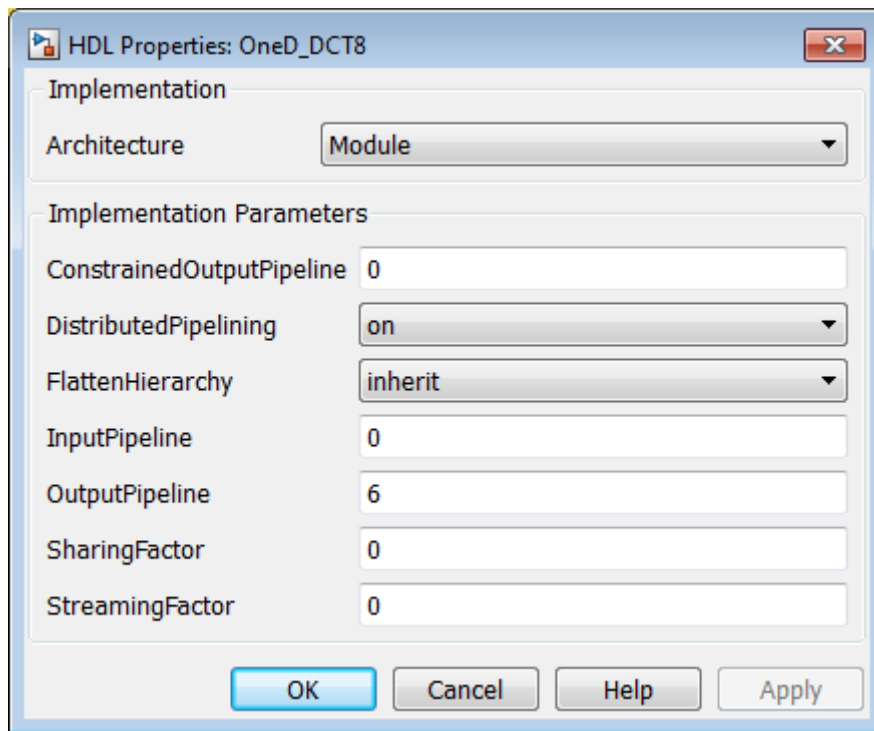


The generated model shows the placement of pipeline registers (highlighted delays) at the outputs of the DUT. (If you are unfamiliar with generated models, see “What is a Generated Model?” on page 12-2.)

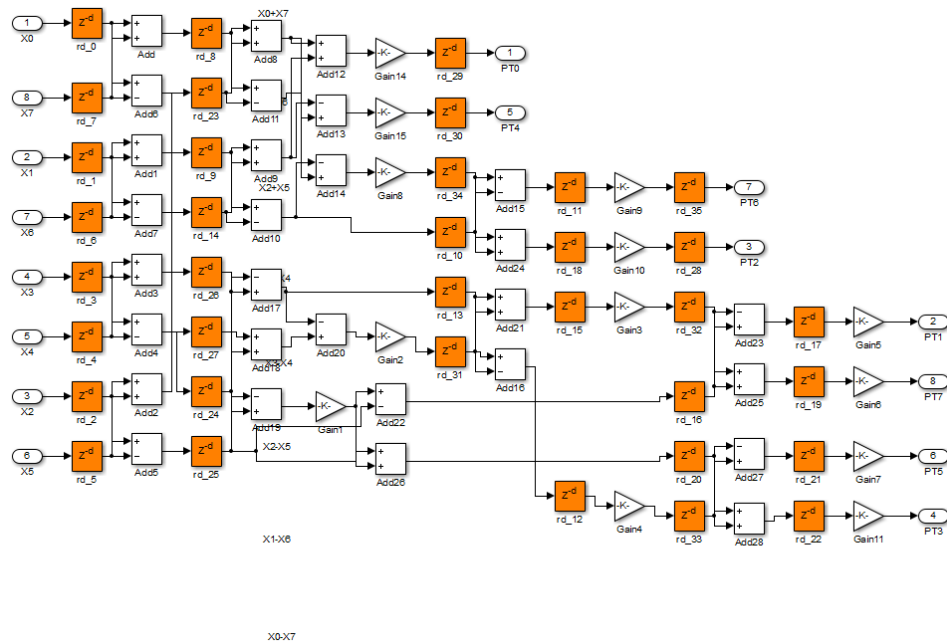




Setting **DistributedPipelining** to on and **OutputPipeline** to 6 specifies distribution of 6 pipeline stages for each signal path in the DUT.



The generated model shows the distribution of pipeline registers (highlighted delays) at internal points within each signal path. The total number of pipeline registers for each path is 6.



## Limitations of Distributed Pipelining

The following limitations apply to distributed pipeline insertion:

- If a MATLAB Function block or Stateflow chart contains a matrix with a statically unresolvable index, the coder generates pipeline registers at the outputs.
- If a Stateflow chart contains a state or local variable, the coder generates pipeline registers at the outputs.
- The latencies of the operations that you choose are approximate. Therefore, pipelining results might not be optimal in cases where the relative operation latencies in the target platform do not match the trend of the chosen latencies.
- If you specify 'DistributedPipelining', 'on' for a subsystem that contains any of the blocks in the following list, the coder issues an error message and terminates code generation.

To enable code generation to proceed, place these blocks inside one or more subsystems:

- Tapped Delay
- M-PSK Demodulator Baseband
- M-PSK Modulator Baseband
- QPSK Demodulator Baseband
- QPSK Modulator Baseband
- BPSK Demodulator Baseband
- BPSK Modulator Baseband
- PN Sequence Generator
- dspsigops/Repeat
- HDL Counter
- dspadpt3/LMS Filter
- dspsrcs4/Sine Wave
- commcnvcod2/Viterbi Decoder
- Triggered Subsystem
- Counter Limited
- Counter Free-Running
- Frame Conversion
- The following blocks allow 'DistributedPipelining', 'on', but the coder treats them in the same way as it treats nested subsystems. That is, the coder distributes pipeline registers around nested Subsystem blocks.
  - Sum (Cascade implementation)
  - Product (Cascade implementation)
  - MinMax (Cascade implementation)
  - Upsample
  - Downsample
  - Rate Transition

- Zero-Order Hold
- Reciprocal Sqrt (RecipSqrtNewton implementation)
- Trigonometric Function (CORDIC Approximation)
- Single Port RAM
- Dual Port RAM
- Simple Dual Port RAM

### **Effects of Hierarchical Distributed Pipelining**

The coder supports a model-level property, `HierarchicalDistPipelining`, which is `off` by default.

- If `HierarchicalDistPipelining` is `on`, the coder distributes pipeline registers hierarchically down until `DistributedPipelining` is `off` for a given subsystem. The coder preserves the original subsystem hierarchy, which enables you to trace the changes that occur during pipelining for nested Subsystem blocks.
- If `HierarchicalDistPipelining` is `off`, distribution happens only within a subsystem. The coder distributes pipeline registers around nested Subsystem blocks.

If you set the `OptimizationReport` property to `on`, the coder adopts an enhanced reporting mechanism to provide the following information:

- If `HierarchicalDistPipelining` is `on`, the Optimization Report uses colored sections to distinguish between different regions where the coder applies hierarchical distributed pipelining:

## Detailed Report

### Hierarchical distributed pipelining region 1:

Status for hierarchical distributed pipelining starting at [Hlp](#) : Distributed pipelining successful.

#### Details within this hierarchical distributed pipelining region:

Subsystem: [Hlp](#)

*Implementation Parameters: DistributedPipelining: 'on'; InputPipeline: 0; OutputPipeline: 0*

**Before Distributed Pipelining : 2 registers (32 flip-flops)**

Registers	Count
16-bit	2

**After Distributed Pipelining : 1 registers (16 flip-flops)**

Registers	Count
16-bit	1

Subsystem: [Section1](#)

*Implementation Parameters: DistributedPipelining: 'on'; InputPipeline: 0; OutputPipeline: 0*

**Before Distributed Pipelining : 0 registers (0 flip-flops)**

**After Distributed Pipelining : 9 registers (288 flip-flops)**

Registers	Count
32-bit	9

- If distributed pipelining fails, the coder gives you information that might help you fix the failure mode.

### See Also

“Distributed Pipeline Insertion for MATLAB Function Blocks” on page 17-42

## FlattenHierarchy

FlattenHierarchy enables you to remove subsystem hierarchy from the HDL code generated from your design.

The FlattenHierarchy options for a subsystem are listed in the following table.

FlattenHierarchy Setting	Description
'inherit' (default)	Use the hierarchy flattening setting of the parent subsystem. If this
'on'	Flatten this subsystem.
'off'	Do not flatten this subsystem, even if the parent subsystem is flattened.

## Prerequisites For Hierarchy Flattening

To flatten hierarchy, a subsystem must have the following block properties.

Property	Required value
DistributedPipelining	'off'
StreamingFactor	0
SharingFactor	0

To flatten hierarchy, you must also have the MaskParameterAsGeneric global property set to 'off'. For more information, see MaskParameterAsGeneric.

## How To Flatten Hierarchy

To set hierarchy flattening using the HDL Block Properties dialog box:

- 1** Right-click the subsystem.
- 2** Select **HDL Code > HDL Block Properties** .
- 3** For **FlattenHierarchy**, select **on**, **off**, or **inherit**.

To set hierarchy flattening from the command line, use `hdlset_param`. For example, to turn on hierarchy flattening for a subsystem, `my_dut`:

```
hdlset_param('my_dut', 'FlattenHierarchy', 'on')
```

See also `hdlset_param`.

### Limitations For Hierarchy Flattening

A subsystem cannot be flattened if the subsystem is:

- Atomic and instantiated in the design more than once.
- A black box implementation or model reference.
- An enabled or triggered subsystem.

---

**Note** This option removes subsystem boundaries before code generation. It does not necessarily generate HDL code with a completely flat hierarchy.

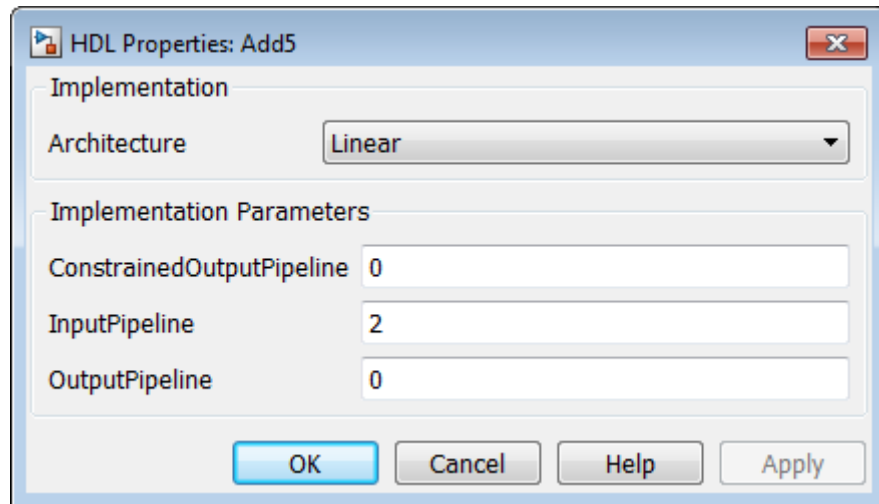
---

### InputPipeline

`InputPipeline` lets you specify a implementation with input pipelining for selected blocks. The parameter value specifies the number of input pipeline stages (pipeline depth) in the generated code.

The following figure shows the `InputPipeline` parameter set to 2 in the HDL Properties dialog box for an Add block .





The following code specifies an input pipeline depth of two stages for each Sum block in the model:

```
sblocks = find_system(gcb, 'BlockType', 'Sum');
for ii=1:length(sblocks),hdlset_param(sblocks{ii},'InputPipeline', 2), end;
```

When generating code for pipeline registers, the coder appends a postfix string to names of input or output pipeline registers. The default postfix string is `_pipe`. To customize the postfix string, use the **Pipeline postfix** option in the **Global Settings / General** pane in the **HDL Code** pane of the Model Configuration Parameters dialog box. Alternatively, you can pass the desired postfix string in the `makehdl` property `PipelinePostfix`. See `PipelinePostfix` for an example.

## LoopOptimization

LoopOptimization enables you to stream or unroll loops in code generated from a MATLAB Function block. Loop streaming optimizes for area; loop unrolling optimizes for speed.

The LoopOptimization options for the MATLAB Function block are listed in the following table.

LoopOptimization Setting	Description
'none' (default)	Do not optimize loops.
'Unrolling'	Unroll loops.
'Streaming'	Stream loops.

### How to Optimize MATLAB Function Block For Loops

To select a loop optimization using the HDL Block Properties dialog box:

- 1 Right-click the MATLAB Function block.
- 2 Select **HDL Code > HDL Block Properties** .
- 3 For **LoopOptimization**, select **none**, **Unrolling**, or **Streaming**.

To select a loop optimization from the command line, use `hdlset_param`. For example, to turn on loop streaming for a MATLAB Function block, `my_m1fn`:

```
hdlset_param('my_m1fn', 'LoopOptimization', 'Streaming')
```

See also `hdlset_param`.

### Limitations for MATLAB Function Block Loop Optimization

The coder cannot stream a loop if:

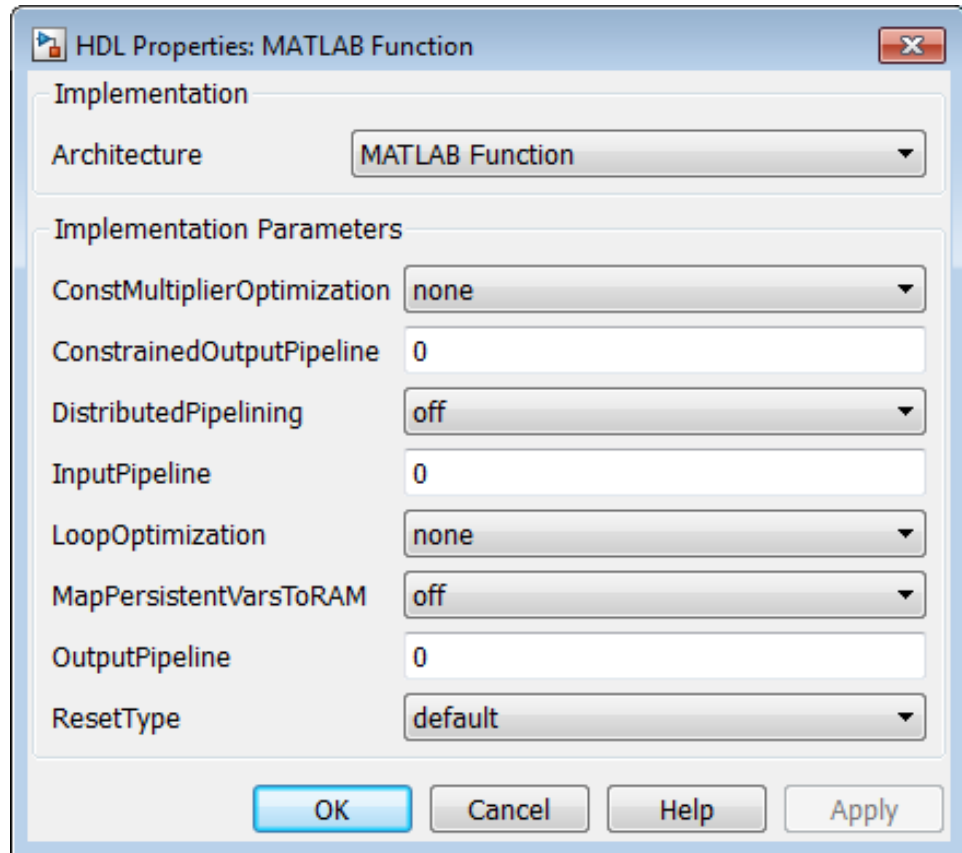
- The loop index counts down. The loop index must increase by 1 on each iteration.
- There are 2 or more nested loops at the same level of hierarchy within another loop.
- Any particular persistent variable is updated both inside and outside a loop.

The coder can stream a loop when the persistent variable is:

- Updated inside the loop and read outside the loop.
- Read within the loop and updated outside the loop.

## MapPersistentVarsToRAM

With the `MapPersistentVarsToRAM` implementation parameter, you can use RAM-based mapping for persistent arrays of a MATLAB Function block instead of mapping to registers.



## Mapping Behavior for Persistent Arrays

MapPersistentVarsToRAM Setting	Mapping Behavior
off	Persistent arrays map to registers in the generated HDL code.
on	<p>A persistent array maps to a block RAM when all of the following conditions are true:</p> <ul style="list-style-type: none"> <li>• Access to the array must be in unconditional code paths.</li> <li>• Each read or write access is for a single element only. For example, submatrix access and array copies are not allowed.</li> <li>• Address computation logic is not read-dependent. For example, computation of a read or write address using the data read from the array is not allowed.</li> <li>• RAMSize is greater than or equal to the RAMMappingThreshold value. RAMSize is the product NumElements * WordLength * Complexity. <ul style="list-style-type: none"> <li>▪ NumElements is the number of elements in the array.</li> <li>▪ WordLength is the number of bits that represent the data type of the array.</li> <li>▪ Complexity is 2 for arrays with a complex base type; 1 otherwise.</li> </ul> </li> </ul> <p>If any of the above conditions is false, the persistent array maps to a register in the HDL code.</p>

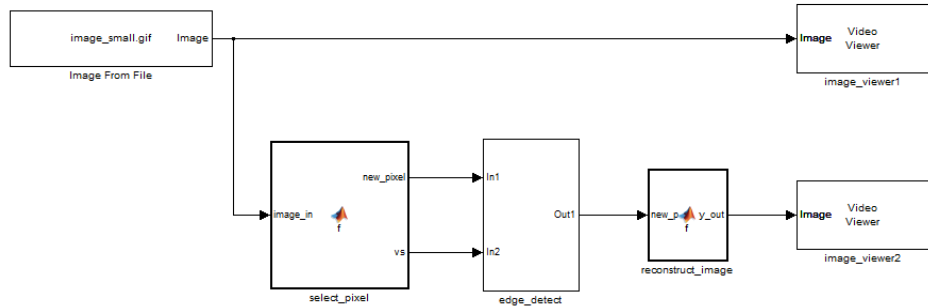
The default value of RAMMappingThreshold is 256. To change the threshold, use `hdlset_param`. For example, the following command changes the mapping threshold for the `sfir_fixed` model to 128 bits:

```
hdlset_param('sfir_fixed', 'RAMMappingThreshold', 128);
```

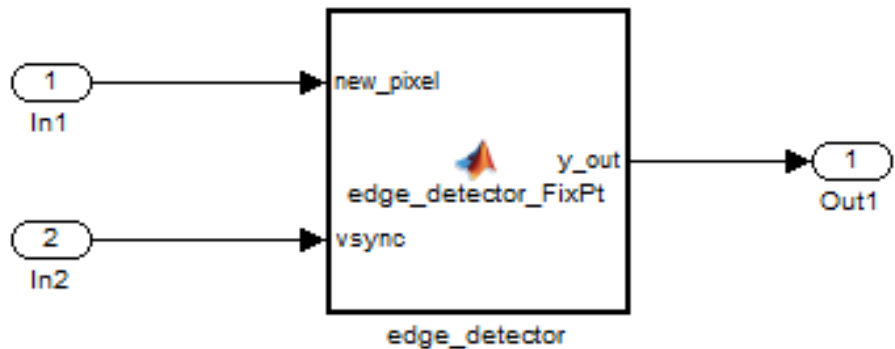
You can also change the RAM mapping threshold in the Configuration Parameters dialog box. For more information, see “HDL Code Generation Pane: Global Settings” on page 7-21.

## Example of Persistent Arrays Mapping to Block RAMs

Suppose that you use the following model to perform Sobel edge detection on a sample image:



The DUT is the `edge_detect` subsystem, which contains a MATLAB Function block named `edge_detector`:



The `edge_detector` block code includes the definition of several persistent arrays:

```
...
fm = hdlfimath;
% initialize line buffers and tap delay lines
persistent addr line_buffer1 line_buffer2 sobel_coeff1 sobel_coeff2
```

```

persistent tap_delay11 tap_delay12 tap_delay13 tap_delay21
persistent tap_delay22 tap_delay23
if isempty( line_buffer1 )
    addr = fi(1, 0, 8, 0, fm);
    line_buffer1 = fi(zeros( 1, 1024 ), 0, 8, 0, fm);
    line_buffer2 = fi(zeros( 1, 1024 ), 0, 8, 0, fm);
    tap_delay11 = fi(zeros( 1, 3 ), 0, 8, 0, fm);
    tap_delay12 = fi(zeros( 1, 3 ), 0, 8, 0, fm);
    tap_delay13 = fi(zeros( 1, 3 ), 0, 8, 0, fm);
    tap_delay21 = fi(zeros( 1, 3 ), 0, 8, 0, fm);
    tap_delay22 = fi(zeros( 1, 3 ), 0, 8, 0, fm);
    tap_delay23 = fi(zeros( 1, 3 ), 0, 8, 0, fm);
    %Coefficients for 3x3 Sobel Edge Detector
    sobel_coeff1 = fi([ 1, 2, 1; 0, 0, 0; -1, -2, -1 ], 1, 3, 0, fm);
    sobel_coeff2 = fi([ -1, 0, 1; -2, 0, 2; -1, 0, +1 ], 1, 3, 0, fm);
end
...

```

When MapPersistentVarsToRAM is off for the edge\_detector block, the Resource Utilization Report shows that the persistent arrays map to registers by default:

## Resource Utilization Report for ex\_edge\_detect\_fixpt

### Summary

Multipliers	36
Adders/Subtractors	60
<b>Registers</b>	<b>2067</b>
RAMs	0
Multiplexers	4

When `MapPersistentVarsToRAM` is on for the `edge_detector` block, the Resource Utilization Report shows a dramatic decrease in the number of registers. The two largest persistent arrays, `line_buffer1` and `line_buffer2`, map to RAMs:

## Resource Utilization Report for `ex_edge_detect_fixpt`

### Summary

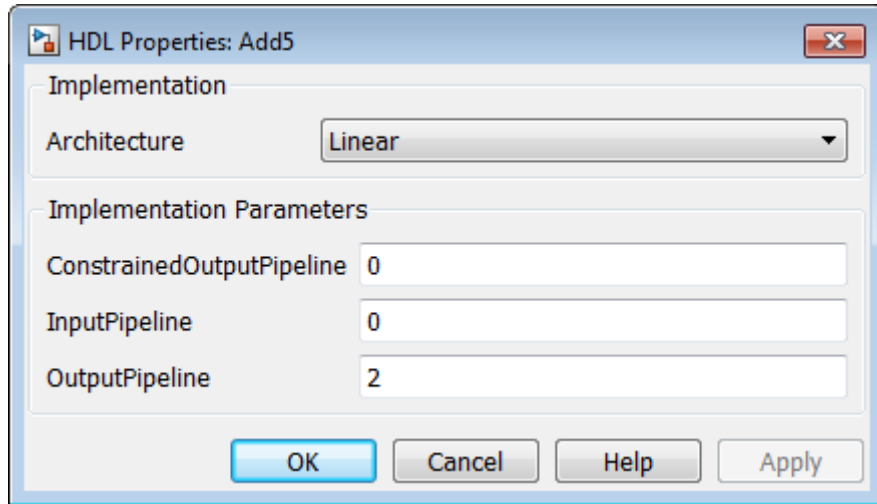
Multipliers	36
Adders/Subtractors	72
Registers	63
RAMs	2
Multiplexers	4

To learn about design patterns that enable efficient RAM mapping of persistent arrays in MATLAB Function blocks, see the `eml_hdl_design_patterns/RAMs` library. For more information, see “MATLAB Function Block Design Patterns for HDL” on page 17-23.

## OutputPipeline

`OutputPipeline` lets you specify a implementation with output pipelining for selected blocks. The parameter value specifies the number of output pipeline stages (pipeline depth) in the generated code.

The following figure shows the `OutputPipeline` parameter set to 2 in the HDL Properties dialog box for an Add block .



The following code specifies an output pipeline depth of two stages for each Sum block in the model:

```
sblocks = find_system(gcb, 'BlockType', 'Sum');
for ii=1:length(sblocks),hdlset_param(sblocks{ii},'OutputPipeline', 2), end;
```

When generating code for pipeline registers, the coder appends a postfix string to names of input or output pipeline registers. The default postfix string is `_pipe`. To customize the postfix string, use the **Pipeline postfix** option in the **Global Settings / General** pane in the **HDL Code** pane of the Model Configuration Parameters dialog box. Alternatively, you can pass the desired postfix string in the `makehdl` property `PipelinePostfix`. See `PipelinePostfix` for an example.

See also “Distributed Pipeline Insertion for MATLAB Function Blocks” on page 17-42.

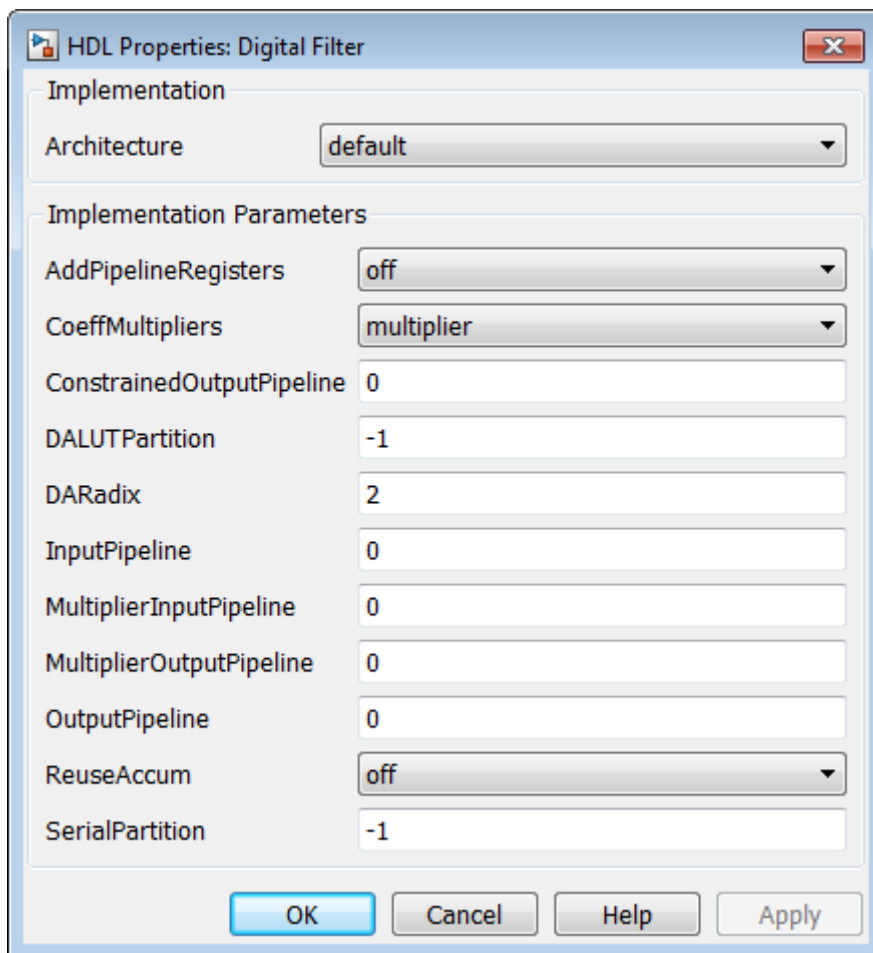
## Pipelining Implementation Parameters for Filter Blocks

The following implementation parameters for filter blocks provide block-specific pipelining support.



- `AddPipelineRegisters` (Default: off): Inserts a pipeline register between stages of computation in a filter.
- `MultiplierInputPipeline` (Default: 0): Generates a specified number of pipeline stages at multiplier inputs for FIR filter structures.
- `MultiplierOutputPipeline` (Default: 0): Generates a specified number of pipeline stages at multiplier outputs for FIR filter structures.

The following figure shows these parameters, set to their default values, in the HDL Block Properties dialog box for a Digital Filter block.



The following table summarizes the filter blocks that support one or more of these parameters:

<b>Filter Block</b>	<b>Supports AddPipelineRegisters</b>	<b>Supports MultiplierInputPipeline</b>	<b>Supports MultiplierOutputPipeline</b>
Digital Filter	Yes	Yes	Yes
Discrete FIR Filter	Yes	Yes	Yes

<b>Filter Block</b>	<b>Supports AddPipelineRegisters</b>	<b>Supports MultiplierInputPipeline</b>	<b>Supports MultiplierOutputPipeline</b>
FIR Decimation	Yes	Yes	Yes
FIR Interpolation	Yes	Yes	Yes
CIC Decimation	Yes	N/A	N/A
CIC Interpolation	Yes	N/A	N/A
Biquad Filter	Yes	N/A	N/A

### **AddPipelineRegisters Details**

The following table summarizes how enabling `AddPipelineRegisters` causes the different filter implementations to place pipeline registers, and the resultant latency.

<b>Filter Block</b>	<b>Pipeline Register Placement</b>	<b>Latency (clock cycles)</b>
Digital Filter (FIR, Asymmetric FIR, and Symmetric FIR filters)	A pipeline register is added between levels of a tree-based adder.	Where FL is the filter length: $\text{ceil}(\log_2(\text{FL}))$
Digital Filter (FIR Transposed)	A pipeline register is added after the products.	1
Digital Filter (IIR SOS)	Pipeline registers are added between the filter sections.	Where NS is number of sections: NS - 1

Filter Block	Pipeline Register Placement	Latency (clock cycles)
FIR Decimation	One pipeline register is added between levels of a tree-based adder, and one is added after the products.	Where NZ is the number of non-zero coefficients: $\text{ceil}(\log_2(NZ))$
FIR Interpolation	A pipeline register is added between levels of a tree-based adder.	Where PL is polyphase filter length: $\text{ceil}(\log_2(PL)) - 1$
CIC Decimation	A pipeline register is added between the comb stages of the differentiators .	Where NS is number of sections (at the input side): NS - 1
CIC Interpolation	A pipeline register is added between the comb stages of the differentiators.	Where NS is number of sections NS
Biquad Filter	Pipeline registers are added between the filter sections.	Where NS is number of sections: NS - 1

### Limitations

Take note of the following limitations when applying `AddPipelineRegisters`, `MultiplierInputPipeline`, and `MultiplierOutputPipeline`:

- For FIR Filters, the coder places pipeline stages in the adder tree structure. In cases where the filter datapath is not full precision, this causes numeric differences between the original model and the generated model. To avoid such discrepancies, the coder modifies the filter block parameters in the generated model to full precision.
- Pipeline stages inserted by `AddPipelineRegisters`, `MultiplierInputPipeline`, and `MultiplierOutputPipeline` introduce delays along the path in the model that contains the affected filter. However, equivalent delays are not introduced on other, parallel

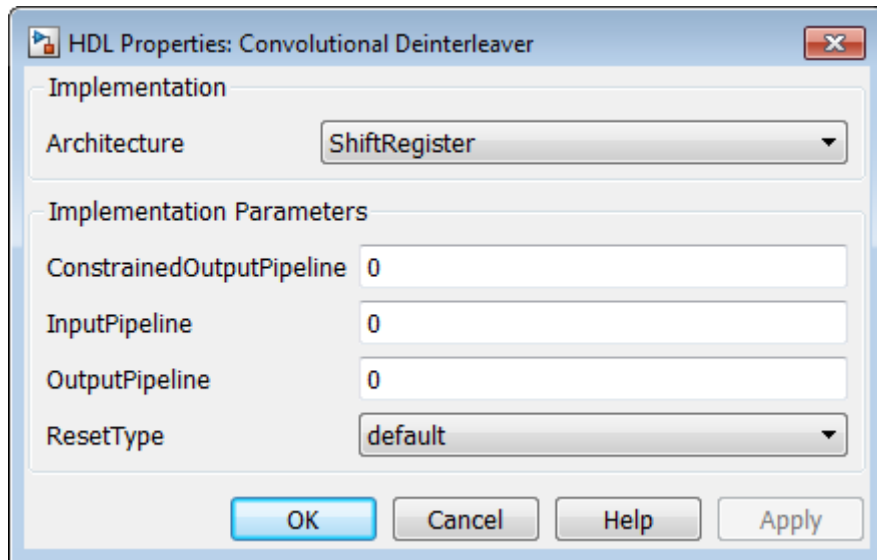
signal paths. To balance delays, use OutputPipeline on parallel data paths.

## RAM

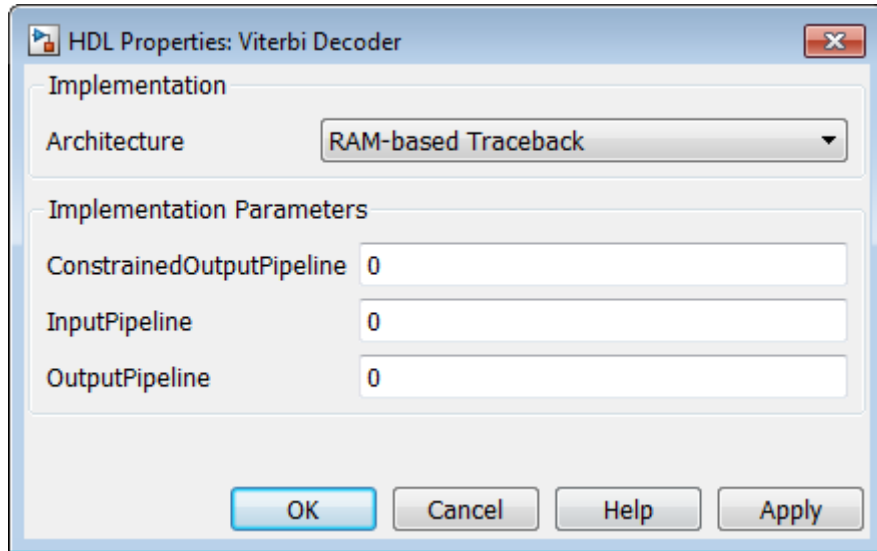
The following blocks support RAM based implementations as an alternative to shift register based implementations.

- commcnvintrlv2/Convolutional Deinterleaver
- commcnvintrlv2/Convolutional Interleaver
- commcnvcod2/Viterbi Decoder

The following figure shows the RAM and shift register options in the HDL Properties dialog box for a Convolutional Deinterleaver.



The following figure shows the RAM-based traceback option in the HDL Properties dialog box for a Viterbi Decoder.



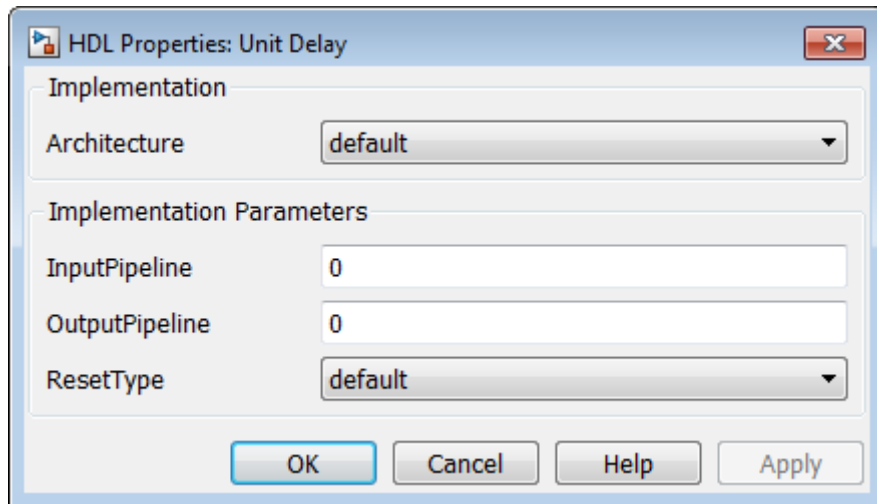
## ResetType

The ResetType implementation parameter lets you suppress generation of reset logic for the following block types:

- commcnvtrlv2/Convolutional Deinterleaver
- commcnvtrlv2/Convolutional Interleaver
- commcnvtrlv2/General Multiplexed Deinterleaver
- commcnvtrlv2/General Multiplexed Interleaver
- dspsigops/Delay
- simulink/Additional Math & Discrete/Additional Discrete/Unit Delay Enabled
- simulink/Commonly Used Blocks/Unit Delay
- simulink/Discrete/Delay
- simulink/Discrete/Memory
- simulink/Discrete/Tapped Delay

- simulink/User-Defined Functions/MATLAB Function
- sflib/Chart
- sflib/Truth Table

The following figure shows the reset type option in the HDL Properties dialog box for a Unit Delay block.



When you specify `ResetType` as 'default', the coder follows the Global Settings/Advanced **Reset type** option for the specified blocks.

When you specify `ResetType` as 'none' for a selection of one or more blocks, the coder overrides the Global Settings/Advanced **Reset type** option for the specified blocks only. Reset signals and synchronous or asynchronous reset logic (as specified by **Reset type**) is still generated as required for other blocks.

Note that when you set `ResetType` to 'none', reset is not applied to generated registers. Mismatches between Simulink and the generated code occur for some number of samples during the initial phase, when registers are not fully loaded. To avoid spurious test bench errors, determine the number of samples required to fully load the registers. Then, set the **Ignore output data checking (number of samples)** option accordingly. (You can use

the `IgnoreDataChecking` property for this purpose, if you are using the command-line interface.) See also `IgnoreDataChecking`.

The following code specifies suppression of reset logic for a specific unit delay block within a subsystem.

```
hdlset_param('rst_exam/ADut/UnitDelay1','ResetType','none');
```

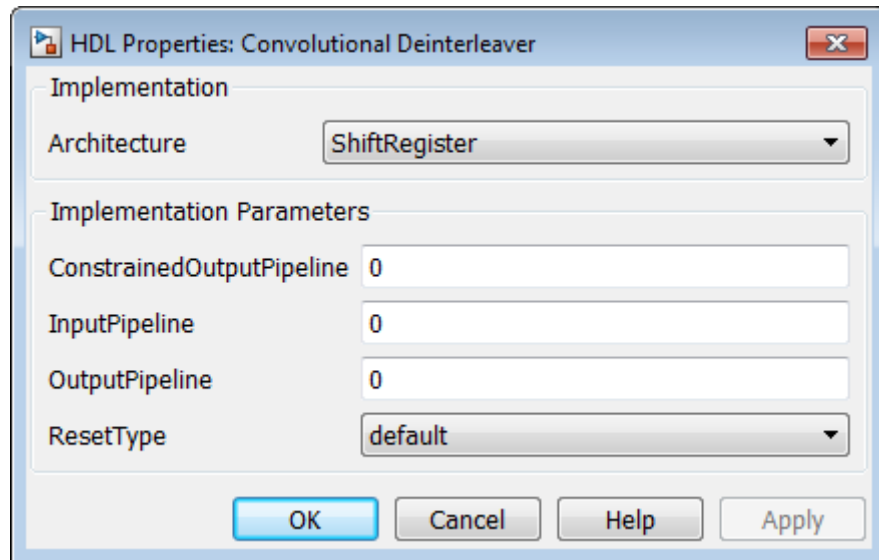
### ShiftRegister

The following blocks support shift register based implementations. (See “Convolutional Interleaver and Deinterleaver Block Requirements and Restrictions” on page 9-33.)

- `commcnvintrlv2/Convolutional Deinterleaver`
- `commcnvintrlv2/Convolutional Interleaver`
- `commcnvintrlv2/General Multiplexed Deinterleaver`
- `commcnvintrlv2/General Multiplexed Interleaver`

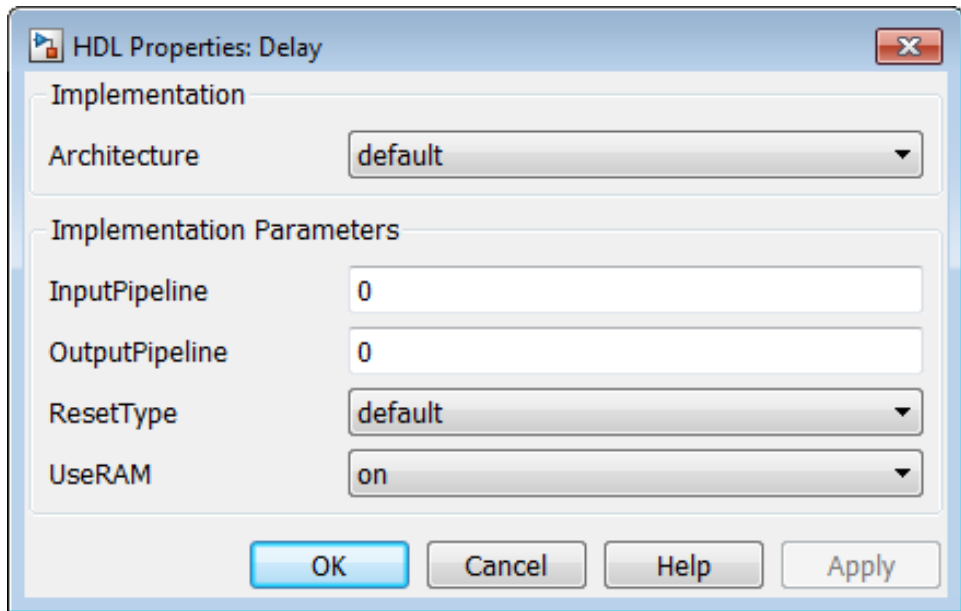
The following figure shows the shift register option in the HDL Properties dialog box for a Convolutional Deinterleaver .





## UseRAM

The UseRAM implementation parameter enables using RAM-based mapping for a block instead of mapping to a shift register. This implementation parameter is available for the Delay block in the Simulink Discrete library and the Delay block in the DSP System Toolbox Signal Operations library.



### Mapping of a Single Delay to a RAM

UseRAM Setting	Mapping Behavior
off	The delay maps to a shift register in the generated HDL code, except in one case. For details, see “Effects of Streaming and Distributed Pipelining” on page 9-100.
on	The delay maps to a dual-port RAM block when all of the following conditions are true: <ul style="list-style-type: none"> <li>• Initial value of the delay is zero.</li> <li>• Delay length &gt; 4.</li> </ul>

UseRAM Setting	Mapping Behavior
	<ul style="list-style-type: none"> <li>• Delay has one of the following set of numeric and data type attributes: <ul style="list-style-type: none"> <li>▪ (a) Real scalar with a non-floating-point data type (such as signed integer, unsigned integer, fixed point, or Boolean)</li> <li>▪ (b) Complex scalar with real and imaginary parts that use non-floating-point data type</li> <li>▪ (c) Vector where each element is either (a) or (b)</li> </ul> </li> <li>• RAMSize is greater than or equal to the RAMMappingThreshold value. RAMSize is the product DelayLength * WordLength * ComplexLength. <ul style="list-style-type: none"> <li>▪ DelayLength is the number of delays that the Delay block specifies.</li> <li>▪ WordLength is the number of bits that represent the data type of the delay.</li> <li>▪ ComplexLength is 2 for complex signals; 1 otherwise.</li> </ul> </li> </ul> <p>If any condition is false, the delay maps to a shift register in the HDL code unless it merges with other delays to map to a single RAM. For more information, see “Mapping of Multiple Delays to a RAM” on page 9-98.</p>

The default value of RAMMappingThreshold is 256. To change the threshold, use `hdlset_param`. For example, the following command changes the mapping threshold for the `sfir_fixed` model to 128 bits:

```
hdlset_param('sfir_fixed', 'RAMMappingThreshold', 128);
```

You can also change the RAM mapping threshold in the Configuration Parameters dialog box. For more information, see “HDL Code Generation Pane: Global Settings” on page 7-21.

## Mapping of Multiple Delays to a RAM

The coder can also merge several delays of equal length into one delay and then map the merged delay to a single RAM. This optimization provides the following benefits:

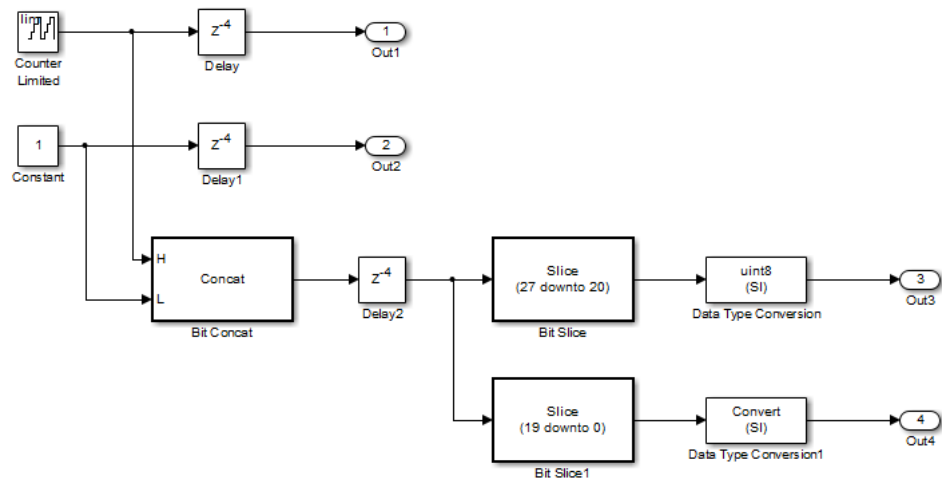
- Increased occupancy on a single RAM
- Sharing of address generation logic, which minimizes duplication of identical HDL code
- Mapping of delays to a RAM when the *individual* delays do not satisfy the threshold

The following rules control whether or not multiple delays can merge into one delay:

- The delays must:
  - Be at the same level of the subsystem hierarchy.
  - Use the same compiled sample time.
  - Have UseRAM set to on, or be generated by streaming or resource sharing.
  - Have the same ResetType setting, which cannot be none.
- The total word length of the merged delay cannot exceed 128 bits.
- The RAMSize of the merged delay is greater than or equal to the RAMMappingThreshold value. RAMSize is the product  $\text{DelayLength} * \text{WordLength} * \text{VectorLength} * \text{ComplexLength}$ .
  - DelayLength is the total number of delays.
  - WordLength is the number of bits that represent the data type of the merged delay.
  - VectorLength is the number of elements in a vector delay. VectorLength is 1 for a scalar delay.
  - ComplexLength is 2 for complex delays; 1 otherwise.

## Example of Multiple Delays Mapping to a RAM

RAMMappingThreshold for the following model is 100 bits.



The Delay and Delay1 blocks merge and map to a dual-port RAM in the generated HDL code by satisfying the following conditions:

- Both delay blocks:
  - Are at the same level of the hierarchy.
  - Use the same compiled sample time.
  - Have `UserRAM` set to on in the HDL block properties dialog box.
  - Have the same `ResetType` setting of default.
- The total word length of the merged delay is 28 bits, which is below the 128-bit limit.
- The `RAMSize` of the merged delay is 112 bits (4 delays \* 28-bit word length), which is greater than the mapping threshold of 100 bits.

When you generate HDL code for this model, the coder generates additional files to specify RAM mapping. The coder stores these files in the same source location as other generated HDL files, for example, the `hdlsrc` folder.

### Effects of Streaming and Distributed Pipelining

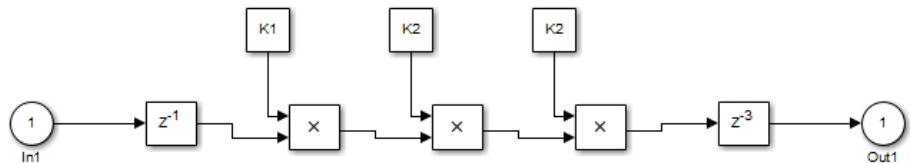
When UseRAM is off for a Delay block, the coder maps the delay to a shift register by default. However, the coder changes the UseRAM setting to on and tries to map the delay to a RAM under the following conditions:

- Streaming is *enabled* for the subsystem with the Delay block.
- Distributed pipelining is *disabled* for the subsystem with the Delay block.

Suppose that distributed pipelining is *enabled* for the subsystem with the Delay block.

- When UseRAM is off, the Delay block participates in retiming.
- When UseRAM is on, the Delay block does not participate in retiming. The coder does not break up a delay marked for RAM mapping.

Consider a subsystem with two Delay blocks, three Constant blocks, and three Product blocks:



When UseRAM is on for the Delay block on the right, that delay does not participate in retiming.

The following summary describes whether or not the coder tries to map a delay to a RAM instead of a shift register.

UseRAM Setting for the Delay Block	Optimizations Enabled for Subsystem with Delay Block		
	Distributed Pipelining Only	Streaming Only	Both Distributed Pipelining and Streaming
On	Yes	Yes	Yes
Off	No	Yes, because mapping to a RAM instead of a shift register can provide an area-efficient design.	No

## Speed vs. Area Optimizations for FIR Filter Implementations

### Overview of Speed vs. Area Optimizations

The coder provides options that extend your control over speed vs. area tradeoffs in the realization of FIR filter designs. To achieve the desired tradeoff, you can either specify a *fully parallel* architecture for generated HDL filter code, or choose one of several *serial* architectures. “Parallel and Serial Architectures” on page 9-102 describes the supported architectures.

The following blocks support these architecture options:

- dsparch4/Digital Filter
- dspmlti4/FIR Decimation
- dspmlti4/FIR.Interpolation
- simulink/Discrete/Discrete FIR Filter

You can specify the full range of parallel and serial architecture options using implementation parameters, as described in “Implementation Parameters for Specifying Speed vs. Area Tradeoffs” on page 9-103

## Parallel and Serial Architectures

**Fully Parallel Architecture.** This is the default option. A fully parallel architecture uses a dedicated multiplier and adder for each filter tap; the taps execute in parallel. A fully parallel architecture is optimal for speed. However, it requires more multipliers and adders than a serial architecture, and therefore consumes more chip area.

**Serial Architectures.** Serial architectures reuse hardware resources in time, saving chip area. The coder provides a range of serial architecture options, summarized below. These architectures have a latency of one clock period (see “Latency in Serial Architectures” on page 9-103).

The available serial architecture options are

- *Fully serial:* A fully serial architecture conserves area by reusing multiplier and adder resources sequentially. For example, a four-tap filter design would use a single multiplier and adder, executing a multiply/accumulate operation once for each tap. The multiply/accumulate section of the design runs at four times the filter’s input/output sample rate. This saves area at the cost of some speed loss and higher power consumption.

In a fully serial architecture, the system clock runs at a much higher rate than the sample rate of the filter. Thus, for a given filter design, the maximum speed achievable by a fully serial architecture will be less than that of a parallel architecture.

- *Partly serial:* Partly serial architectures cover the full range of speed vs. area tradeoffs that lie between fully parallel and fully serial architectures.

In a partly serial architecture, the filter taps are grouped into a number of serial *partitions*. The taps within each partition execute serially, but the partitions execute in parallel with respect to one another. The outputs of the partitions are summed at the final output.

When you select a partly serial architecture, you specify the number of partitions and the length (number of taps) of each partition. For example,



you could specify a four-tap filter with two partitions, each having two taps. The system clock would run at twice the filter's sample rate.

- *Cascade-serial*: A cascade-serial architecture closely resembles a partly serial architecture. As in a partly serial architecture, the filter taps are grouped into a number of serial partitions that execute in parallel with respect to one another. However, the accumulated output of each partition is cascaded to the accumulator of the previous partition. The output of all partitions is therefore computed at the accumulator of the first partition. This technique is termed *accumulator reuse*. A final adder is not required, which saves area.

The cascade-serial architecture requires an extra cycle of the system clock to complete the final summation to the output. Therefore, the frequency of the system clock must be increased slightly with respect to the clock used in a non-cascade partly serial architecture.

To generate a cascade-serial architecture, you specify a partly serial architecture with accumulator reuse enabled (see “Implementation Parameters for Specifying Speed vs. Area Tradeoffs” on page 9-103. If you do not specify the serial partitions, the coder automatically selects an optimal partitioning.

**Latency in Serial Architectures.** Serialization of a filter increases the total latency of the design by one clock cycle. The serial architectures use an accumulator (an adder with a register) to add the products sequentially. An additional final register is used to store the summed result of all the serial partitions, requiring an extra clock cycle for the operation. To handle latency, the coder inserts a Delay block into the generated model after the filter block.

## Implementation Parameters for Specifying Speed vs. Area Tradeoffs

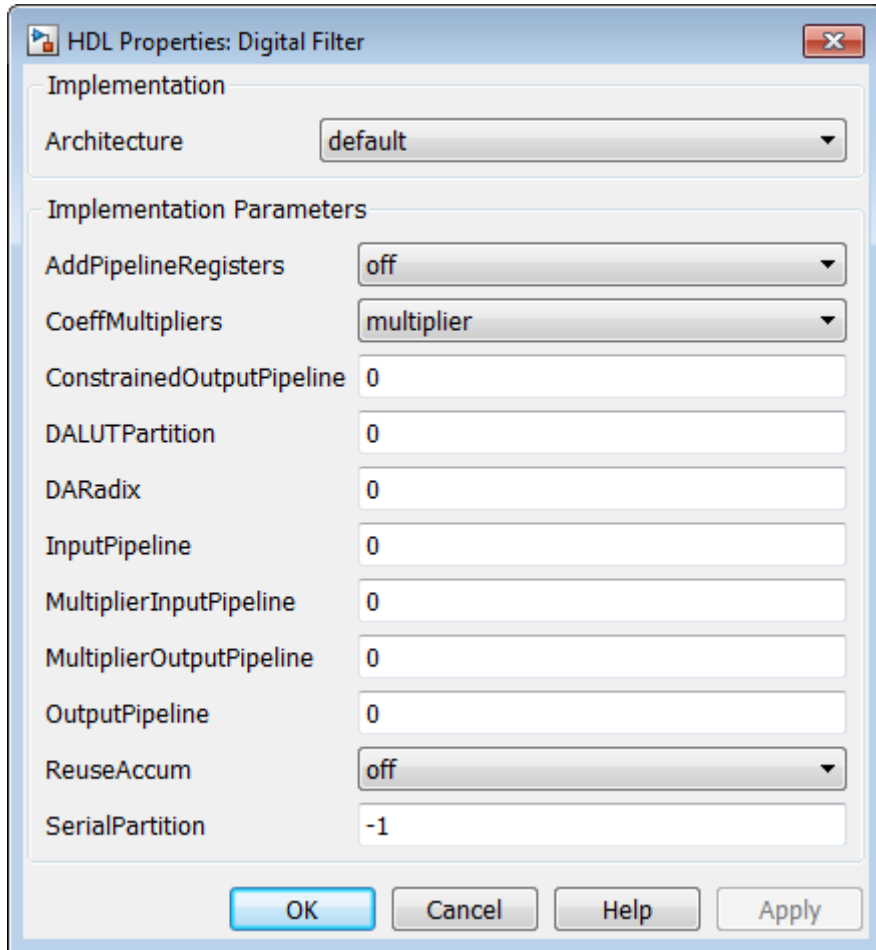
By default, `makehdl` generates filter code using a fully parallel architecture. If you want to generate FIR filter code with a fully parallel architecture, you do not need to specify this explicitly.

Two implementation parameters specify serial architecture options when generating code via `makehdl`:

- `'SerialPartition'`: This parameter specifies the serial partitioning of the filter.

- 'ReuseAccum': This parameter enables or disables accumulator reuse.

The following figure shows these parameters (at default values) on the HDL Properties dialog box for a Digital Filter block.

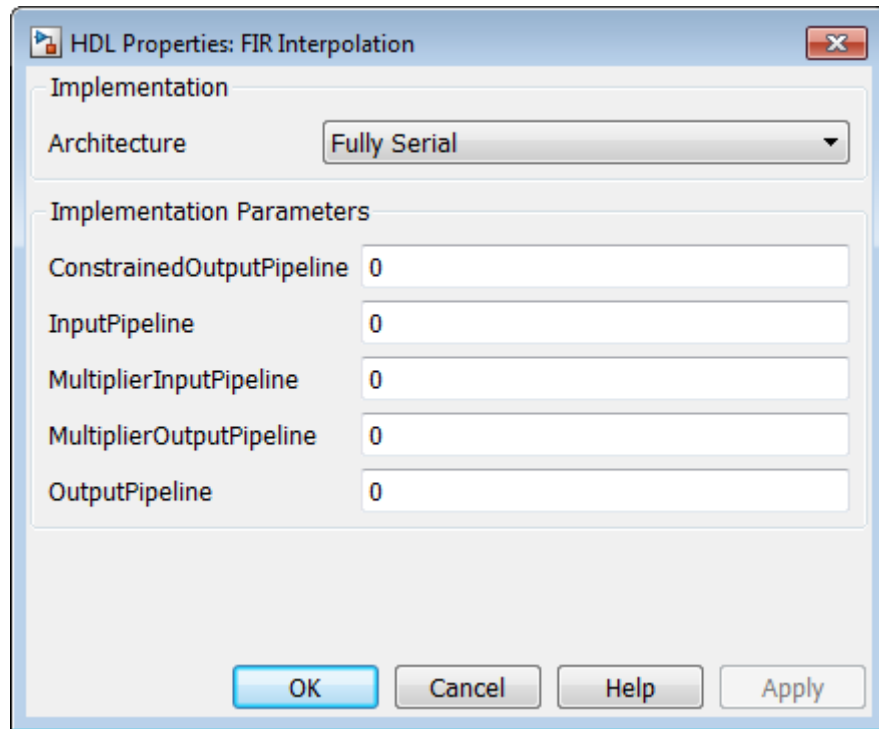


The table below summarizes how to set these parameters to generate the desired architecture.

<b>To Generate This Architecture...</b>	<b>Set SerialPartition to...</b>	<b>Set ReuseAccum to...</b>
Fully parallel	Omit this property	Omit this property
Fully serial	N, where N is the length of the filter	Not specified, or 'off'
Partly serial	<p>[p1 p2 p3 . . . pN] : a vector of integers having N elements, where N is the number of serial partitions. Each element of the vector specifies the length of the corresponding partition. The sum of the vector elements must be equal to the length of the filter. When you define the partitioning for a partly serial architecture, consider the following:</p> <ul style="list-style-type: none"> <li>• The filter length should be divided as uniformly as possible into a vector of length equal to the number of multipliers intended. For example, if your design requires a filter of length 9 with 2 multipliers, the recommended partition is [5 4]. If your design requires 3 multipliers, the recommended partition is [3 3 3] rather than some less uniform division such as [1 4 4] or [3 4 2].</li> <li>• If your design is constrained by the need to compute each output value (corresponding to each input value) in an exact number N of clock cycles, use N as the largest partition size and partition the other elements as uniformly as possible. For example, if the filter length is 9 and your design requires exactly 4 cycles to compute the output, define the partition as [4 3 2]. This partition executes in 4 clock cycles, at the cost of 3 multipliers.</li> </ul>	'off'

To Generate This Architecture...	Set SerialPartition to...	Set ReuseAccum to...
Cascade-serial with explicitly specified partitioning	[p1 p2 p3...pN]: a vector of integers having N elements, where N is the number of serial partitions. Each element of the vector specifies the length of the corresponding partition. The sum of the vector elements must be equal to the length of the filter. The values of the vector elements must be in descending order, except that the last two element must be equal. For example, for a filter of length 9, partitions such as [5 4] or [4 3 2] would be legal, but the partitions [3 3 3] or [3 2 4] would raise an error at code generation time.	'on'
Cascade-serial with automatically optimized partitioning	Omit this property	'on'

**FIL Interpolation Block Exception.** The SerialPartition property is set automatically for you on the FIL Interpolation Block when you select Fully Serial architecture.



**Filter Block Settings and Limitations.** When you specify `SerialPartition` and `ReuseAccum` for a Digital Filter block, observe the following constraints.

- If you specify **Dialog parameters** as the `Coefficient` source:
  - Set **Transfer function type** to FIR (all zeros).
  - Select **Filter structure** as one of: Direct form,, Direct form symmetric, or Direct form asymmetric.
- If you specify **Discrete-time filter object** as the `Coefficient` source, the filter object must be one of the following:
  - `dfilt.dffir`
  - `dfilt.dfsymfir`
  - `dfilt.dfasymfir`

When you specify `SerialPartition` and `ReuseAccum` for a Discrete FIR Filter block, select **Filter structure** as one of the following:

- Direct form
- Direct form symmetric
- Direct form asymmetric

Observe the following limitations for FIR Decimation filters:

- The coder supports `SerialPartition` only for the FIR Direct Form structure.
- Accumulator reuse is not supported.

The coder supports serial partitioning for filter blocks only if all settings of the filter block are in full precision.

**Use Full Precision Filter Settings.** The coder supports serial partitioning for filter blocks only if all settings of the filter block are in full precision.

### Interface Generation Parameters

Some block implementation parameters let you customize features of an interface generated for the following block types:

- `simulink/Ports & Subsystems/Model`
- `built-in/Subsystem`
- `lfilelib/HDL Cosimulation`
- `modelsimlib/HDL Cosimulation`

For example, you can specify generation of a black box interface for a subsystem, and pass parameters that specify the generation and naming of clock, reset, and other ports in HDL code. For more information about interface generation parameters, see “Customize the Generated Interface” on page 15-54.

## Blocks That Support Complex Data

You can use complex signals in the test bench without restriction.

In the device under test (DUT) selected for HDL code generation, support for complex signals is limited to a subset of the blocks that the coder supports. These blocks appear in the following table. Some restrictions apply for some of these blocks.

---

**Note** All blocks listed support the `InputPipeline` and `OutputPipeline` implementation parameters.

---

Complex data expands into real and imaginary signals. The naming conventions for these derived signals are:

- Real components have the same name as the original complex signal, suffixed with the default string `'_re'` (for example, `x_re`). To specify a different suffix, set the **Complex real part postfix** option (or the corresponding `ComplexRealPostfix` CLI property).
- Imaginary components have the same name as the original complex signal, suffixed with the string `'_im'` (for example, `x_im`). To specify a different suffix, set the **Complex imaginary part postfix** option (or the corresponding `ComplexImagPostfix` CLI property).

Simulink Block	Restrictions
dspadpt3/LMS Filter	
dspindex/Variable Selector	
dsparch4/Biquad Filter	See “Complex Coefficients and Data Support for the Digital Filter and Biquad Filter Blocks” on page 9-113
dsparch4/Digital Filter	See “Complex Coefficients and Data Support for the Digital Filter and Biquad Filter Blocks” on page 9-113
dspindex/Multiport Selector	

<b>Simulink Block</b>	<b>Restrictions</b>
dspsigattribs/Convert 1-D to 2-D	
dspsigattribs/Frame Conversion	
dspsigops/Delay	
dspsigops/Downsample	
dspsigops/NCO	
dspsigops/Upsample	
dspsrcs4/DSP Constant	
dspsrcs4/Sine Wave	
hdl demolib/Dual Port RAM	
hdl demolib/Simple Dual Port RAM	
hdl demolib/Single Port RAM	
hdl demolib/HDL FFT	
hdl demolib/HDL Streaming FFT	
sflib/Chart	
simulink/Additional Math & Discrete/Additional Discrete/Unit Delay Enabled	
simulink/Commonly Used Blocks/Constant	
simulink/Commonly Used Blocks/Data Type Conversion	
simulink/Commonly Used Blocks/Demux	
simulink/Commonly Used Blocks/Gain	
simulink/Commonly Used Blocks/Ground	
simulink/Commonly Used Blocks/Product	



<b>Simulink Block</b>	<b>Restrictions</b>
simulink/Commonly Used Blocks/Sum	
simulink/Commonly Used Blocks/Mux	
simulink/Commonly Used Blocks/Relational Operator	~= and == operators only
simulink/Commonly Used Blocks/Switch	
simulink/Commonly Used Blocks/Unit Delay	
simulink/Discrete/Delay	
simulink/Discrete/Memory	
simulink/Discrete/Zero-Order Hold	
simulink/Discrete/Tapped Delay	
simulink/Logic and Bit Operations/Compare To Constant	
simulink/Logic and Bit Operations/Compare To Zero	
simulink/Logic and Bit Operations/Shift Arithmetic	
simulink/Lookup Tables/1-D Lookup Table	
simulink/Math Operations/Add	
simulink/Math Operations/Assignment	
simulink/Math Operations/Complex to Real-Imag	
simulink/Math Operations/Unary Minus	

<b>Simulink Block</b>	<b>Restrictions</b>
simulink/Math Operations/Math Function	The conj, hermitian, and transpose functions support complex data.
simulink/Math Operations/Matrix Concatenate	
simulink/Math Operations/Product of Elements	Only the default (linear) implementation supports complex data.  Complex division is not supported.
simulink/Math Operations/Real-Imag to Complex	
simulink/Math Operations/Reshape	
simulink/Math Operations/Subtract	Only the default (linear) implementation supports complex data.
simulink/Math Operations/Sum of Elements	Only the default (linear) implementation supports complex data.
simulink/Math Operations/Vector Concatenate	
simulink/Signal Attributes/Rate Transition	
simulink/Signal Attributes/Signal Conversion	
simulink/Signal Attributes/Signal Specification	
simulink/Signal Routing/Index Vector	
simulink/Signal Routing/Multiport Switch	

<b>Simulink Block</b>	<b>Restrictions</b>
simulink/Signal Routing/Selector	
simulink/User-Defined Functions/MATLAB Function	See also “Complex Data Type Support” on page 17-50.

## Complex Coefficients and Data Support for the Digital Filter and Biquad Filter Blocks

The coder supports use of complex coefficients and complex input signals for all filter structures of the Digital Filter and Biquad Filter blocks, except decimators and interpolators. In many cases, you can use complex data and complex coefficients in combination. The following table shows the filter structures that support complex data and/or coefficients, and the permitted combinations.

<b>Filter Structure</b>	<b>Complex Data</b>	<b>Complex Coefficients</b>	<b>Complex Data and Coefficients</b>
dfilt.dffir	Y	Y	Y
dfilt.dfsymfir	Y	Y	Y
dfilt.dfasymfir	Y	Y	Y
dfilt.dffirt	Y	Y	Y
dfilt.scalar	Y	Y	Y
dfilt.delay	Y	N/A	N/A
mfilt.cicdecim	Y	N/A	N/A
mfilt.cicinterp	Y	N/A	N/A
mfilt.firdecim	Y	Y	N
mfilt.firinterp	Y	Y	N
dfilt.df1sos	Y	Y	Y
dfilt.df1tsos	Y	Y	Y
dfilt.df2sos	Y	Y	Y
dfilt.df2tsos	Y	Y	Y

## Blocks That Support Buses

In this section...
“Supported Bus Blocks” on page 9-114
“Settings and Requirements” on page 9-114
“Limitations” on page 9-117
“See Also” on page 9-118

### Supported Bus Blocks

The following bus-capable blocks support HDL code generation:

- Bus Creator
- Bus Selector

If you want to use buses in your design *and* you want to generate HDL code, then you must use these blocks for the buses in your design. No other bus-capable blocks support HDL code generation.

### Settings and Requirements

Although the Bus Creator and Bus Selector blocks do not have new GUI elements for code generation, there are some conditions you must meet for HDL code generation.

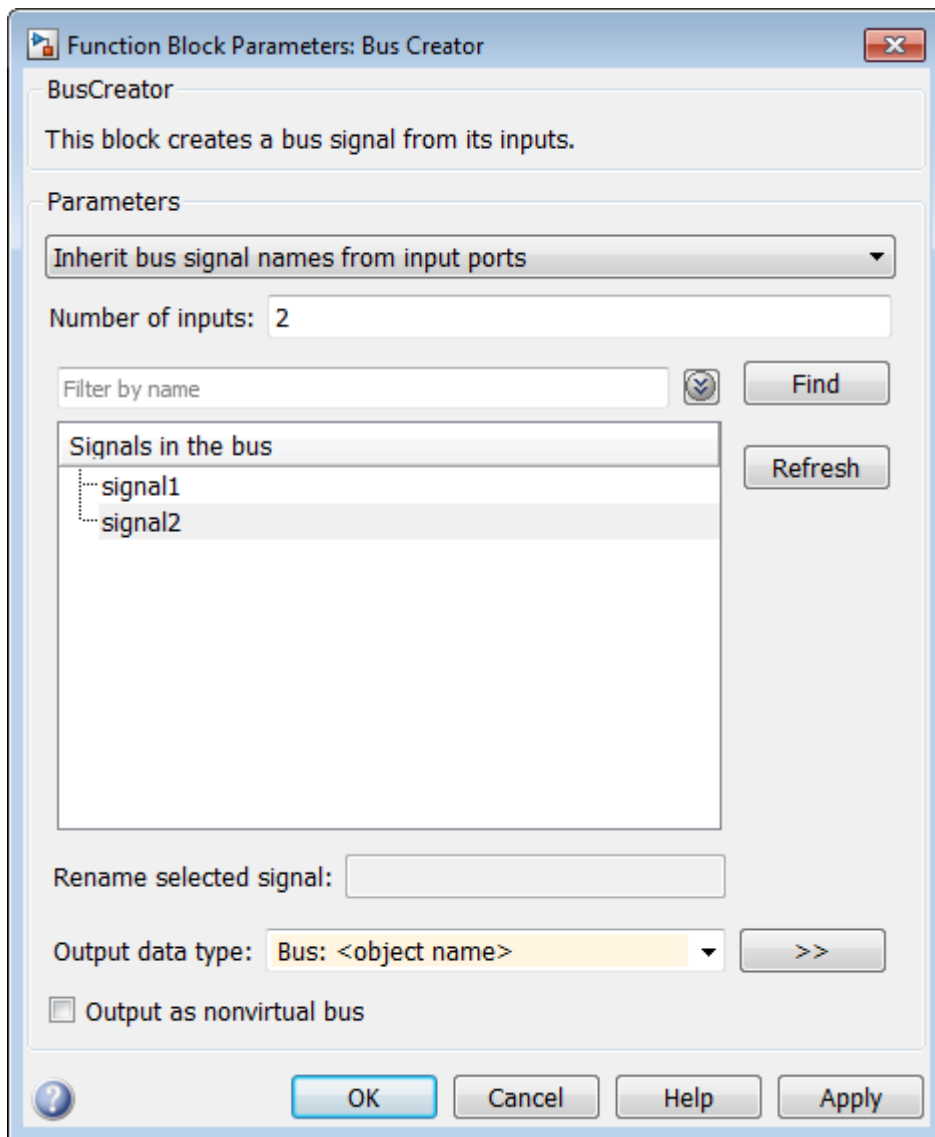
#### Requirements

Make sure the buses at the level you want to generate code from are connected to either a Bus Creator or Bus Selector block.

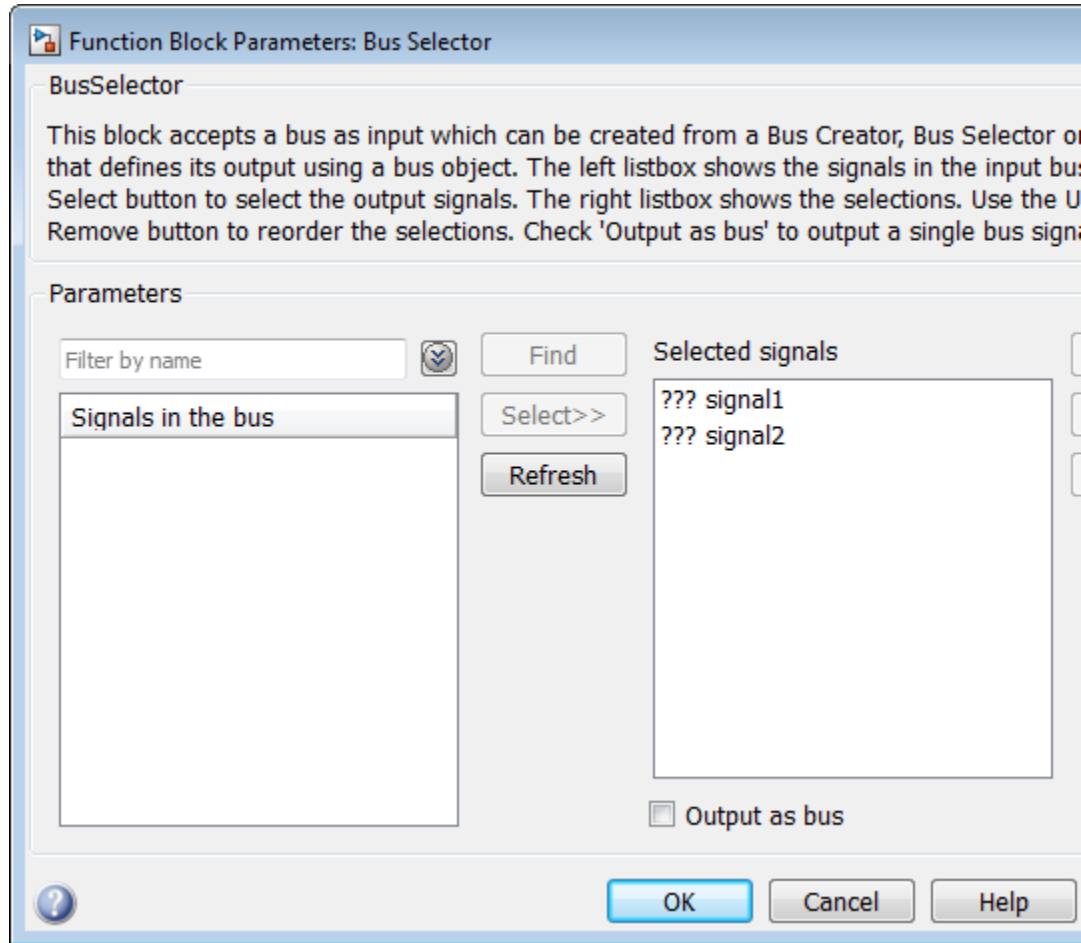
#### Settings

- Perform *one* of the following tasks to enable HDL code generation:
  - Run function `hdlsetup` at the MATLAB command prompt.

- In the Configuration Parameters dialog, select the Diagnostics page. On the Connectivity pane, set **Mux blocks used to create bus signals** to *error*.
- In the Bus Creator dialog:
  - Make sure **Output as nonvirtual bus** is *not* checked.
  - Make sure Bus Creator output is a BusObject.



- In the Bus Selector dialog, make sure **Output as a bus** is *not* checked.



## Limitations

HDL code generation for buses does not support:

- Buses that do not have BusObject data type
- Non-virtual bus
- Output as a bus (for Bus Selector)

- Other bus-capable blocks

### **See Also**

- Bus Creator
- Bus Selector



# Lookup Table Block Support

The coder supports the following lookup table (LUT) blocks:

- simulink/Lookup Tables/n-D Lookup Table
- simulink/Lookup Tables/Prelookup
- simulink/Lookup Tables/Direct Lookup Table (n-D)
- simulink/Lookup Tables/1-D Lookup Table
- simulink/Lookup Tables/2-D Lookup Table

When you configure a lookup table block for HDL code generation, observe the requirements and limitations described in the following sections.

## n-D Lookup Table

### Required Block Settings

- **Number of table dimensions:** The coder supports a maximum dimension of 2.
- **Index search method:** Select Evenly spaced points.
- **Extrapolation method:** The coder supports only Clip. The coder does not support extrapolation beyond the table bounds.
- **Interpolation method:** The coder supports only Flat or Linear.
- **Diagnostic for out-of-range input:** Select Error. If you select other options, the coder displays a warning.
- **Use last table value for inputs at or above last breakpoint:** Select this check box.
- **Require all inputs to have the same data type:** Select this check box.
- **Fraction:** Select Inherit: Inherit via internal rule.
- **Integer rounding mode:** Select Zero, Floor, or Simplest.

### Avoid Generation of Divide Operator

The coder gives a warning if it encounters conditions under which a division operation is required to match the model's simulation behavior. The conditions described in this section will cause the n-D Lookup Table block to emit a divide operator. When you use the n-D Lookup Table block for HDL code generation, you should avoid the following conditions:

- If the block is configured to use interpolation, a division operator will be required. To avoid this, set **Interpolation method** : to Flat.
- The second way depends on the table spacing. HDL code generation requires the block to use the "Evenly Spaced Points" algorithm. The block mapping from the input data type to the zero-based table index in general requires a division. When the breakpoint spacing is an exact power of 2, this divide is implemented as a shift instead of as a divide. To adjust the breakpoint spacing, you can adjust the number of breakpoints in the table and/or the difference between the left and right bounds of the breakpoint range.

### Table Data Typing and Sizing

- It is good practice to structure your table such that the spacing between breakpoints is a power of two. The coder issues a warning if the breakpoint spacing does not meet this condition. When the breakpoint spacing is a power of two, you can replace division operations in the prelookup step with right-shift operations.
- Table data must resolve to a nonfloating-point data type.
- All ports on the block require scalar values.

### Prelookup

#### Required Block Settings

- **Index search method**: Select Evenly spaced points.
- **Extrapolation method**: Select Clip.
- **Diagnostic for out-of-range input**: Select Error. If you select other options, the coder displays a warning.

- **Use last breakpoint for input at or above upper limit:** Select this check box.
- **Breakpoint data type:** Select Inherit: Same as input.
- **Integer rounding mode:** Select Zero, Floor, or Simplest.

### Table Data Typing and Sizing

- It is good practice to structure your table such that the spacing between breakpoints is a power of two. The coder issues a warning if the breakpoint spacing does not meet this condition. When the breakpoint spacing is a power of two, you can replace division operations in the prelookup step with right-shift operations.
- All ports on the block require scalar values.
- The coder permits floating-point data for breakpoints.

## Direct Lookup Table (n-D)

### Required Block Settings

- **Number of table dimensions:** The coder supports a maximum dimension of 2.
- **Inputs select this object from table:** Select Element.
- **Make table an input:** Clear this check box.
- **Diagnostic for out-of-range input:** Select Error. If you select other options, the coder displays a warning.

### Table Data Typing and Sizing

- It is good practice to size each dimension in the table to be a power of two. The coder issues a warning if the length of a dimension (*except* the innermost dimension) is not a power of two. By following this practice, you can avoid multiplications during table indexing operations and realize a more efficient table in hardware.

- Table data must resolve to a nonfloating-point data type. The coder examines the output port to verify that its data type meets this requirement.
- All ports on the block require scalar values.

### **1-D Lookup Table**

The 1-D Lookup Table block is subject to the same limitations as the n-D Lookup Table block. See “n-D Lookup Table” on page 9-119 for detailed information.

### **2-D Lookup Table**

The 2-D Lookup Table block is subject to the same limitations as the n-D Lookup Table block. See “n-D Lookup Table” on page 9-119 for detailed information.

# Generating HDL Code for Multirate Models

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- “Code Generation from Multirate Models” on page 10-2
- “Configure Multirate Models for HDL Code Generation” on page 10-3
- “Code Generation from a Multirate DUT” on page 10-6
- “Generate a Global Oversampling Clock” on page 10-9
- “Generate Multicycle Path Information Files” on page 10-16
- “HDL Properties for Controlling Multirate Code Generation” on page 10-27

## Code Generation from Multirate Models

The coder supports HDL code generation for single-clock and multiple clock multirate models. Your model can include blocks running at multiple sample rates:

- Within the device under test (DUT).
- In the test bench driving the DUT. In this case, the DUT inherits multiple sample rates from its inputs or outputs.
- In both the test bench and the DUT.

A *timing controller* entity generates the required rates from a single master clock using one or more counters, creating multiple clock enables. The master clock rate is the fastest rate in the model in single clock mode. In multiple clock mode, it can be any clock in the DUT. The outputs of the timing controller are clock enable signals running at rates an integer multiple slower than the timing controller's master clock

Each timing controller entity definition is written to a separate code file. The timing controller file and entity names derive from the name of the subsystem that is selected for code generation (the DUT). To form the timing controller name, the coder appends the value of the `TimingControllerPostfix` property to the DUT name.

When using single clock mode, HDL code generated from multirate models employs a single master clock that corresponds to the base rate of the DUT. When using multiple clock mode, HDL code generated from multirate models employs one clock input for each rate in the DUT. The number of timing controllers generated in multiple clock mode depends on the design in the DUT.

In general, generating HDL code for a multirate model does not differ greatly from generating HDL code for a single-rate model. However, there are a few requirements and restrictions on the configuration of the model and the use of specialized blocks (such as Rate Transitions) that apply to multirate models.

# Configure Multirate Models for HDL Code Generation

## In this section...

“Overview” on page 10-3

“Configuring Model Parameters” on page 10-3

“Configuring Sample Rates in the Model” on page 10-4

“Constraints for Rate Transition Blocks and Other Blocks in Multirate Models” on page 10-4

## Overview

Certain requirements and restrictions apply to multirate models that are intended for HDL code generation. This section provides guidelines on how to configure model and block parameters to meet these requirements.

## Configuring Model Parameters

Before generating HDL code, configure the parameters of your model using the `hdlsetup` command. This sets up your multirate model for HDL code generation. This section summarizes settings applied to the model by `hdlsetup` that are relevant to multirate code generation. These include:

- **Solver** options that are recommended or required for HDL code generation:
  - **Type:** Fixed-step.
  - **Solver:** Discrete (no continuous states). Other fixed-step solvers could be selected, but this option is usually best for simulating discrete systems.
  - **Tasking mode:** Must be explicitly set to `SingleTasking`. Do not set **Tasking mode** to `Auto`.
- `hdlsetup` configures the following **Diagnostics / Sample time** options for all models:
  - **Multitask rate transition:** error
  - **Single task rate transition:** error

In multirate models intended for HDL code generation, Rate Transition blocks must be explicitly inserted when blocks running at different rates are connected. Setting **Multitask rate transition** and **Single task rate transition** to error to detect illegal rate transitions before code is generated.

## Configuring Sample Rates in the Model

The coder requires that at least one valid sample rate (sample time > 0) must exist in the model. If all rates are 0, -1, or -2, the code generator (makehdl) and compatibility checker (checkhdl) terminates with an error message.

## Constraints for Rate Transition Blocks and Other Blocks in Multirate Models

This section describes constraints you should observe when configuring Rate Transition, Upsample, Downsample, Zero-Order Hold, and various types of delay blocks in multirate models intended for HDL code generation.

### Rate Transition Blocks

Rate Transition blocks must be explicitly inserted into the signal path when blocks running at different rates are connected. For general information about the Rate Transition block, see the Rate Transition block documentation.

Make sure the data transfer properties for Rate Transition blocks are set as follows:

- **Ensure deterministic data transfer:** Selected.
- **Ensure data integrity during data transfer:** Selected.

### Upsample

When configuring Upsample blocks, set **Frame based mode** to Maintain input frame size.

When the Upsample block is in this mode, **Initial conditions** has no effect on generated code.



## Downsample

Configure Downsample blocks as follows:

- Set **Frame based mode** to Maintain input frame size.
- Set **Sample based mode** to Allow multirate.

Given these Downsample block settings, **Initial conditions** has no effect on generated code if **Sample offset** is set to 0.

## Delay and Zero-Order Hold Blocks

Use Rate Transition blocks, rather than the following blocks, to create rate transitions in models intended for HDL code generation:

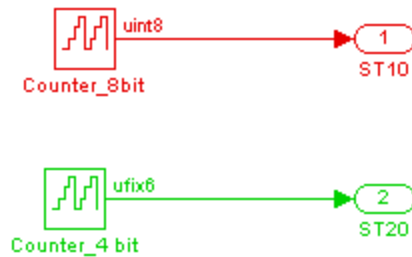
- Delay
- Tapped Delay
- Unit Delay
- Unit Delay Enabled
- Zero-Order Hold

The Delay blocks listed should be configured to have the same input and output sample rates.

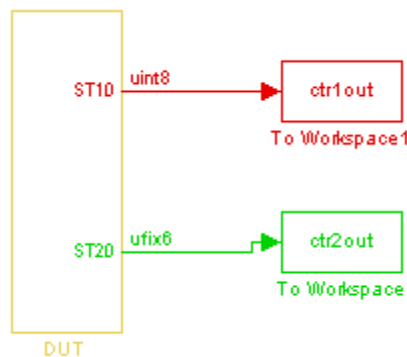
Zero-Order Hold blocks must be configured with inherited (–1) sample times.

## Code Generation from a Multirate DUT

The following block diagram shows the interior of a subsystem containing blocks that are explicitly configured with different sample times. The upper and lower Counter Free-Running blocks have sample times of 10 s and 20 s respectively. The counter output signals are routed to output ports ST10 and ST20, which inherit their sample times. The signal path terminating at ST10 runs at the base rate of the model; the signal path terminating at ST20 is a subrate signal, running at half the base rate of the model.



As shown in the next figure, the outputs of the multirate DUT drive To Workspace blocks in the test bench. These blocks inherit the sample times of the DUT outputs.



The following listing shows the VHDL entity declaration generated for the DUT.

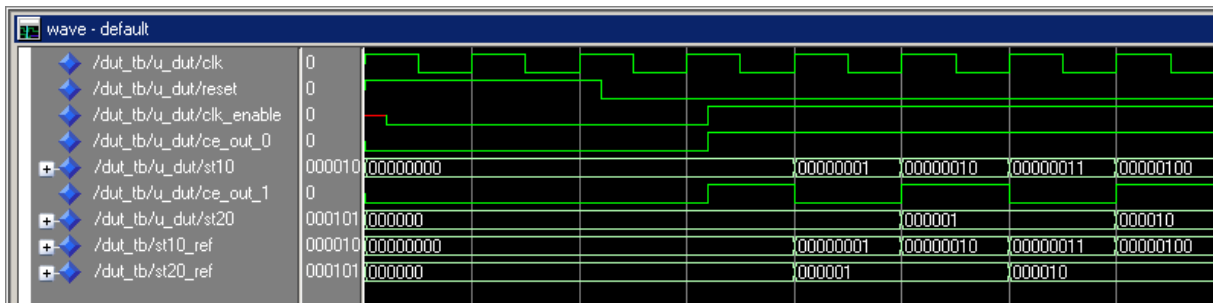
```

ENTITY DUT IS
  PORT( clk
        : IN   std_logic;
        reset
        : IN   std_logic;
        clk_enable
        : IN   std_logic;
        ce_out_0
        : OUT  std_logic;
        ce_out_1
        : OUT  std_logic;
        ST10
        : OUT  std_logic_vector(7 DOWNTO 0); -- uint8
        ST20
        : OUT  std_logic_vector(5 DOWNTO 0) -- ufix6
        );
END DUT;

```

The entity has the standard clock, reset, and clock enable inputs and data outputs for the ST10 and ST20 signals. In addition, the entity has two clock enable outputs (ce\_out\_0 and ce\_out\_1). These clock enable outputs replicate internal clock enable signals maintained by the timing controller entity.

The following figure, showing a portion of a Mentor Graphics ModelSim simulation of the generated VHDL code, lets you observe the timing relationship of the base rate clock (clk), the clock enables, and the computed outputs of the model.



After the assertion of clk\_enable (replicated by ce\_out\_0), a new value is computed and output to ST10 for every cycle of the base rate clock.

A new value is computed and output for subrate signal ST20 for every other cycle of the base rate clock. An internal signal, `enb_1_2_1` (replicated by `ce_out_1`) governs the timing of this computation.

## Generate a Global Oversampling Clock

### In this section...

“Why Use a Global Oversampling Clock?” on page 10-9

“Requirements for the Oversampling Factor” on page 10-9

“Specifying the Oversampling Factor From the GUI” on page 10-10

“Specifying the Oversampling Factor From the Command Line” on page 10-12

“Resolving Oversampling Rate Conflicts” on page 10-12

### Why Use a Global Oversampling Clock?

In many designs, the DUT is not self-contained. For example, consider a DUT that is part of a larger system that supplies timing signals to its components under control of a global clock. The global clock typically runs at a higher rate than some of the components under its control. By specifying such a *global oversampling clock*, you can integrate your DUT into a larger system without using Upsample or Downsample blocks.

To generate global clock logic, you specify an *oversampling factor*. The oversampling factor expresses the desired rate of the global oversampling clock as a multiple of the base rate of your model.

When you specify an oversampling factor, the coder generates the global oversampling clock and derives the required timing signals from clock signal. Generation of the global oversampling clock affects only generated HDL code. The clock does not affect the simulation behavior of your model.

### Requirements for the Oversampling Factor

When you specify the oversampling factor for a global oversampling clock, note these requirements:

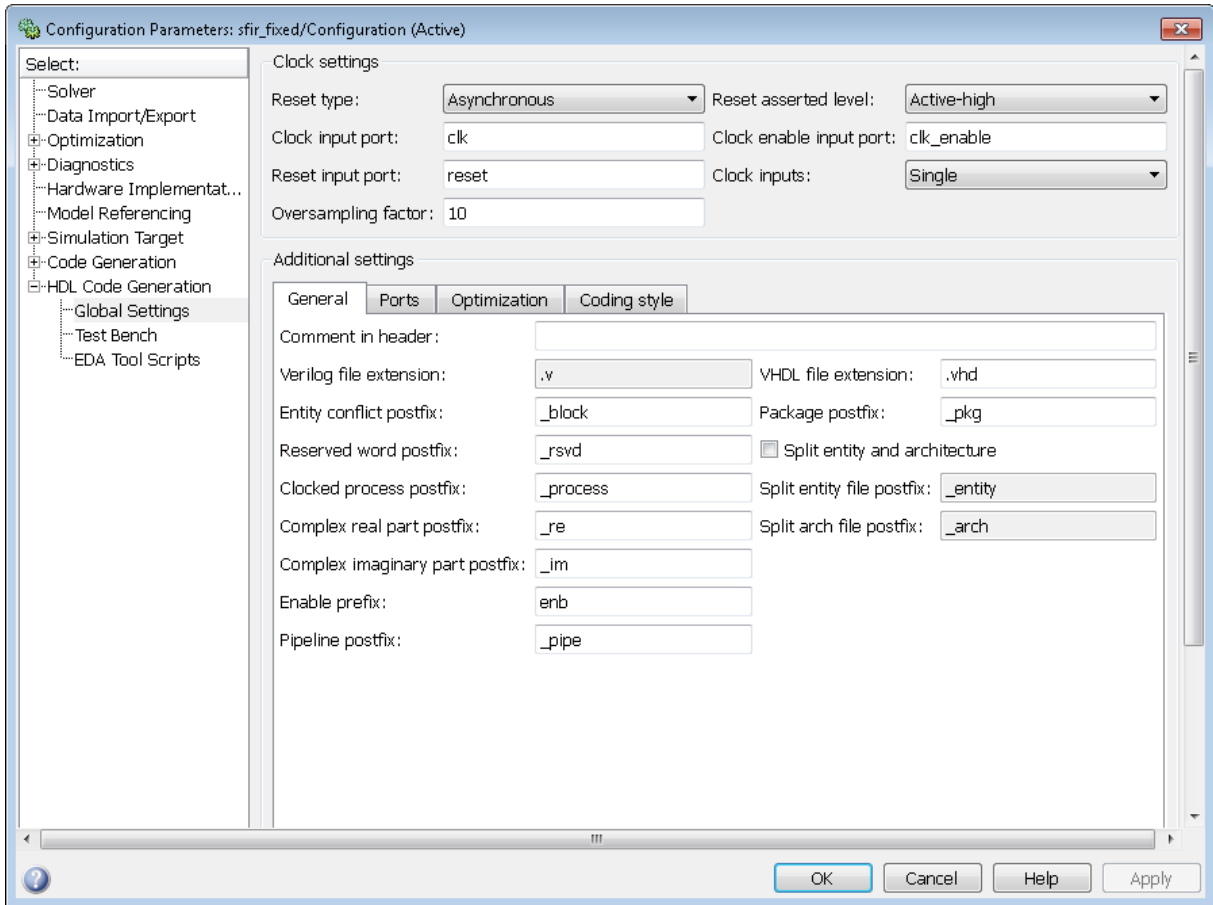
- The oversampling factor must be an integer greater than or equal to 1.
- The default value is 1. In the default case, the coder does not generate a global oversampling clock.

- Some DUTs require multiple sampling rates for their internal operations. In such cases, the other rates in the DUT must divide evenly into the global oversampling rate. For more information, see “Resolving Oversampling Rate Conflicts” on page 10-12 .

### Specifying the Oversampling Factor From the GUI

You can specify the oversampling factor for a global clock from the GUI as follows:

- 1 Select the **HDL Code > Global Settings** pane in the Model Configuration Parameters dialog box.
- 2 For **Oversampling factor** in the **Clock settings** section, enter the desired oversampling factor. In the following figure, **Oversampling factor** specifies a global oversampling clock that runs at ten times the base rate of the model.



**3** Click **Generate** on the **HDL Code** pane to initiate code generation.

The coder reports the oversampling clock rate:

```
### Begin VHDL Code Generation
### MESSAGE: The design requires 10 times faster clock with respect to the base rate = 1.
### Working on symmetric_fir_tc as hdlsrc/symmetric_fir_tc.vhd
### Working on sfir_fixed/symmetric_fir as hdlsrc/symmetric_fir.vhd
### HDL Code Generation Complete.
```

## Specifying the Oversampling Factor From the Command Line

You can specify the oversampling factor for a global clock from the command line by setting the 'Oversampling', N property in the makehdl command. The following example specifies an oversampling factor of 7:

```
>> makehdl(gcb,'Oversampling', 7)
### Generating HDL for 'sfir_fixed/symmetric_fir'
### Starting HDL Check.
### HDL Check Complete with 0 errors, 0 warnings and 0 messages.

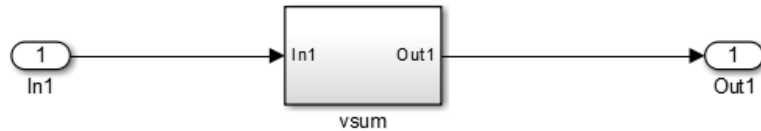
### Begin VHDL Code Generation
### MESSAGE: The design requires 7 times faster clock with respect to the base rate = 1.
### Working on symmetric_fir_tc as hdlsrc\symmetric_fir_tc.vhd
### Working on sfir_fixed/symmetric_fir as hdlsrc\symmetric_fir.vhd
### HDL Code Generation Complete.
```

## Resolving Oversampling Rate Conflicts

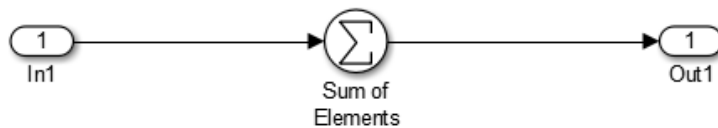
The HDL realization of some designs is inherently multirate, even though the original Simulink model is single-rate. As an example, consider the `simplevectorsum_cascade` model (also discussed in “Latency Differences in an Area-Optimized Model” on page 12-8).

This model consists of a subsystem, `vsum`, driven by a vector input of width 10, with a scalar output. The following figure shows the root level of the model.





The device under test is the `vsum` subsystem, shown in the following figure. The subsystem contains a Sum block, configured for vector summation.



The `simplevectorsum_cascade` model specifies a cascaded implementation (`SumCascadeHDL Emission`) for the Sum block. The generated HDL code for a cascaded vector Sum block implementation runs at two effective rates: a faster (oversampling) rate for internal computations and a slower rate for input/output. The coder reports that the inherent oversampling rate for the DUT is five times the base rate:

```
>> dut = 'simplevectorsum_cascade/vsum';
>> makehdl(dut);
### Generating HDL for 'simplevectorsum_cascade/vsum'
### Starting HDL Check.
### HDL Check Complete with 0 errors, 0 warnings and 0 messages.

### The code generation and optimization options you have chosen have introduced
    additional pipeline delays.
### The delay balancing feature has automatically inserted matching delays for
    compensation.
### The DUT requires an initial pipeline setup latency. Each output port
    experiences these additional delays
### Output port 0: 1 cycles

### Begin VHDL Code Generation
### MESSAGE: The design requires 5 times faster clock with respect to the
    base rate = 1.
...

```

In some cases, the clock requirements for such a DUT conflict with the global oversampling rate. To avoid oversampling rate conflicts, verify that subrates in the model divide evenly into the global oversampling rate.

For example, if you request a global oversampling rate of 8 for the `simplevectorsum_cascade` model, the coder displays a warning and ignores the requested oversampling factor. The coder instead respects the oversampling factor that the DUT requests:

```
>> dut = 'simplevectorsum_cascade/vsum';
>> makehdl(dut,'Oversampling',8);
### Generating HDL for 'simplevectorsum/vsum'
### Starting HDL Check.
### HDL Check Complete with 0 errors, 0 warnings and 0 messages.

### The code generation and optimization options you have chosen have introduced
    additional pipeline delays.
### The delay balancing feature has automatically inserted matching delays for
    compensation.
### The DUT requires an initial pipeline setup latency. Each output port

```

```
    experiences these additional delays
### Output port 0: 1 cycles

### Begin VHDL Code Generation
### WARNING: The design requires 5 times faster clock with respect to
    the base rate = 1, which is incompatible with the oversampling
    value (8). Oversampling value is ignored.
...

```

An oversampling factor of 10 works in this case:

```
>> dut = 'simplevectorsum_cascade/vsum';
>> makehdl(dut,'Oversampling',10);
### Generating HDL for 'simplevectorsum_cascade/vsum'
### Starting HDL Check.
### HDL Check Complete with 0 errors, 0 warnings and 0 messages.

### The code generation and optimization options you have chosen have introduced
    additional pipeline delays.
### The delay balancing feature has automatically inserted matching delays for
    compensation.
### The DUT requires an initial pipeline setup latency. Each output port
    experiences these additional delays
### Output port 0: 1 cycles

### Begin VHDL Code Generation
### MESSAGE: The design requires 10 times faster clock with respect to
    the base rate = 1.
...

```

## Generate Multicycle Path Information Files

### In this section...

“Overview” on page 10-16

“Format and Content of a Multicycle Path Information File” on page 10-17

“File Naming and Location Conventions” on page 10-23

“Generating Multicycle Path Information Files Using the GUI” on page 10-23

“Generating Multicycle Path Information Files Using the Command Line” on page 10-24

“Limitations” on page 10-24

“Example of Generating a Multicycle Path Information File” on page 10-26

### Overview

The coder implements multirate systems in HDL by generating a master clock running at the model’s base rate, and generating subrate timing signals from the master clock (see also “Code Generation from Multirate Models” on page 10-2). The propagation time between two subrate registers can be more than one cycle of the master clock. A *multicycle path* is a path between two such registers.

When synthesizing HDL code, it is often useful to provide an analysis of multicycle register-to-register paths to the synthesis tool. If the synthesis tool can identify multicycle paths, you may be able to:

- Realize higher clock rates from your multirate design.
- Reduce the area of your design.
- Reduce the execution time of the synthesis tool.

Using the **Generate multicycle path information** option (or the equivalent `'MulticyclePathInfo'` property for `makehdl`) you can instruct the coder to analyze multicycle paths in the generated code, and generate a *multicycle path information file*.

A multicycle path information file is a text file that describes one or more *multicycle path constraints*. A multicycle path constraint is a *timing exception* – it relaxes the default constraints on the system timing by allowing signals on a given path to have a longer propagation time. When using multiple clock mode, the file also contains clock definitions.

Typically a synthesis tool gives every signal a time budget of exactly 1 clock cycle to propagate from a source register to a destination register. A timing exception defines a *path multiplier*  $N$  that informs the synthesis tool that a signal has  $N$  clock cycles ( $N > 1$ ) to propagate from the source to destination register. The path multiplier expresses some number of cycles of a *relative clock* at either the source or destination register. Where a timing exception is defined for a path, the synthesis tool has more flexibility in meeting the timing requirements for that path and for the system as a whole.

The generated multicycle path information file does not follow the native constraint file format of a particular synthesis tool. The file contains the multicycle path information required by popular synthesis tools. You can manually convert this information to multicycle path constraints in the format required by your synthesis tool, or write a script or tool to perform the conversion. The next section describes the format of a multicycle path constraint file in detail.

## Format and Content of a Multicycle Path Information File

The following listing shows a simple multicycle path information file.

```

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Constraints Report
%   Module: Sbs
%   Model: mSbs.mdl
%
%   File Name:hdlsrc/Sbs_constraints.txt
%   Created: 2009-04-10 09:50:10
%   Generated by MATLAB 7.9 and HDL Coder 1.6
%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

```

```

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Multicycle Paths
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
FROM : Sbs.boolireg; TO : Sbs.booloreg; PATH_MULT : 2; RELATIVE_CLK : source,
      Sbs.clk;
FROM : Sbs.boolireg_v<0>; TO : Sbs.booloreg_v<0>; PATH_MULT : 2;
      RELATIVE_CLK : source, Sbs.clk;
FROM : Sbs.doubireg; TO : Sbs.douboreg; PATH_MULT : 2; RELATIVE_CLK : source,
      Sbs.clk;
FROM : Sbs.doubireg_v<0>; TO : Sbs.douboreg_v<0>; PATH_MULT : 2;
      RELATIVE_CLK : source, Sbs.clk;
FROM : Sbs.intireg(7:0); TO : Sbs.intoreg(7:0); PATH_MULT : 2;
      RELATIVE_CLK : source, Sbs.clk;
FROM : Sbs.intireg_v<0>(7:0); TO : Sbs.intoreg_v<0>(7:0); PATH_MULT : 2
      RELATIVE_CLK : source, Sbs.clk;

```

The first section of the file is a header that identifies the source model and gives other information about how the coder generated the file. this section terminates with the following comment lines:

```

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Multicycle Paths
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

```

---

**Note** For a single-rate model or a model without multicycle paths, the coder generates only the header section of the file.

---

The main body of the file follows. This section contains a flat table, each row of which defines a multicycle path constraint.

Each constraint consists of four fields. The format of each field is one of the following:

- KEYWORD : field;
- KEYWORD : subfield1,... subfield\_N;

The keyword identifies the type of information contained in the field. The keyword string in each field terminates with a space followed by a colon.

The delimiter between fields is the semicolon. Within a field, the delimiter between subfields is the comma.

The following table defines the fields of a multicycle path constraint, in left-to-right order.

Keyword : field (or subfields)	Field Description
FROM : src_reg_path;	The source (or FROM) register of a multicycle path in the system. The value of <code>src_reg_path</code> is the HDL path of the source register's output signal. See also "Register Path Syntax for FROM : and TO : Fields" on page 10-21 .
TO : dst_reg_path;	The destination (or TO) register of a multicycle path in the system. The FROM register drives the TO register in the HDL code. The value of <code>dst_reg_path</code> is the HDL path of the destination register's output signal. See also "Register Path Syntax for FROM : and TO : Fields" on page 10-21.
PATH_MULT : N;	<p>The <i>path multiplier</i> defines the number of clock cycles that a signal has to propagate from the source to destination register. The <code>RELATIVE_CLK</code> field describes the clock associated with the path multiplier (the <i>relative clock</i> for the path).</p> <p>The path multiplier value N indicates that the signal has N clock cycles of its relative clock to propagate from source to destination register.</p> <p>The coder does not report register-to-register paths where N = 1, because this is the default path multiplier.</p>
RELATIVE_CLK : relclock, sysclock;	<p>The <code>RELATIVE_CLK</code> field contains two comma-delimited subfields. Each subfield expresses the location of the relative clock in a different form, for the use of different synthesis tools. The subfields are:</p> <ul style="list-style-type: none"> <li>• <code>relclock</code>: Since the coder currently generates only single-clock systems, this subfield takes the value <code>source</code>. In a multi-clock system, the relative clock associated with a multicycle path could be either the source or destination register of the path, and this subfield could take on either of the values <code>source</code> or <code>destination</code>. This usage is reserved for future release of the coder.</li> <li>• <code>sysclock</code>: This subfield is intended for use with synthesis tools that require the actual propagation time for a multicycle path. <code>sysclock</code> provides the path to the system's top-level clock (e.g., <code>Sbs.clk</code>) You can use the period of this clock and the path multiplier to calculate the propagation time for a given path.</li> </ul>



## Register Path Syntax for FROM : and TO : Fields

The FROM : and TO: fields of a multipath constraint provide the path to a source or destination register and information about the signal data type, size, and other characteristics.

**Fixed Point Signals.** For fixed point signals, the register path has the form

```
reg_path<ps> (hb:lb)
```

where:

- `reg_path` is the HDL hierarchical path of the signal. The delimiter between hierarchical levels is the period, for example: `Sbs.u_H1.initreg`.
- `<ps>`: Part select (zero-origin integer index) for vector signals. Angle brackets `<>` delimit the part select field
- `(hb:lb)`: Bit select field, indicated from high-order bit to low-order bit. The signal width `(hb:lb)` is the same as the defined width of the signal in the HDL code. This representation does not necessarily imply that the bits of the FROM : register are connected to the corresponding bits of the TO: register. The actual bit-to-bit connections are determined during synthesis.

**Boolean and Double Signals.** For boolean and double signals, the register path has the form

```
reg_path<ps>
```

where:

- `reg_path` is the HDL hierarchical path of the signal. The delimiter between hierarchical levels is the period (`.`), for example: `Sbs.u_H1.initreg`.
- `<ps>`: Part select (zero-origin integer index) for vector signals. Angle brackets `<>` delimit the part select field

For boolean and double signals, no bit select field is present.

---

**Note** The format does not distinguish between boolean and double signals.

---

**Examples.** The following table gives several examples of register-to-register paths as represented in a multicycle path information file.

Path	Description
FROM : Sbs.intireg(7:0); TO : Sbs.intoreg(7:0);	Both signals are fixed point and eight bits wide.
FROM : Sbs.intireg; TO : Sbs.intoreg;	Both signals are either boolean or double.
FROM : Sbs.intireg<0>(7:0); TO : Sbs.intoreg<1>(7:0);	The FROM signal is the first element of a vector. The TO signal is the second element of a vector. Both signals are fixed point and eight bits wide.
FROM : Sbs.u_H1.intireg(7:0); TO : Sbs.intoreg(7:0);	The signal intireg is defined in the module H1, and H1 is inside the module Sbs. u_H1 is the instance name of H1 in Sbs. Both signals are fixed point and eight bits wide.

### Ordering of Multicycle Path Constraints

For a given model or subsystem, the ordering of multicycle path constraints within a multicycle path information file may vary depending on whether the target language is VHDL or Verilog, and on other factors. The ordering of constraints may also change in future versions of the coder. When you design scripts or other tools that process multicycle path information file, do not build in any assumptions about the ordering of multicycle path constraints within a file.

### Clock Definitions

When you use multiple clock mode, the multicycle path information file also contains a "Clock Definitions" section, as shown in the following listing. This section is located after the header and before the "Multicycle Paths" section.

```

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Clock Definitions
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
CLOCK: Sbs.clk PERIOD: 0.05
CLOCK: Sbs.clk_1_2 BASE_CLOCK: Sbs.clk MULTIPLIER: 2 PERIOD: 0.1

```

The following table defines the fields for the clock definitions.

<b>Keyword : field (or subfields)</b>	<b>Field Description</b>
CLOCK: clock_name	Each clock in the design has a CLOCK definition line.
PERIOD: float_value	The Simulink rate (floating point value) associated with this CLOCK.
BASE_CLOCK: base_clock_name	Names the master clock. This field does not appear on the master clock.
MULTIPLIER: int_value	Gives the ratio of the period of this clock to the master clock. This field does not appear on the master clock.

## File Naming and Location Conventions

The file name for the multicycle path information file derives from the name of the DUT and the postfix string '\_constraints', as follows:

*DUTname\_constraints.txt*

For example, if the DUT name is `symmetric_fir`, the name of the multicycle path information file is `symmetric_fir_constraints.txt`.

The coder writes the multicycle path information file to the target .

## Generating Multicycle Path Information Files Using the GUI

By default, the coder does not generate multicycle path information files. To enable generation of multicycle path information files, select **Generate multicycle path information** in the **HDL Code > EDA Tool Scripts** pane of the Model Configuration Parameters dialog box.

When you select **Generate multicycle path information**, the coder generates a multicycle path information file each time you initiate code generation.

## Generating Multicycle Path Information Files Using the Command Line

To generate a multicycle path information file from the command line, pass in the property/value pair 'MulticyclePathInfo', 'on' to makehdl, as in the following example.

```
>> dut = 'hdlfirtdecim_multicycle/Subsystem';
>> makehdl(dut, 'MulticyclePathInfo','on');
### Generating HDL for 'hdlfirtdecim_multicycle/Subsystem'
### Starting HDL Check.
### HDL Check Complete with 0 errors, 0 warnings and 1 message.

### MESSAGE: For the block 'hdlfirtdecim_multicycle/Subsystem/downsamp0'
    The initial condition may not be used when the sample offset is 0.

### Begin VHDL Code Generation
### Working on Subsystem_tc as hdlsrc\Subsystem_tc.vhd
### Working on hdlfirtdecim_multicycle/Subsystem as hdlsrc\Subsystem.vhd
### Generating package file hdlsrc\Subsystem_pkg.vhd
### Finishing multicycle path connectivity analysis.
### Writing multicycle path information in hdlsrc\Subsystem_constraints.txt
### HDL Code Generation Complete.
```

## Limitations

### Unsupported Blocks and Implementations

The following table lists block implementations (and associated Simulink blocks) that will not contribute to multicycle path constraints information.

Implementation	Block(s)
SumCascadeHDLEmission	Add, Subtract, Sum, Sum of Elements
ProductCascadeHDLEmission	Product, Product of Elements
MinMaxCascadeHDLEmission	MinMax, Maximum, Minimum
ModelReferenceHDLInstantiation	Model
SubsystemBlackBoxHDLInstantiation	Subsystem

Implementation	Block(s)
RamBlockDualHDLInstantiation	Dual Port RAM
RamBlockSimpDualHDLInstantiation	Simple Dual Port RAM
RamBlockSingleHDLInstantiation	Single Port RAM

## Limitations on MATLAB Function Blocks and Stateflow Charts

**Loop-Carried Dependencies.** The coder does not generate constraints for MATLAB Function blocks or Stateflow charts that contain a for loop with a loop-carried dependency.

**Indexing Vector or Matrix Variables.** In order to generate constraints for a vector or matrix index expression, the index expression must be one of the following:

- A constant
- A for loop induction variable

For example, in the following example of code for a MATLAB Function block, the index expression `reg(i)` does not generate constraints.

```
,
function y = fcn(u)
%#codegen

N=length(u);
persistent reg;
if isempty(reg)
    reg = zeros(1,N);
end

y = reg;

for i = 1:N-1
    reg(i) = u(i) + reg(i+1);
end
```

```
reg(N) = u(N);
```

### **File Generation Time**

---

**Tip** Generation of constraint files for large models can be slow.

---

### **Example of Generating a Multicycle Path Information File**

The “Getting Started with Multicycle Path Constraint Generation” example illustrates generation of a multicycle path information file using a model of a decimating filter. To open the example, enter the following at the command line:

```
showdemo hdlmulticyclepath
```

# HDL Properties for Controlling Multirate Code Generation

In this section...
“Overview” on page 10-27
“HoldInputDataBetweenSamples” on page 10-27
“OptimizeTimingController” on page 10-27

## Overview

This section summarizes coder properties that provide additional control over multirate code generation.

## HoldInputDataBetweenSamples

This property determines how long (in terms of base rate clock cycles) data values for subrate signals are held in a valid state.

When 'on' (the default), data values for subrate signals are held in a valid state across each subrate sample period.

When 'off', data values for subrate signals are held in a valid state for only one base-rate clock cycle. See `HoldInputDataBetweenSamples` for details.

## OptimizeTimingController

This property specifies whether the timing controller generates the required rates using multiple counters per rate (the default) or a single counter. The use of multiple counters optimizes generated code for speed and area. See `OptimizeTimingController` for details.





# The hdl demolib Block Library

---

- “Open the hdl demolib Library” on page 11-2
- “RAM Blocks” on page 11-3
- “RAM Without a Clock Enable” on page 11-13
- “ROM Generation Using Basic Simulink Blocks” on page 11-14
- “FIR Filter with Dual Port RAM Block” on page 11-15
- “HDL Counter” on page 11-16
- “HDL FFT” on page 11-28
- “Signal Processing with the HDL FFT Block” on page 11-36
- “HDL FIFO” on page 11-37
- “HDL Streaming FFT” on page 11-41
- “Bitwise Operators” on page 11-51

### Open the hdldemo1ib Library

The hdldemo1ib library provides HDL-specific implementations supporting simulation and code generation for:

- Single and dual-port RAMs
- Counter with single-shot and free-running modes
- Minimum resource FFT
- Operations on bits and bit fields
- FIFO (Queue)

These blocks are implemented as subsystems. The blocks provide HDL-specific functionality that is not currently supported by other Simulink blocks.

To open the hdldemo1ib library, type the following command at the MATLAB prompt:

```
hdldemo1ib
```

## RAM Blocks

### In this section...

- “Overview of RAM Blocks” on page 11-3
- “Dual Port RAM Block” on page 11-4
- “Simple Dual Port RAM Block” on page 11-7
- “Single Port RAM Block” on page 11-8
- “Code Generation for RAM Blocks” on page 11-11
- “Limitations for RAM Blocks” on page 11-12

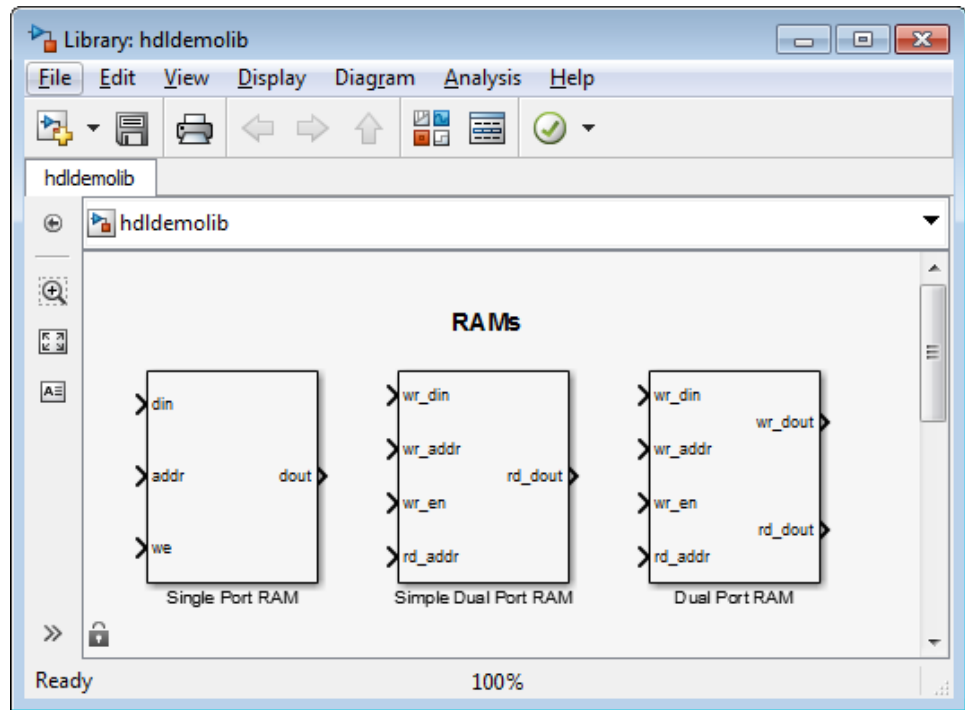
### Overview of RAM Blocks

The RAM blocks let you:

- Simulate the behavior of a single-port or dual-port RAM in your model.
- Generate an interface to the inputs and outputs of the RAM in HDL code.
- Generate RTL code that can be inferred as a RAM by most synthesis tools, for most FPGAs.

The RAM blocks are grouped together in the `hdl1demolib` library, as shown in the following figure. The library provides three type of RAM blocks:

- Dual Port RAM
- Simple Dual Port RAM
- Single Port RAM



To open the library, type the following command at the MATLAB prompt:

```
hdldemo1ib
```

Then, drag the desired RAM block from the `hdldemo1ib` library to your model, and set the block parameters and connect signals following the guidelines in the following sections.

## Dual Port RAM Block

### Dual Port RAM Block Ports and Parameters

The following figure shows the Dual Port RAM block.



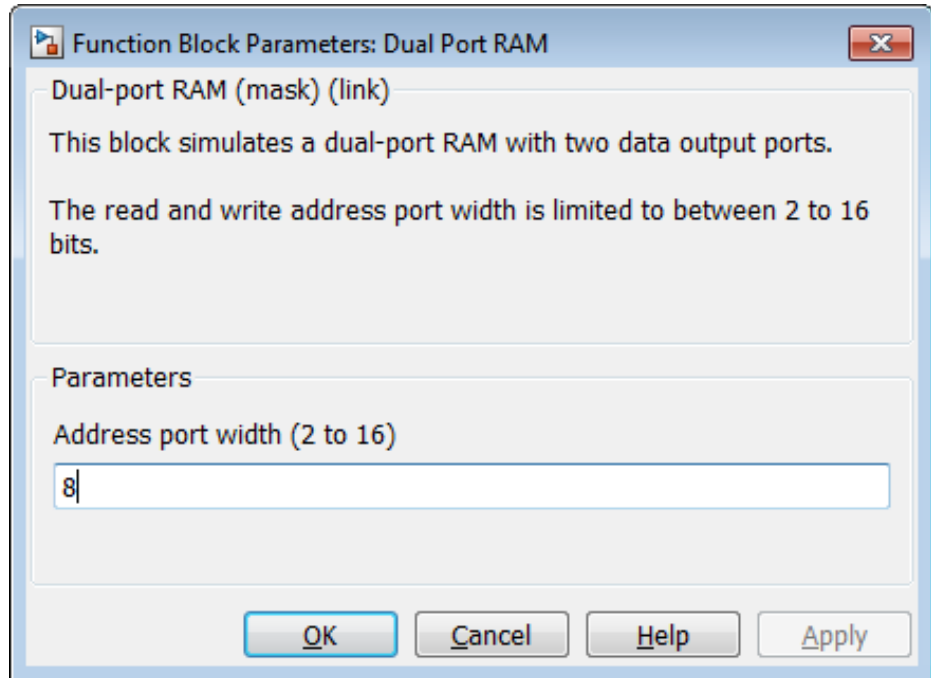
The block has the following input and output ports:

- **wr\_din** : Data input. Only scalar signals can be connected to this port. The data type of the input signal can be fixed point, integer, or complex, and can be of any width. The port inherits the width and data type of its input signal.
- **wr\_addr, rd\_addr**: Write and read address ports, respectively.

To set the width of the address ports, enter the desired width value (minimum width 2 bits, maximum width 16 bits ) into the **Address port width** field of the block GUI, as shown in the following figure. The default width is 8 bits.

The data type of signals connected to these ports must be unsigned integer (uintN) or unsigned fixed point (ufixN) with a fraction length of 0.

Vector signals are not accepted at the address ports.



- `wr_en`: Write enable. This port must be connected to a Boolean signal.
- `wr_dout`, `rd_dout`: Output ports with read data for addresses `wr_addr` and `rd_addr`, respectively.

---

**Tip** If data output at the write port is not required, you can achieve better RAM inference with synthesis tools by using the Simple Dual Port RAM block rather than the Dual Port RAM block.

---

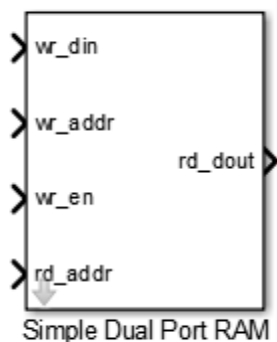
### Read-During-Write Behavior

During a write, new data appears at the output of the write port (`wr_dout`) of the Dual Port RAM block. If a read operation is performed at the same address at the read port, old data is read at the output (`rd_dout`).

## Simple Dual Port RAM Block

### Simple Dual Port RAM Block Ports and Parameters

The following figure shows the Simple Dual Port RAM block.



This block is similar to the Dual Port RAM. It differs from Dual Port RAM in its read-during-write behavior, and it does not have the data output at the write port (*wr\_dout*).

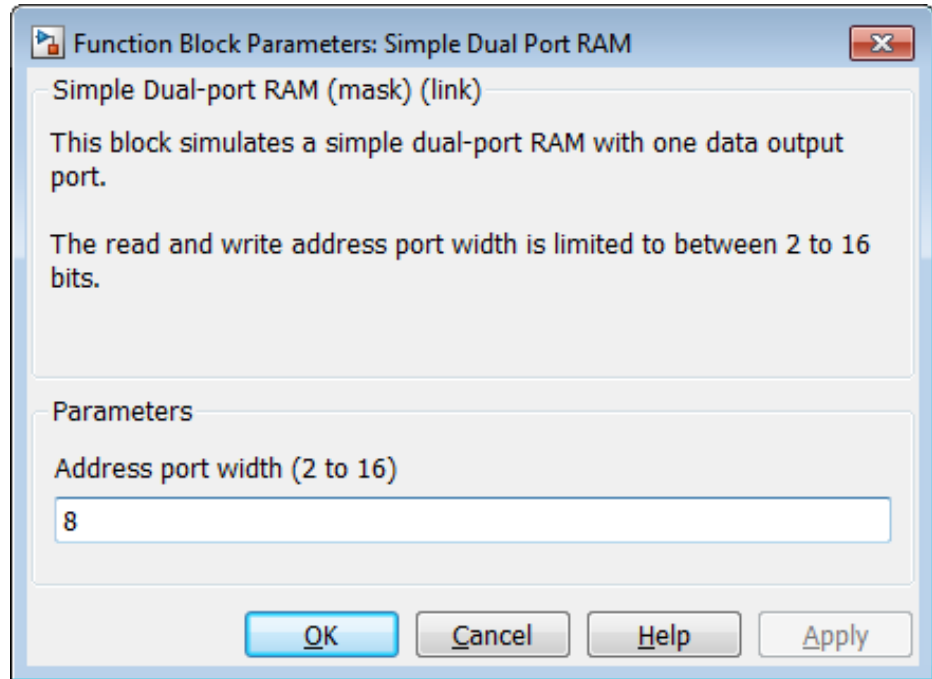
The block has the following input and output ports:

- *wr\_din* : Data input. Only scalar signals can be connected to this port. The data type of the input signal can be fixed point, integer, or complex, and can be of any width. The port inherits the width and data type of its input signal.
- *wr\_addr*, *rd\_addr*: Write and read address ports, respectively.

To set the width of the address ports, enter the desired width value (minimum width 2 bits, maximum width 16 bits) into the **Address port width** field of the block GUI, as shown in the following figure. The default width is 8 bits.

The data type of signals connected to these ports must be unsigned integer (*uintN*) or unsigned fixed point (*ufixN*) with a fraction length of 0.

Vector signals are not accepted at the address ports.



- `wr_en`: Write enable. This port must be connected to a Boolean signal.
- `rd_dout`: Output port with read data for addresses `wr_addr` and `rd_addr`, respectively.

### Read-During-Write Behavior

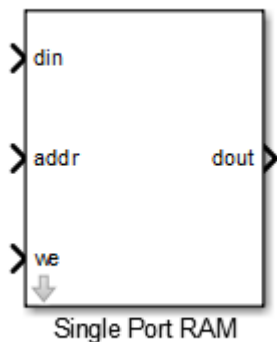
During a write operation, if a read operation is performed at the same address at the read port, old data is read at the output.

## Single Port RAM Block

### Single Port RAM Block Ports and Parameters

The following figure shows the Single Port RAM block.





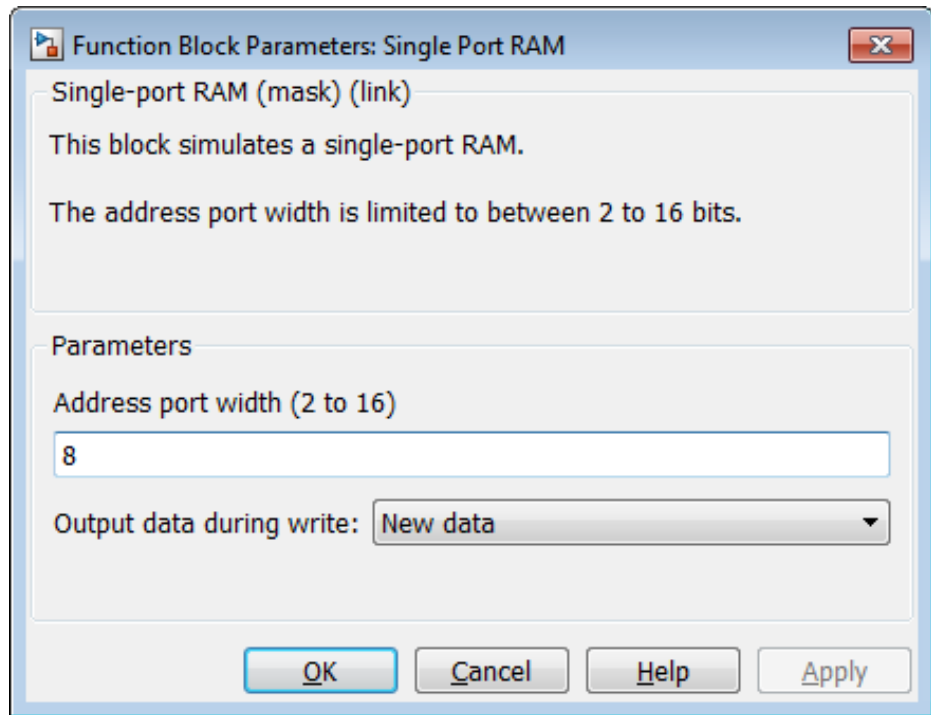
The block has the following input and output ports:

- **din** : Data input. Only scalar signals can be connected to this port. The data type of the input signal can be fixed point, integer, or complex, and can be of any width. The port inherits the width and data type of its input signal.
- **addr**: Write address port.

To set the width of the address ports, enter the desired width value (minimum width 2 bits, maximum width 16 bits) into the **Address port width** field of the block GUI, as shown in the following figure. The default width is 8 bits.

The data type of signals connected to these ports must be unsigned integer (`uintN`) or unsigned fixed point (`ufixN`) with a fraction length of 0.

Vector signals are not accepted at the address ports.



- we: Write enable. This port must be connected to a Boolean signal.
- dout: Output port with data for address addr.

### Read-During-Write Behavior

The **Output data during write** dropdown menu provides options that control how the RAM handles output/read data. These options are:

- New data (default): During a write, new data appears at the output port (dout).
- Old data: During a write, old data appears at the output port (dout).

---

**Note** Depending on your synthesis tool and target device, the setting of **Output data during write** may affect the result of RAM inference. See “Limitations for RAM Blocks” on page 11-12 for further information on read-during-write behavior in hardware.

---

## Code Generation for RAM Blocks

Code generation for a RAM block creates a separate file, *blockname.ext*, where *blockname* is derived from the name of the RAM block, and *ext* is the target language filename extension.

Code generated for RAM blocks has:

- A latency of 1 clock cycle for read data output.
- No reset signal, since some synthesis tools do not infer a RAM from HDL code if it includes a reset.

Most synthesis tools infer a RAM from the generated HDL code with default settings. However, your synthesis tool may not map the generated code to RAM for the following reasons:

- Small RAM size: your synthesis tool may use registers to implement a small RAM for better performance.
- A clock enable signal is present. You can suppress generation of a clock enable signal in RAM blocks, as described in “Implement RAMs With or Without Clock Enable” on page 11-11.

Please note that code generated to initialize a RAM is intended for simulation only, and may be ignored by synthesis tools.

## Implement RAMs With or Without Clock Enable

The `RAMArchitecture` property enables or suppresses generation of clock enable logic for all RAM blocks in a subsystem. You can set `RAMArchitecture` to the following values:

- `'WithClockEnable'` (default): Generates RAMs using HDL templates that include a clock enable signal, and an empty RAM wrapper.

- 'WithoutClockEnable': Generates RAMs without clock enables, and a RAM wrapper that implements the clock enable logic.

Some synthesis tools may not infer RAMs with a clock enable. Set `GlobalRAMArchitecture` to 'WithoutClockEnable' if your synthesis tool does not support RAM structures with a clock enable, and cannot map your generated HDL code to FPGA RAM resources. To learn how to generate RAMs without clock enables for your design, see the Getting Started with RAM and ROM example. To open the example, type the following command at the MATLAB prompt:

```
hdlcoderramrom
```

## Limitations for RAM Blocks

The following limitations apply to the use of RAM blocks in HDL code generation:

- If you use RAM blocks to perform concurrent read and write operations, you should manually verify the read-during-write behavior in hardware. The read-during-write behavior of the RAM blocks in Simulink matches that of the generated behavioral HDL code. However, a synthesis tool may not follow the same behavior during RAM inferring, causing the read-during-write behavior in hardware to differ from the behavior of the Simulink model or generated HDL code. Actual read-during-write behavior in hardware depends on how synthesis tools infer RAM from generated HDL code, and on the hardware architecture of the target device.

## RAM Without a Clock Enable

The RAM blocks in the `hdldemo1lib` library implement RAM structures using HDL templates that include a clock enable signal.

However, some synthesis tools do not support RAM inference with a clock enable. As an alternative, the coder provides a generic style of HDL templates that do not use a clock enable signal for the RAM structures. The generic RAM template implements clock enable with logic in a wrapper around the RAM.

You may want to use the generic RAM style if your synthesis tool does not support RAM structures with a clock enable, and cannot map generated HDL code to FPGA RAM resources. To learn how to use generic style RAM for your design, see the Getting Started with RAM and ROM example. To open the example, type the following command at the MATLAB prompt:

```
hdlcoderramrom
```

## **ROM Generation Using Basic Simulink Blocks**

HDL Coder does not provide a ROM block, but you can easily build one using basic Simulink blocks. The Getting Started with RAM and ROM example includes a ROM built using a 1-D Lookup Table block and a Unit Delay block. To open the example, type the following command at the MATLAB prompt:

```
hdlcoderramrom
```

## FIR Filter with Dual Port RAM Block

The RAM-Based FIR Filter example (`hdlcoderfirram`) generates VHDL code for a Dual Port RAM block. Run this example to acquaint yourself with the generated code.

The HDL device under test (DUT) in the model is the `FIR_RAM` subsystem. The `FIR_RAM` subsystem contains a Dual Port RAM block. The entity and architecture definitions generated for this block are written to `DualPortRAM_Inst0.vhd` .

The code generated for the top-level DUT, `FIR_RAM.vhd`, contains the component instantiation for the Dual Port RAM block.

## HDL Counter

### In this section...

“Overview” on page 11-16

“Counter Modes” on page 11-16

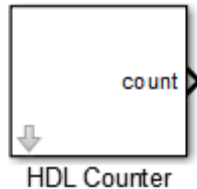
“Control Ports” on page 11-18

“Defining the Counter Data Type and Size” on page 11-21

“HDL Implementation and Implementation Parameters” on page 11-22

“Parameters and Dialog Box” on page 11-23

### Overview



The HDL Counter block implements a free-running or count-limited hardware counter that supports signed and unsigned integer and fixed-point data types.

The counter emits its value for the current sample time from the **count** output. By default, the counter does not have input ports. Optionally, you can add control ports that let you enable, disable, load, or reset the counter, or set the direction (positive or negative) of the counter.

### Counter Modes

The HDL Counter supports two operation modes, selected from the **Counter type** dropdown menu.



### Free Running Mode (default)

The counter is initialized to the value defined by the **Initial value** parameter upon assertion of a reset signal. The reset signal can be either the model's global reset, or a reset received through an optional **Local reset port** that you can define on the HDL Counter block.

On each sample time, the value defined by the **Step value** parameter is added to the counter, and the counter emits its current value at the count output. When the counter value overflows or underflows the counter's word size, the counter wraps around and continues the counting sequence until reset is asserted or the model stops running.

By default, the positive or negative direction of the count is determined by the sign of the **Step value**. Optionally, you can define a **Count direction** control port on the HDL Counter block.

**Free Running Mode Examples.** For a 4-bit unsigned integer counter with an **Initial value** of 0 and a **Step value** of 5, the counter output sequence is

0, 5, 10, 15, 4, 9, 14, 3, . . .

For a 4-bit signed integer counter with an **Initial value** of 0 and a **Step value** of -2, the counter output sequence is

0, -2, -4, -6, -8, 6, 4, 2, 0, -2, -4, . . .

### Count Limited Mode

The counter is initialized to the value defined by the **Initial value** parameter upon assertion of a reset signal. The reset signal can be either the model's global reset, or a reset received through an optional **Local reset port** that you can define on the HDL Counter block.

On each sample time, the value defined by the **Step value** parameter is added to the counter, and the current value is tested for equality with the value defined by the **Count to value** parameter. If the current value equals the **Count to value**, the counter is reloaded with the initial value. The counter then emits its current value at the count output.

If the counter value overflows or underflows the counter's word size, the counter wraps around and continues the counting sequence. The sequence continues until reset is asserted or the model stops running.

The condition for resetting the counter is exact equality. For some combinations of **Initial value**, **Step value**, and **Count to value**, the counter value may not reach the **Count to value**, or the counter may overflow and iterate through the counter range some number of times before reaching the **Count to value**.

By default, the positive or negative direction of the count is determined by the sign of the **Step value**. Optionally, you can define a **Count direction** control port on the HDL Counter block.

**Count Limited Mode Examples.** For an 8-bit signed integer counter with an **Initial value** of 0, a **Step value** of 2, and a **Count to value** of 8, the counter output sequence is

0 2 4 6 8 0 ...

For a 3-bit unsigned integer counter with an **Initial value** of 0, a **Step value** of 3, and a **Count to value** of 7, the counter output sequence is

0 3 6 1 4 7 0 3 6 1 4 7 ...

For a 3-bit unsigned integer counter with an **Initial value** of 0, a **Step value** of 2, and a **Count to value** of 7, the counter output sequence does not reach the **Count to value**:

0 2 4 6 0 2 4 6 ...

## Control Ports

By default, the HDL Counter does not have inputs. Control ports are optional inputs that you can add to the block to:

- Reset the counter independently from the global reset logic.
- Load the counter with a value.
- Enable or disable the counter.
- Set the positive or negative direction of the counter.

The following figure shows the HDL Counter block configured with all available control ports.



The following characteristics apply to control ports:

- Control ports are synchronous.
- All control ports except the load value input have Boolean data type.
- Control ports must have the same sample time.
- If control ports exist on the block, the HDL Counter block inherits its sample time from the ports, and the **Sample time** parameter on the block dialog box is disabled.
- Signals at control ports are active-high.

### Creating Control Ports for Loading and Resetting the Counter

By default, the counter is loaded (or reloaded) with the defined **Initial value** at the following times:

- When the model's global reset is asserted
- (In **Count limited** mode only) When the counter value equals the **Count to** value

You can further control reset and load behavior with signals connected to control ports. You can add these control ports to the block via the following options:

**Local reset port:** Select this option to create a reset input port on the block. The local reset port is labeled `rst`. The `rst` port should be connected to a Boolean signal. When this signal is set to 1, the counter resets to its initial value.

**Load ports:** When you select this option, two input ports, labeled `load` and `load_val`, are created on the block. The `load` port should be connected to a Boolean signal. When this signal is set to 1, the counter is loaded with the value at the `load_val` input. The load value must have the same data type as the counter.

### **Enabling or Disabling the Counter**

When you select the **Count enable** port option, a control port labeled `enb` is created on the block. The `enb` port should be connected to a Boolean signal. When this signal is set to 0, the counter is disabled and the current counter value is held at the output. When the `enb` signal is set to 1, the counter resumes operation.

### **Controlling the Counter Direction**

By default, the negative or positive direction of the counter is determined by the sign of the **Step value**. When you select the **Count direction** port option, a control port labeled `dir` is created on the block. The `dir` port should be connected to a Boolean signal. The `dir` signal determines the direction of the counter as follows:

- When the `dir` signal is set to 1, the step value is added to the current counter value to compute the next value.
- When the `dir` signal is set to 0, the step value is subtracted from the current counter value to compute the next value.

The following table summarizes the effect of the **Count direction** port.

Count Direction Signal Value	Step Value Sign	Actual Count Direction
1	+ (Positive)	Up
1	- (Negative)	Down
0	+ (Positive)	Down
0	- (Negative)	Up

### Priority of Control Signals

The following table defines the priority of control signals, and shows how the counter value is set in relation to the control signals.

rst	load	enb	dir	Next Counter Value
1	–	–	–	initial value
0	1	–	–	load_val value
0	0	0	–	current value
0	0	1	1	current value + step value
0	0	1	0	current value - step value

### Defining the Counter Data Type and Size

The HDL Counter block supports signed and unsigned integer and fixed-point data types. Use the following parameters to set the data type:

**Output data type:** Select Signed or Unsigned. The default is Unsigned.

**Word length:** Enter the desired number of bits (including the sign bit) for the counter.

Default: 8

Minimum: 1 if **Output data type** is Unsigned, 2 if **Output data type** is Signed

Maximum: 125

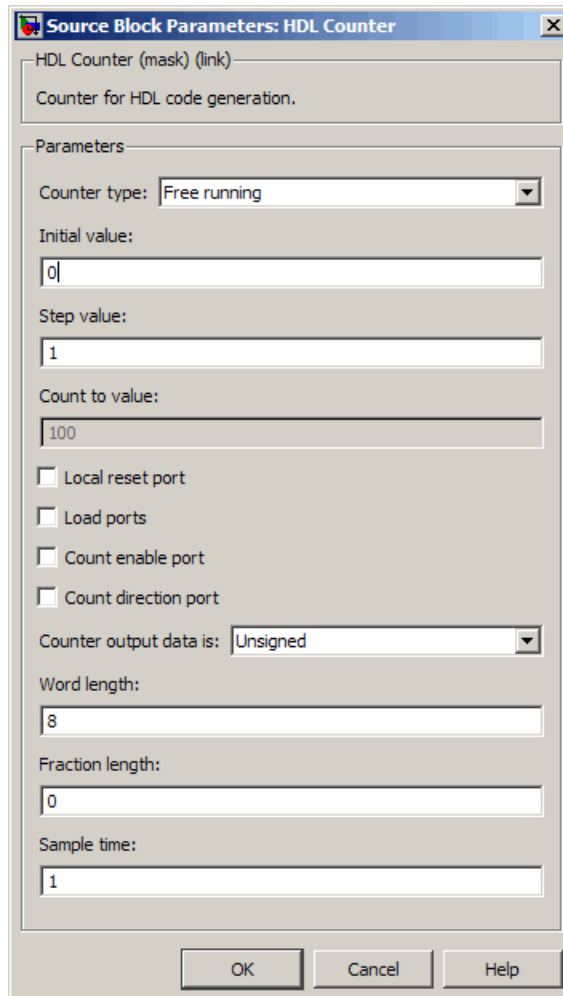
**Fraction length:** To define an integer counter, accept the default **Fraction length** of 0. To define a fixed-point counter, enter the number of bits to the right of the binary point.

## **HDL Implementation and Implementation Parameters**

Implementation: default

Implementation Parameters: InputPipeline, OutputPipeline

## Parameters and Dialog Box



### Counter type

Default: Free running

This dropdown menu selects the operation mode of the counter (see “Counter Modes” on page 11-16). The operation modes are:

- Free running
- Count limited

When `Count limited` is selected, the **Count to value** field is enabled.

### **Initial value**

Default: 0

By default, the counter is loaded (or reloaded) with the defined **Initial value** at the following times:

- When the model's global reset is asserted.
- (In **Count limited** mode only) When the counter value equals the **Count to value**. See also "Count Limited Mode" on page 11-17.

### **Step value**

Default: 1

The **Step value** is an increment that is added to the counter on each sample time. By default (i.e., in the absence of a count direction control signal) the sign of the step value determines the count direction (see also "Controlling the Counter Direction" on page 11-20).

Set **Step value** to a nonzero value that can be represented in the counter's data type precision without rounding. The magnitude (absolute value) of the step value must be a number that can be represented with the counter's data type.

For a signed N-bit integer counter:

- The range of counter values is  $-(2^{N-1}) \dots (2^{N-1} - 1)$ .
- The range of legal step values is  $-(2^{N-1} - 1) \dots (2^{N-1} - 1)$  (zero is excluded).

For example, for a 4-bit signed integer counter, the counter range is  $[-8 \dots 7]$ , but the ranges of legal step values are  $[-7 \dots -1]$  and  $[1 \dots 7]$ .



### Count to value

Default: 100

The **Count to value** field is enabled when the **Count limited counter mode** is selected. When the counter value is equal to the **Count to value**, the counter resets to the **Initial value** and continues counting. The condition for resetting the counter is exact equality. For some combinations of **Initial value**, **Step value**, and **Count to value**, the counter value may not reach the **Count to value**, or the counter may overflow and iterate through the counter range some number of times before reaching the **Count to value** (see “Count Limited Mode” on page 11-17).

Set **Count to value** to a value that is not equal to the **Initial value**.

### Local reset port

Default: cleared

Select this option to create a reset input port on the block. Only Boolean signals should be connected to this port. The port is labeled **rst**. See “Creating Control Ports for Loading and Resetting the Counter” on page 11-19.

### Load ports

Default: cleared

Select this option to create load and load value input ports on the block. The ports are labeled **load** and **load\_val**, respectively. The signal applied to the **load** port must be Boolean. The signal applied to the **load\_val** port must have the same data type as the counter. See also “Creating Control Ports for Loading and Resetting the Counter” on page 11-19.

### Count enable port

Default: cleared

Select this option to create a count enable input port on the block. Only Boolean signals should be connected to this port. The port is labeled **enb**. See also “Enabling or Disabling the Counter” on page 11-20.

### **Count direction port**

Default: cleared

Select this option to create a count direction input port on the block. Only Boolean signals should be connected to this port. The port is labeled dir. See also “Controlling the Counter Direction” on page 11-20.

### **Counter output data is:**

Default: Unsigned

This dropdown menu selects whether the counter output is signed or unsigned.

### **Word length**

Default: 8

**Word length** is a positive integer that defines the size, in bits, of the counter.

Minimum: 1 if **Output data type** is Unsigned, 2 if **Output data type** is Signed

Maximum: 125

### **Fraction length**

Default: 0

To define an integer counter, accept the default **Fraction length** of 0. To define a fixed-point counter, enter the number of bits to the right of the binary point.

Default: 0

### **Sample time**

Default: 1

If the HDL Counter block does not have input ports, the **Sample time** field is enabled, and an explicit sample time must be defined. Enter the desired sample time, or accept the default.

If the HDL Counter block has input ports, this field is disabled, and the block sample time is inherited from the input signals. All input signals must have the same sample time setting. (See also “Control Ports” on page 11-18.)

## HDL FFT

<b>In this section...</b>
“Overview” on page 11-28
“Block Inputs and Outputs” on page 11-28
“HDL Implementation and Implementation Parameters” on page 11-31
“Parameters and Dialog Box” on page 11-31

### Overview

The HDL FFT block implements a minimum resource FFT architecture.

In the current release, the HDL FFT block supports the Radix-2 with decimation-in-time (DIT) algorithm for FFT computation. See the FFT block reference section in the DSP System Toolbox documentation for more information about this algorithm.

The results returned by the HDL FFT block are bit-for-bit compatible with results returned by the DSP System Toolbox FFT block.

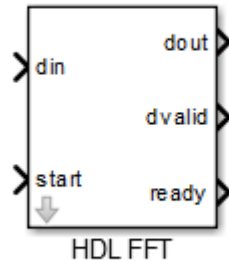
The operation of the HDL FFT block differs from the DSP System Toolbox FFT block, due to the requirements of hardware realization. The HDL FFT block:

- Requires serial input
- Generates serial output
- Operates in burst I/O mode

The HDL FFT block provides handshaking signals to support these features (see “Block Inputs and Outputs” on page 11-28).

### Block Inputs and Outputs

As shown in the following figure, the HDL FFT block has two input ports and three output ports. Two of these ports are for data input and output signals. The other ports are for control signals.



The input ports are:

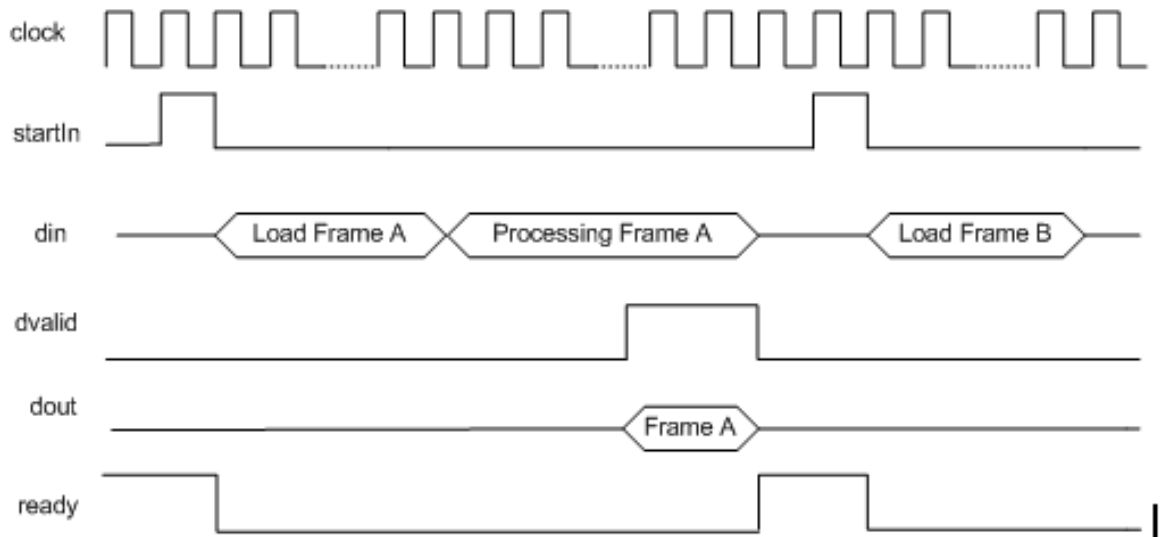
- **din**: The input data signal. A complex signal is required.
- **start**: Boolean control signal. When this signal is asserted true (1), the HDL FFT block initiates processing of a data frame.

The output ports are:

- **dout**: Data output signal. The Radix-2 with DIT algorithm produces output with linear ordering.
- **dvalid**: Boolean control signal. The HDL FFT block asserts this signal true (1) when a burst of valid output data is available at the **dout** port.
- **ready**: Boolean control signal. The HDL FFT block asserts this signal true (1) to indicate that it is ready to process a new frame.

### Configuring Control Signals

For efficient hardware deployment of the HDL FFT block, the timing of the block's input and output data streams must be considered carefully. The following figure shows the timing relationships between the system clock and the **start**, **ready**, and **dvalid** signals.



When `ready` is asserted, the start signal (active high) triggers the FFT block. The high cycle period of the `start` signal does not affect the behavior of the block.

One clock cycle after the start trigger, the block begins to load data and the `ready` signal is deasserted. During the interval when the block is loading, processing, and outputting data, `ready` is low and the start signal is ignored.

The `dvalid` signal is asserted high for  $N$  clock cycles (where  $N$  is the FFT length) after processing is complete. `ready` is asserted again after the  $N$ -point FFT outputs are sent out.

The expression `Tcycle` denotes the total number of clock cycles required by the HDL FFT block to complete an FFT of length  $N$ . `Tcycle` is defined as follows:

- Where  $N > 8$

$$Tcycle = 3N/2 - 2 + \log_2(N) * (N/2 + 3);$$

- Where  $N = 8$

```
Tcycle = 3N/2-1 +log2(N)*(N/2+3);
```

Given `Tcycle`, you can then define the period between assertions of the HDL FFT start signal in a way that is suitable to your application. In the “Using the Minimum Resource HDL FFT” example, this period is computed and assigned to the variable `startLen`, as follows:

```
if (N<=8)
startLen = (ceil(Tcycle/N)+1)*N;
else
startLen = ceil(Tcycle/N)*N;
end
```

In the example model, `startLen` determines the period of a Pulse Generator that drives the HDL FFT block’s `start` input. These values are computed in the model’s initialization function (`InitFcn`), which is defined in the **Callbacks** pane of the Simulink Model Explorer.

The HDL FFT block asserts and deasserts the `ready` and `dvalid` signals automatically. These signals are routed to the model components that write to and read from the HDL FFT block.

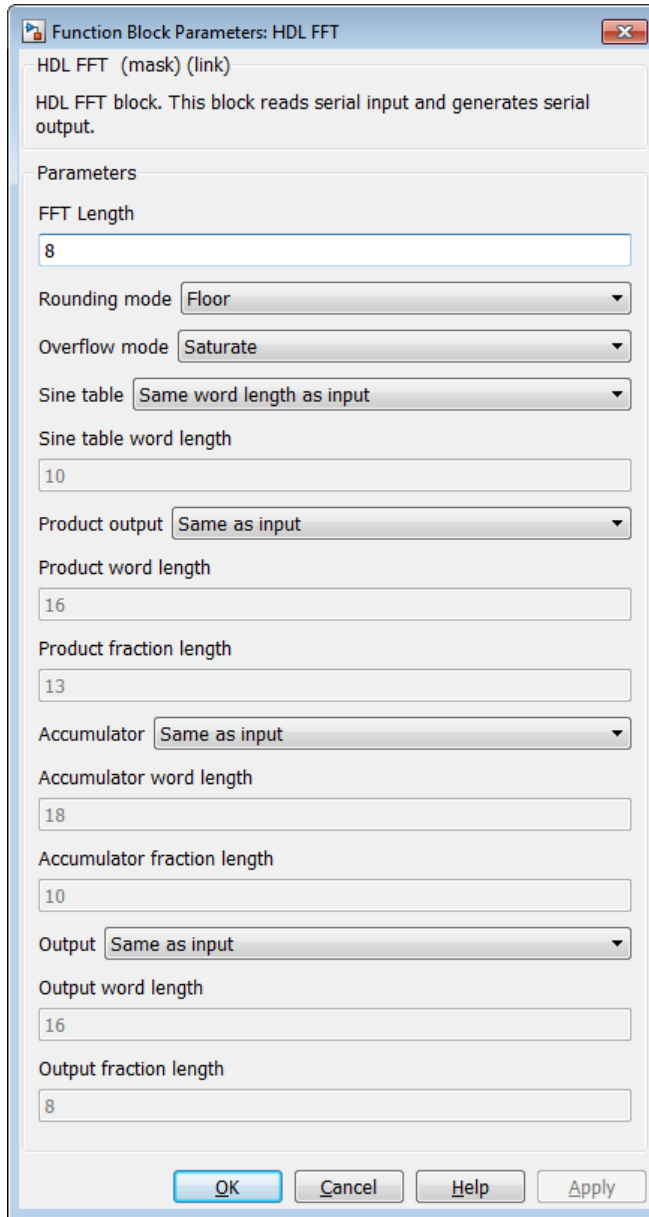
## HDL Implementation and Implementation Parameters

Implementation: default

Implementation Parameters: `InputPipeline`, `OutputPipeline`

## Parameters and Dialog Box

The following figure shows the HDL FFT block dialog box, with parameters at their default settings.





## FFT Length

Default: 8

The FFT length must be a power of 2, in the range  $2^3 .. 2^{16}$ .

## Rounding mode

Default: Floor

The HDL FFT block supports all rounding modes of the DSP System Toolbox FFT block. See also the FFT block reference section in the DSP System Toolbox documentation.

## Overflow mode

Default: Saturate

The HDL FFT block supports all overflow modes of the DSP System Toolbox FFT block. See also the FFT block reference section in the DSP System Toolbox documentation.

## Sine table

Default: Same word length as input

Choose how you specify the word length of the values of the sine table. The fraction length of the sine table values is equal to the word length minus one.

- When you select **Same word length as input**, the word length of the sine table values match that of the input to the block.
- When you select **Specify word length**, you can enter the word length of the sine table values, in bits, in the **Sine table word length** field. The sine table values do not obey the **Rounding mode** and **Overflow mode** parameters; they always saturate and round to Nearest.

## Product output

Default: Same as input

Use this parameter to specify how you want to designate the product output word and fraction lengths:

- When you select `Same as input`, these characteristics match those of the input to the block.
- When you select `Binary point scaling`, you can enter the word length and the fraction length of the product output, in bits, in the **Product word length** and **Product fraction length** fields.

## Accumulator

Default: `Same as input`

Use this parameter to specify how you want to designate the accumulator word and fraction lengths:

When you select `Same as product output`, these characteristics match those of the product output.

- When you select `Same as input`, these characteristics match those of the input to the block.
- When you select `Binary point scaling`, you can enter the word length and the fraction length of the accumulator, in bits, in the **Accumulator word length** and **Accumulator fraction length** fields.

## Output

Default: `Same as input`

Choose how you specify the output word length and fraction length:

- When you select `Same as input`, these characteristics match those of the input to the block.
- When you select `Binary point scaling`, you can enter the word length and the fraction length of the output, in bits, in the **Output word length** and **Output fraction length** fields.

---

**Note** The HDL FFT block skips the divide-by-two operation on butterfly outputs for fixed-point signals.

---

## Signal Processing with the HDL FFT Block

To get started with the HDL FFT block, run the “Using the Minimum Resource HDL FFT” example, which is located in the HDL Coder/Signal Processing example library.

The example illustrates the use of the HDL FFT block in simulation. The model includes buffering and control logic that handles serial input and output. In the example, a complex source signal is stored as a series of samples in a FIFO. Samples from the FIFO are processed serially by the HDL FFT block, which emits a stream of scalar FFT data.

For comparison, the same source signal is also processed by the frame-based DSP System Toolbox FFT block. The output frames from the DSP System Toolbox FFT block are buffered into a FIFO and compared to the output of the HDL FFT block. Examination of the results shows the outputs to be identical.

## HDL FIFO

### In this section...

“Overview” on page 11-37

“Block Inputs and Outputs” on page 11-37

“HDL Implementation and Implementation Parameters” on page 11-38

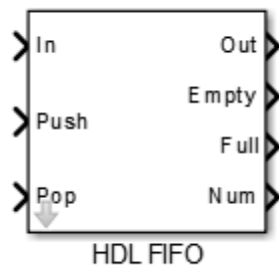
“Parameters and Dialog Box” on page 11-38

### Overview

The HDL FIFO block stores a sequence of input samples in a first in, first out (FIFO) register. The HDL FIFO block closely resembles the Queue block of the DSP System Toolbox, but with HDL-related enhancements such as multirate support.

### Block Inputs and Outputs

The following figure shows the HDL FIFO block with input and output ports enabled.



The input ports are:

- In: The data input signal.
- Push: Control signal. When this port receives a value of 1, the block pushes the input at the In port onto the end of the FIFO register.

- **Pop:** Control signal. When this port receives a value of 1, the block pops the first element off the FIFO register and holds the **Out** port at that value

The output ports are:

- **Out:** The data output signal.
- **Empty:** The block asserts this signal true (1) when the FIFO register is empty. Display of this port is optional.
- **Full:** The block asserts this signal true (1) to indicate that the FIFO register is full. Display of this port is optional.
- **Num:** The current number of data values in the FIFO register. Display of this port is optional.

In the event that two or more of the control input ports are triggered at the same time step, the operations execute in the following order:

**1** Pop

**2** Push

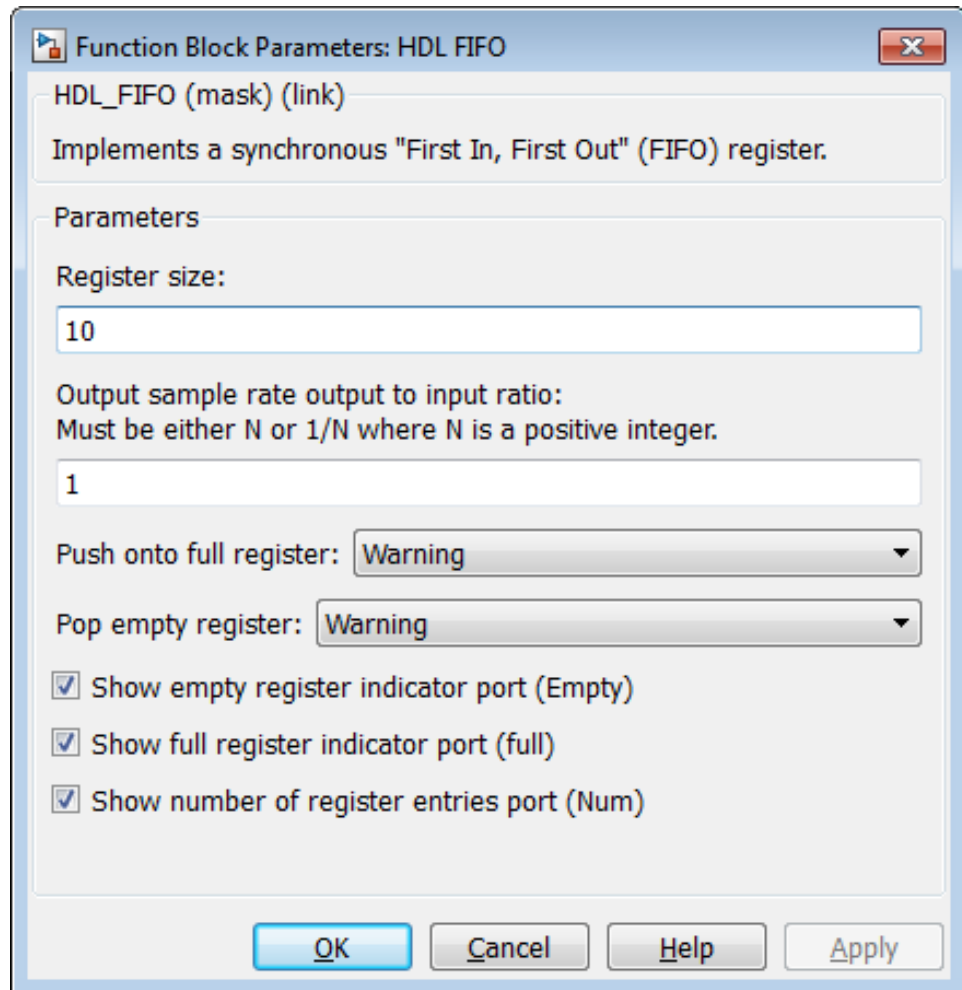
## **HDL Implementation and Implementation Parameters**

Implementation: default

Implementation Parameters: InputPipeline, OutputPipeline

## **Parameters and Dialog Box**

The following figure shows the HDL FIFO block dialog box, with parameters at their default settings.



- **Register size:** Specify the number of entries that the FIFO register can hold.  
Default: 10
- **Output sample rate output to input ratio:** Inputs (In, Push) and outputs (Out, Pop) can run at different sample rates. Enter the required ratio of output to input rates, expressed as N or 1/N, where N is a positive integer.

Default: 1

The Full, Empty, and Num signals run at the faster rate.

- **Push onto full register:** Response (Ignore, Error, or Warning) to a trigger received at the Push port when the register is full.

Default: Warning

- **Pop empty register:** Response (Ignore, Error, or Warning) to a trigger received at the Pop port when the register is empty.

Default: Warning

- **Show empty register indicator port (Empty):** Enable the Empty output port, which is high (1) when the FIFO register is empty, and low (0) otherwise.
- **Show full register indicator port (Full):** Enable the Full output port, which is high (1) when the FIFO register is full, and low (0) otherwise.
- **Show number of register entries port (Num):** Enable the Num output port, which tracks the number of entries currently on the queue.



## HDL Streaming FFT

### In this section...

“Overview” on page 11-41

“HDL Streaming FFT Block Example” on page 11-41

“Block Inputs and Outputs” on page 11-41

“Timing Description” on page 11-42

“HDL Implementation and Implementation Parameters” on page 11-46

“Parameters and Dialog Box” on page 11-46

### Overview

The HDL Streaming FFT block supports the Radix-2 with decimation-in-frequency (DIF) algorithm for FFT computation. See the FFT block reference section in the DSP System Toolbox documentation for more information about this algorithm.

The HDL Streaming FFT block returns results identical to results returned by the Radix-2 DIF algorithm of the DSP System Toolbox FFT block.

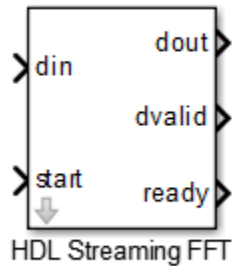
### HDL Streaming FFT Block Example

To get started with the HDL Streaming FFT block, run the “OFDM Receiver with 512-Point Streaming I/O FFT” example, which is in the HDL Coder/Signal Processing example library.

The example implements a simple OFDM transmitter and receiver. The model compares the results obtained from the DSP System Toolbox FFT block to results obtained from the HDL Streaming FFT block.

### Block Inputs and Outputs

As shown in the following figure, the HDL Streaming FFT block has two input ports and three output ports. Two of these ports are for data input and output signals. The other ports are for control signals.



The block has the following input ports:

- **din**: The input data signal. The coder requires a complex fixed-point signal.
- **start**: Boolean control signal. When **start** asserts true (1), the HDL Streaming FFT block initiates processing of a data frame.

The block has the following output ports:

- **dout**: Data output signal.
- **dvalid**: Boolean control signal. The HDL Streaming FFT block asserts this signal true (1) when a stream of valid output data is available at the **dout** port.
- **ready**: Boolean control signal. The HDL Streaming FFT block asserts this signal true (1) to indicate that it is ready to process a new frame.

## Timing Description

The HDL Streaming FFT block operates in one of two modes:

- *Continuous data streaming* mode: In this mode, the HDL Streaming FFT block expects to receive a continuous stream of data at **din**. After an initial delay, the block produces a continuous stream of data at **dout**.
- *Non-continuous data streaming* mode: In this mode, the HDL Streaming FFT block receives non-continuous bursts of streaming data at **din**. After

an initial delay, the block produces non-continuous bursts of streaming data at `dout`.

The behavior of the control signals determines the timing mode of the block.

### **Continuous Data Streaming Timing**

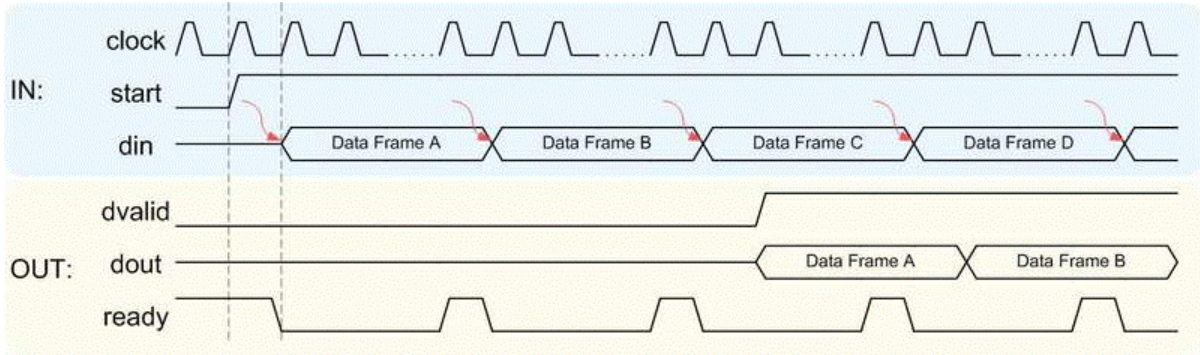
Assertion of the `start` signal (active high) triggers processing by the HDL Streaming FFT block. To initiate continuous data stream processing, assert the `start` signal in one of the following ways:

- Hold the `start` signal high (as shown in Continuous Data Streaming with Start Signal Held High on page 11-44).
- Pulse the `start` signal every `N` clock cycles, where `N` is the FFT length (as shown in Continuous Data Streaming With Pulsed Start Signal on page 11-44).

One clock cycle after the `start` trigger, the block begins to load data at `din`. After the first frame of streaming data, the block starts to receive the next frame of streaming data.

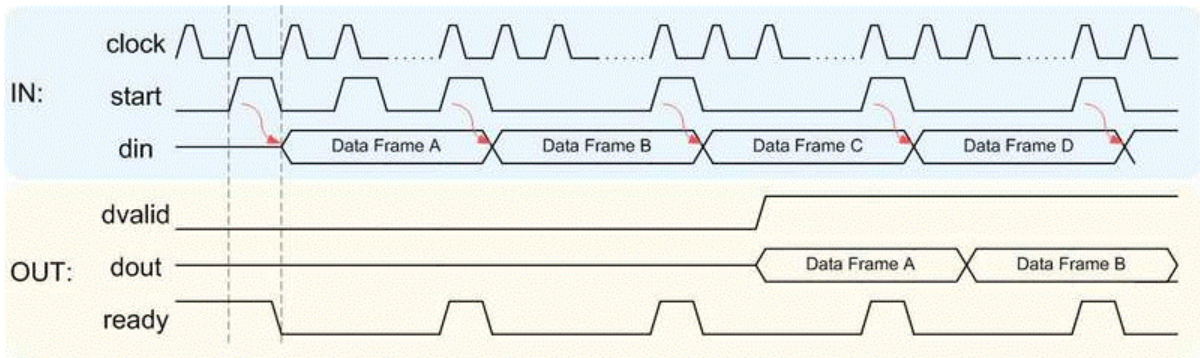
Meanwhile, the block performs the FFT calculation on the incoming data frames and outputs the results continuously at `dout`. The HDL Streaming FFT block asserts and deasserts the `ready` and `dvalid` signals automatically. The block asserts `dvalid` high whenever the output data stream is valid. The block asserts `ready` high to indicate that the block is ready to load a new data frame. When `ready` is low, the block ignores the `start` signal.

The following figures illustrate continuous data streaming. Each data frame corresponds to a stream of `N` input data values, where `N` is the FFT length.



**Continuous Data Streaming with Start Signal Held High**

**Note** The start signal can be a single cycle pulse; it need not be held high for the entire data frame. When processing for a frame begins, further pulses on start do not affect processing of that frame. However, a start pulse must occur at the beginning of each data frame.



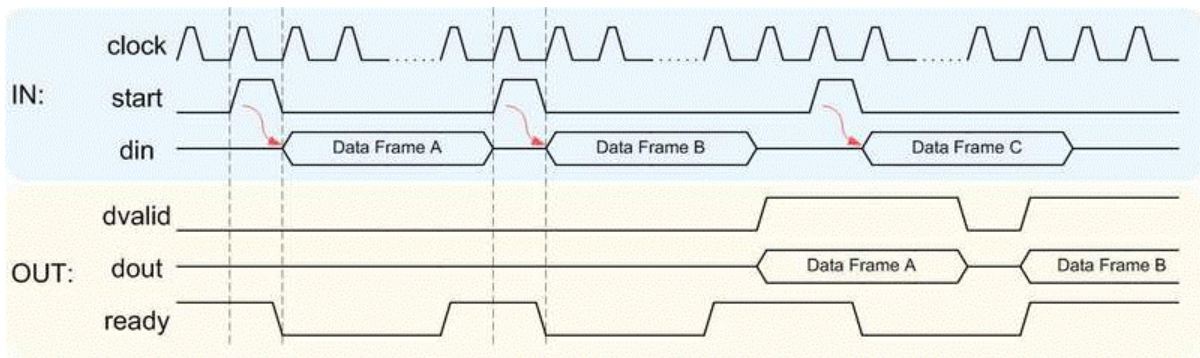
**Continuous Data Streaming With Pulsed Start Signal**

**Non-Continuous Data Streaming Timing**

In this mode, the HDL Streaming FFT block receives continuous bursts of streaming data at din. After an initial delay, the block produces non-continuous bursts of streaming data at dout. Breaks occur between data frames when the following condition exist:

- The start signal does not assert every N clock cycles (where N is the FFT length)
- The start signal is not continuously held high.

Non-continuous data streaming mode allows you more flexibility in determining the intervals between input data streams.

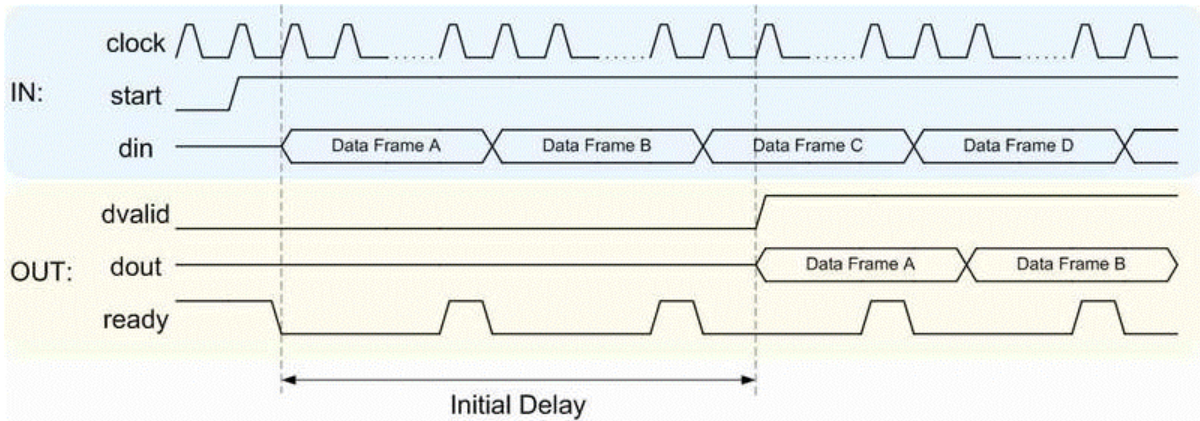


### Initial Delay

The initial delay of the HDL Streaming FFT block is the interval between the following times:

- The time the block begins to receive the first frame of input data
- The time the block asserts `dvalid` and produces the first valid output data.

The initial delay represents the time the block uses to load a data frame, calculate the FFT, and output the beginning of the first output frame. The following figure illustrates the initial delay.



If you select the block option **Display computed initial delay on mask**, the block icon displays the initial delay. The display represents the delay time as  $Z^{-n}$ , where  $n$  is the delay time in samples.

## HDL Implementation and Implementation Parameters

Implementation: default

Implementation Parameters: InputPipeline, OutputPipeline

## Parameters and Dialog Box

The following figure shows the HDL Streaming FFT block dialog box, with parameters at their default settings.

Function Block Parameters: HDL Streaming FFT

HDL Streaming FFT (mask) (link)

HDL Streaming FFT block. This block reads serial input and generates serial output.

Parameters

FFT Length  
1024

Rounding mode Floor

Overflow mode Wrap

Sine table Same word length as input

Sine table word length  
16

Product output Same as input

Product word length  
32

Product fraction length  
23

Accumulator Same as input

Accumulator word length  
32

Accumulator fraction length  
23

Output Same as input

Output word length  
16

Output fraction length  
8

Output in bit-reversed order

Display computed initial delay on mask

OK Cancel Help Apply

### **FFT Length**

Default: 1024

The FFT length must be a power of 2, in the range  $2^3$  to  $2^{16}$ .

### **Rounding mode**

Default: Floor

The HDL Streaming FFT block supports all rounding modes of the DSP System Toolbox FFT block. See also the FFT block reference section in the DSP System Toolbox documentation.

### **Overflow mode**

Default: Wrap

The HDL Streaming FFT block supports all overflow modes of the DSP System Toolbox FFT block. See also the FFT block reference section in the DSP System Toolbox documentation.

### **Sine table**

Default: Same word length as input

Choose how you specify the word length of the values of the sine table. The fraction length of the sine table values is equal to the word length minus one.

- When you select **Same word length as input**, the word lengths of the sine table values match the word lengths of the block inputs.
- When you select **Specify word length**, you can enter the word length of the sine table values, in bits, in the **Sine table word length** field. The sine table values do not obey the **Rounding mode** and **Overflow mode** parameters. They always saturate and round to Nearest.

### **Product output**

Default: Same as input



Use this parameter to specify how you want to designate the product output word and fraction lengths:

- When you select **Same as input**, these characteristics match the characteristics of the input to the block.
- **Binary point scaling**: Enter the word length and the fraction length of the product output, in bits, in the **Product word length** and **Product fraction length** fields.

### Accumulator

Default: **Same as input**

Use this parameter to specify how you want to designate the accumulator word and fraction lengths:

When you select **Same as product output**, these characteristics match the characteristics of the product output.

- When you select **Same as input**, these characteristics match the characteristics of the input to the block.
- **Binary point scaling**: Enter the word length and the fraction length of the accumulator, in bits, in the **Accumulator word length** and **Accumulator fraction length** fields.

### Output

Default: **Same as input**

Choose how you specify the output word length and fraction length:

- **Same as input**: these characteristics match the characteristics of the input to the block.
- **Binary point scaling**: lets you enter the word length and fraction length of the output, in bits, in the **Output word length** and **Output fraction length** fields.

### Output in bit-reversed order

Default: Off

- On: The output data stream is in bit-reversed order.
- Off: The output data stream is in natural order.

For more information about the effects of bit reversal, see “Linear and Bit-Reversed Output Order” in the DSP System Toolbox documentation.

### **Display computed initial delay on mask**

Default: Off

- On: The block icon displays the initial delay as  $Z^{-n}$ , where  $n$  is the delay time in samples.
- Off: The block icon does not display the initial delay.

---

**Note** **Sine table**, **Product output**, **Accumulator**, and **Output** do not support:

- Inherit via internal rule
  - Slope and bias scaling
-

## Bitwise Operators

### In this section...

“Overview of Bitwise Operator Blocks” on page 11-51

“Bit Concat” on page 11-53

“Bit Reduce” on page 11-56

“Bit Rotate” on page 11-58

“Bit Shift” on page 11-60

“Bit Slice” on page 11-62

### Overview of Bitwise Operator Blocks

The Bitwise Operator sublibrary provides commonly used operations on bits and bit fields.

Bitwise Operator blocks support:

- Scalar and vector inputs
- Fixed-point, integer (signed or unsigned), and Boolean data types
- A maximum word size of 128 bits

Bitwise Operator blocks do not currently support:

- Double, single, or complex data types
- Matrix inputs

To open the Bitwise Operators sublibrary, double-click its icon

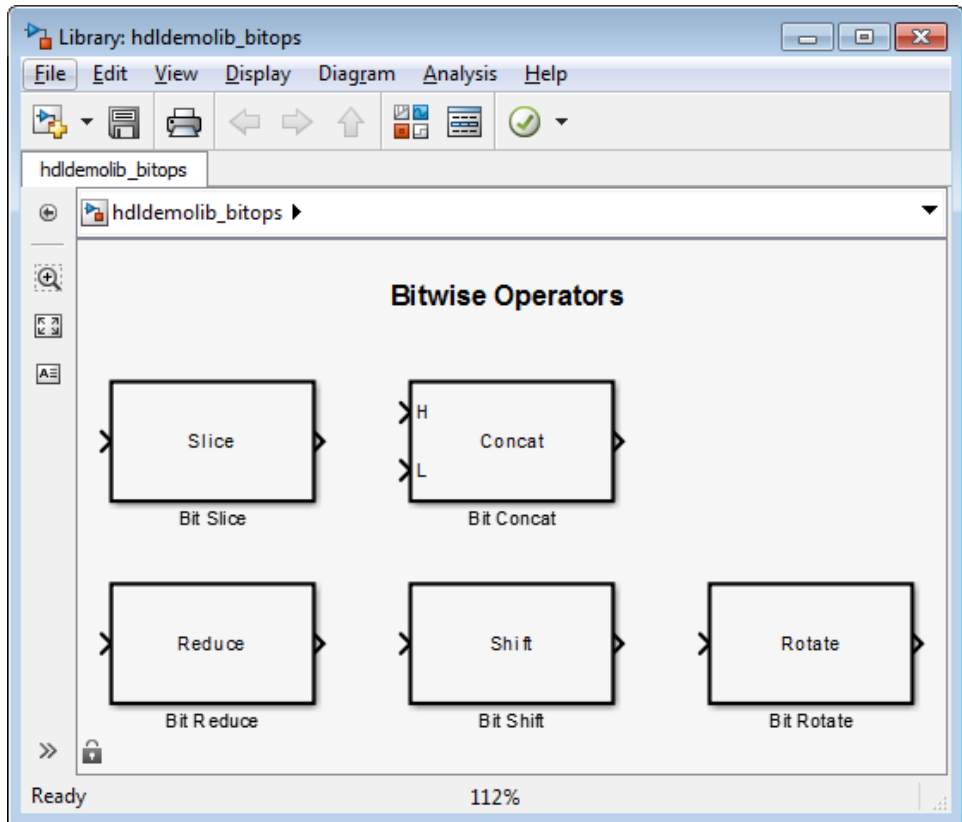


Bitwise Operators

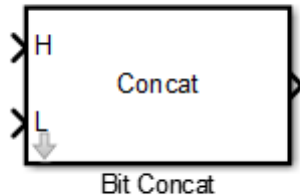
in the `hdl demolib` window. Alternatively, you can open the Bitwise Operators sublibrary directly by typing the following command at the MATLAB prompt:

hdl1demo1ib\_bitops

The following figure shows the Bitwise Operators sublibrary.



## Bit Concat



### Description

The Bit Concat block concatenates up to 128 input words into a single output. The input port labeled L designates the lowest-order input word; the port labeled H designates the highest-order input word. The right-left ordering of words in the output follows the low-high ordering of input signals.

The operation of the block depends on the number and dimensions of the inputs, as follows:

- Single input: The input can be a scalar or a vector. When the input is a vector, the coder concatenates the individual vector elements together.
- Two inputs: Inputs can be any combination of scalar and vector. When one input is scalar and the other is a vector, the coder performs scalar expansion. Each vector element is concatenated with the scalar, and the output has the same dimension as the vector. When both inputs are vectors, they must have the same size.
- Three or more inputs (up to a maximum of 128 inputs): Inputs must be uniformly scalar or vector. All vector inputs must have the same size.

### Data Type Support

- Input: Fixed-point, integer (signed or unsigned), Boolean

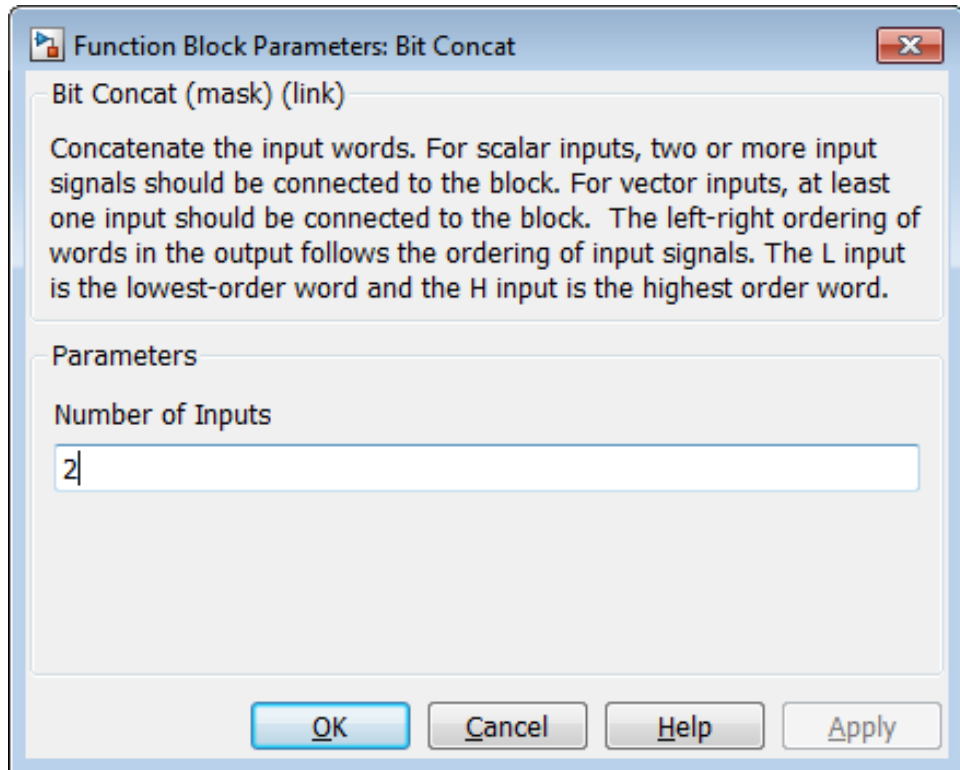
- Output: Unsigned fixed-point or integer (Maximum concatenated output word size: 128 bits)

## HDL Implementation and Implementation Parameters

Implementation: default

Implementation Parameters: InputPipeline, OutputPipeline

## Parameters and Dialog Box



**Number of Inputs:** Enter an integer specifying the number of input signals. The number of input ports displayed on the block updates when **Number of Inputs** changes.

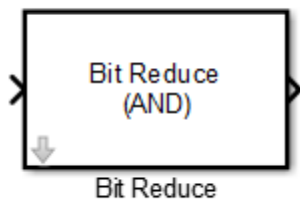
- Default: 2.
- Minimum: 1
- Maximum: 128

---

**Caution** Make sure that the **Number of Inputs** is equal to the number of signals you connect to the block. If unconnected inputs are present on the block, an error will occur at code generation time.

---

## Bit Reduce



### Description

The Bit Reduce block performs a selected bit reduction operation (AND, OR, or XOR) on all the bits of the input signal, reducing it to a single-bit result.

### Data Type Support

- Input: Fixed-point, integer (signed or unsigned), Boolean
- Output: `ufix1`

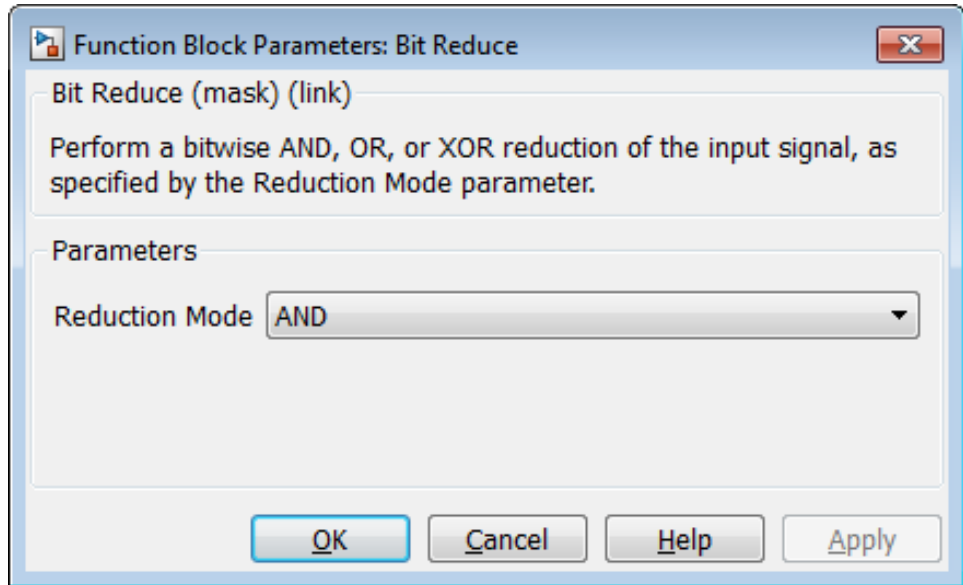
### HDL Implementation and Implementation Parameters

Implementation: `default`

Implementation Parameters: `InputPipeline`, `OutputPipeline`



## Parameters and Dialog Box



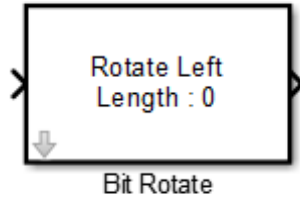
### Reduction Mode

Default: AND

Specifies the reduction operation, as follows:

- AND: Perform a bitwise AND reduction of the input signal.
- OR: Perform a bitwise OR reduction of the input signal.
- XOR: Perform a bitwise XOR reduction of the input signal.

## Bit Rotate



### Description

The Bit Rotate block rotates the input signal left or right by a specified number of bit positions.

### Data Type Support

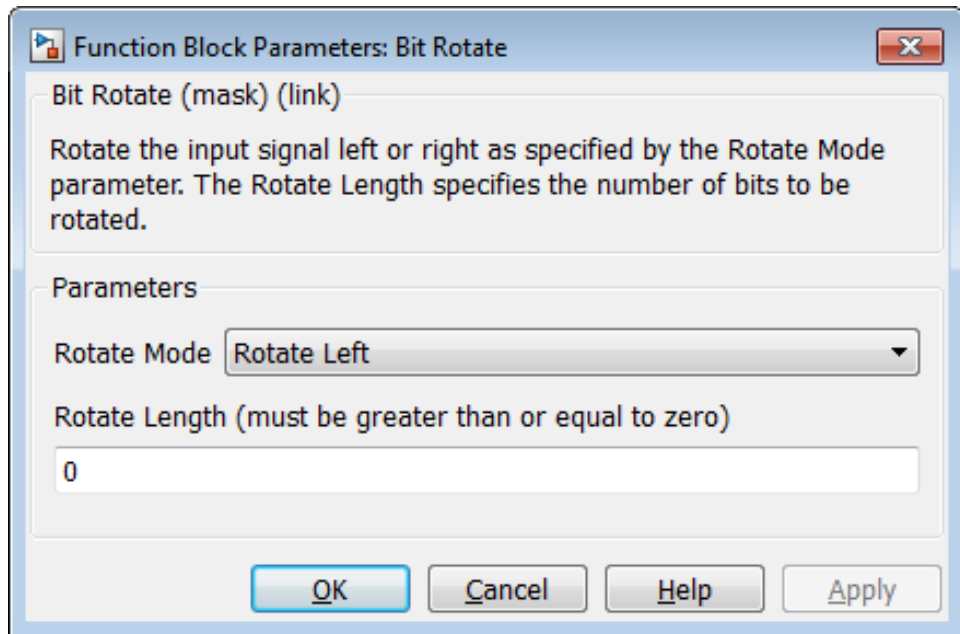
- Input: Fixed-point, integer (signed or unsigned), Boolean
  - Minimum word size: 2 bits
  - Maximum word size: 128 bits
- Output: Has the same data type as the input signal

### HDL Implementation and Implementation Parameters

Implementation: default

Implementation Parameters: InputPipeline, OutputPipeline

## Parameters and Dialog Box



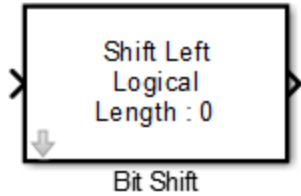
**Rotate Mode:** Specifies direction of rotation, either left or right.

Default: Rotate Left

**Rotate Length:** Specifies the number of bits to be rotated. **Rotate Length** must be greater than or equal to zero.

Default: 0

## Bit Shift



### Description

The Bit Shift block performs a logical or arithmetic shift on the input signal.

### Data Type Support

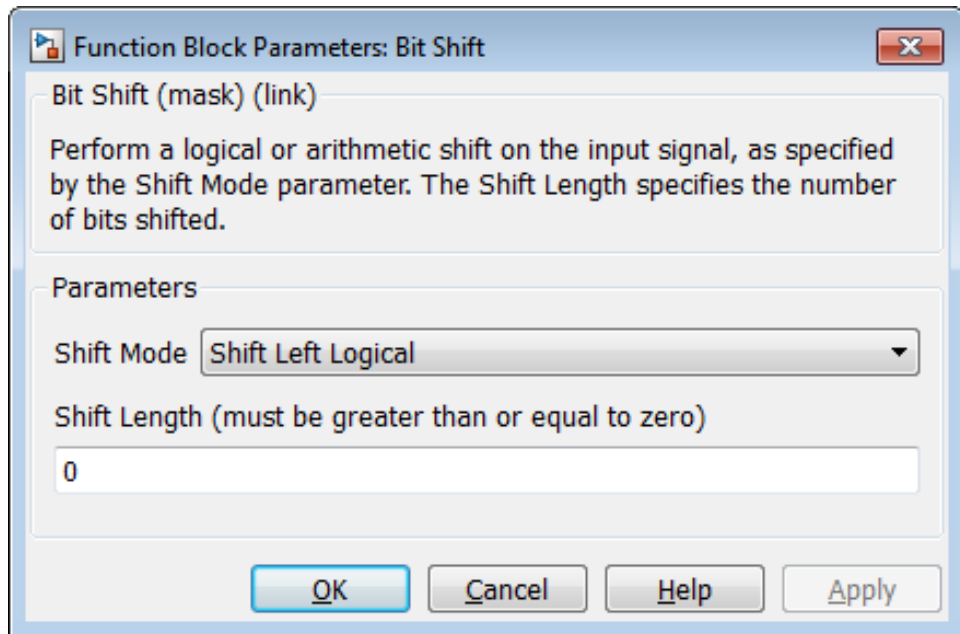
- Input: Fixed-point, integer (signed or unsigned), Boolean
  - Minimum word size: 2 bits
  - Maximum word size: 128 bits
- Output: Has the same data type as the input signal

### HDL Implementation and Implementation Parameters

Implementation: default

Implementation Parameters: InputPipeline, OutputPipeline

## Parameters and Dialog Box



### Shift Mode

Default: Shift Left Logical

Specifies the type and direction of shift, as follows:

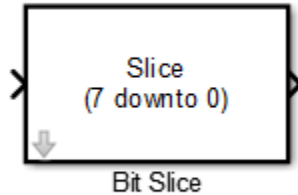
- Shift Left Logical
- Shift Right Logical
- Shift Right Arithmetic

### Shift Length

Default: 0

Specifies the number of bits to be shifted. **Shift Length** must be greater than or equal to zero.

## Bit Slice



### Description

The Bit Slice block returns a field of consecutive bits from the input signal. The lower and upper boundaries of the bit field are specified by zero-based indices entered in the **LSB Position** and **MSB Position** parameters.

### Data Type Support

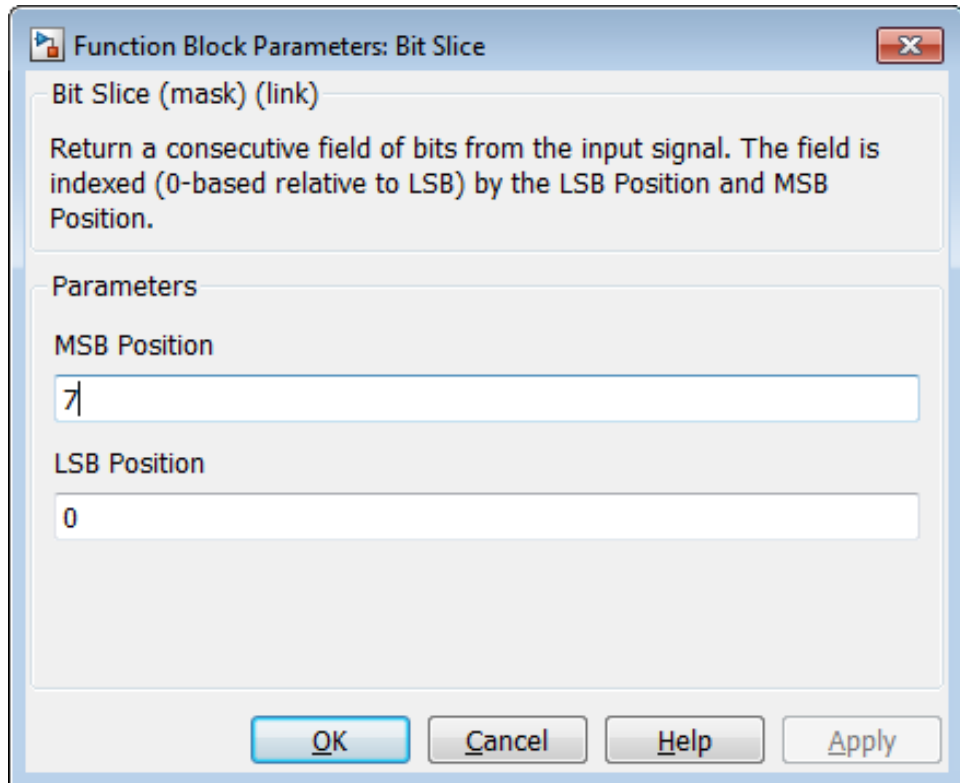
- Input: Fixed-point, integer (signed or unsigned), Boolean
- Output: unsigned fixed-point or unsigned integer

### HDL Implementation and Implementation Parameters

Implementation: default

Implementation Parameters: InputPipeline, OutputPipeline

## Parameters and Dialog Box



### MSB Position

Default: 7

Specifies the bit position (zero-based) of the most significant bit (MSB) of the field to be extracted.

For an input word size *WS*, **LSB Position** and **MSB Position** should satisfy the following constraints:

```
WS > MSB Position >= LSB Position >= 0;
```

The word length of the output is computed as (MSB Position - LSB Position) + 1.

**LSB Position**

Default: 0

Specifies the bit position (zero-based) of the least significant bit (LSB) of the field to be extracted.



# Generating Bit-True Cycle-Accurate Models

---

- “What is a Generated Model?” on page 12-2
- “Numeric Differences in a Speed-Optimized Model” on page 12-4
- “Latency Differences in an Area-Optimized Model” on page 12-8
- “Defaults and Options for Generated Models” on page 12-11
- “Limitations for Generated Models” on page 12-16

## What is a Generated Model?

In some circumstances, significant differences in behavior can arise between a Simulink model and the HDL code generated from that model. Such differences fall into two categories:

- *Numerics*: differences in intermediate and/or final computations. For example, a selected block implementation may restructure arithmetic operations to optimize for speed (see “Numeric Differences in a Speed-Optimized Model” on page 12-4). Where such numeric differences exist, the HDL code is no longer *bit-true* to the model.
- *Latency*: insertion of delays of one or more clock cycles at certain points in the HDL code. Some block implementations that optimize for area can introduce these delays. Where such latency exists, the timing of the HDL code is no longer *cycle-accurate* with respect to the model.

To help you evaluate such cases, the coder creates a *generated model* that is bit-true and cycle-accurate with respect to the generated HDL code. The generated model lets you:

- Run simulations that reflect the behavior of the generated HDL code.
- Create test benches based on the generated model, rather than the original model.
- Visually detect (by color highlighting of affected subsystems) differences between the original and generated models.

The coder creates a generated model as part of the code generation process, and generates test benches based on the generated model, rather than the original model. In cases where no latency or numeric differences occur, you can disregard the generated model except when generating test benches.

The coder also provides options so that you can:

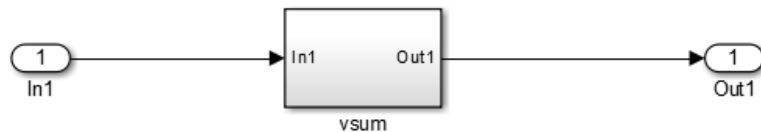
- Specify the color highlighting of differences between the original and generated models.
- Specify a name or prefix for the generated model.

“Defaults and Options for Generated Models” on page 12-11 describes these options.

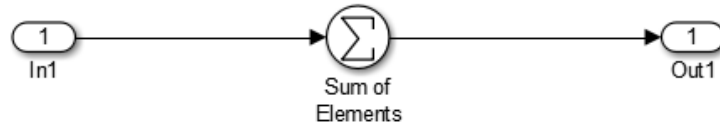
## Numeric Differences in a Speed-Optimized Model

This example first selects a speed-optimized Sum block implementation for simple model that computes a vector sum. It then examines a generated model and locates the numeric changes introduced by the optimization.

The model, `simplevectorsum_tree`, consists of a subsystem, `vsum`, driven by a vector input of width 10, with a scalar output. The following figure shows the root level of the model.



The device under test is the `vsum` subsystem, shown in the following figure. The subsystem contains a Sum block, configured for vector summation.

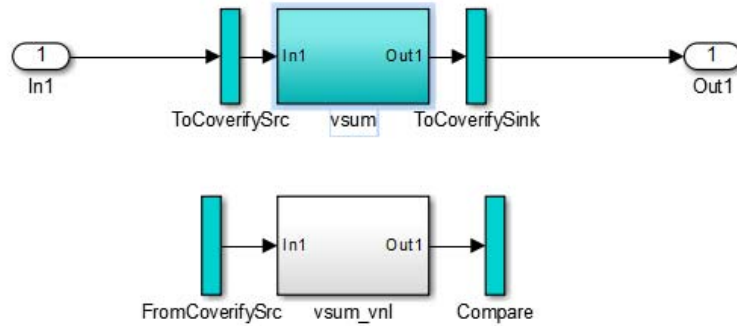


The model is configured to use the **Tree** implementation when generating HDL code for the Sum block within the `vsum` subsystem. This implementation, optimized for minimal latency, generates a tree-shaped structure of adders for the Sum block.

To select a nondefault implementation for an individual block:

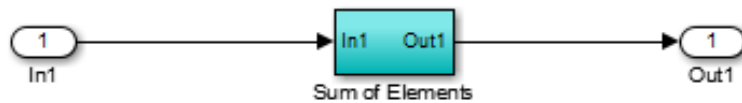
- 1** Right-click the block and select **HDL Code > HDL Block Properties** .
- 2** In the HDL Properties dialog box, select the desired implementation from the **Architecture** menu.
- 3** Click **Apply** and close the dialog box.

After code generation, you can view the validation model, `gm_simplevectorsum_tree_vn1`.

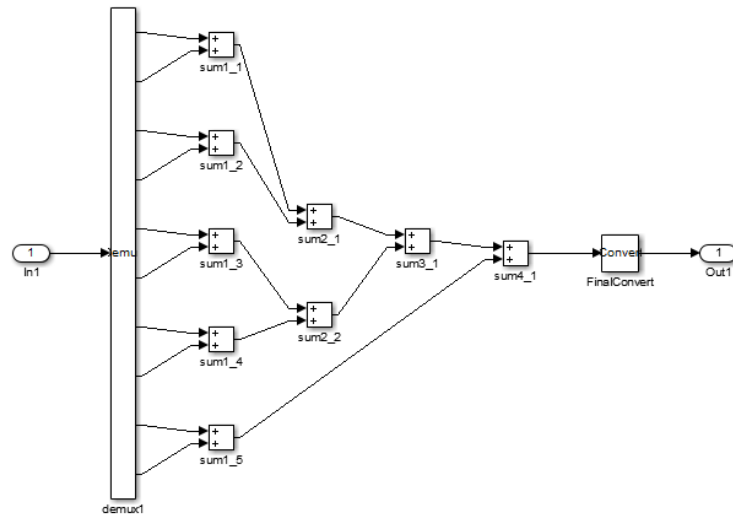


The `vsum` subsystem has been highlighted in cyan. This highlighting indicates that the subsystem differs in some respect from the `vsum` subsystem of the original model.

The following figure shows the `vsum` subsystem in the generated model. Observe that the `Sum` block is now implemented as a subsystem, which also appears highlighted.



The following figure shows the internal structure of the Sum subsystem.

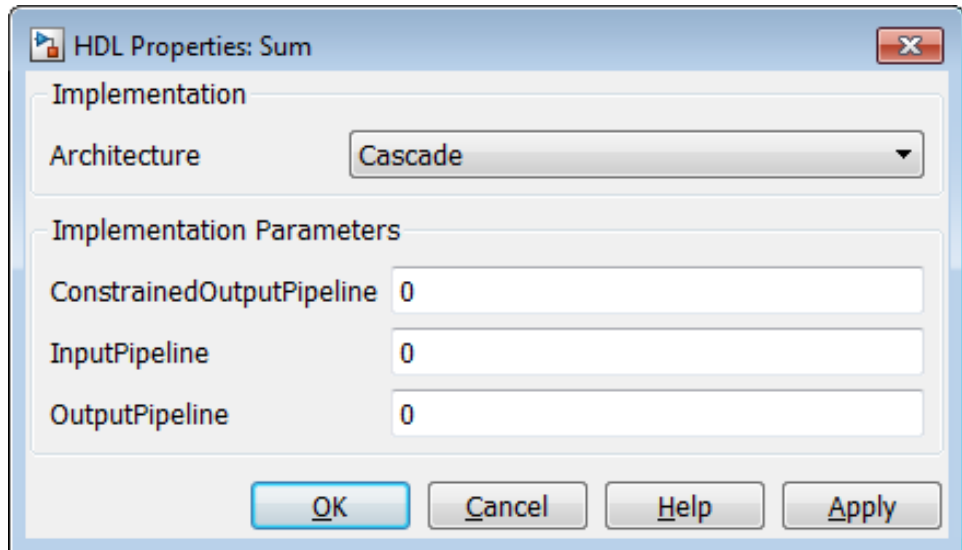


The generated model implements the vector sum as a tree of adders (Sum blocks). The vector input signal is demultiplexed and connected, as five pairs of operands, to the five leftmost adders. The widths of the adder outputs increase from left to right, as required to avoid overflow in computing intermediate results.

## Latency Differences in an Area-Optimized Model

This example uses the `simplevectorsum_cascade` model. This model is identical to the model in (“Numeric Differences in a Speed-Optimized Model” on page 12-4), except that it uses a cascaded implementation for the Sum block. This implementation introduces latency differences.

The following figure shows the HDL Properties dialog box for a Sum block, with the Cascade implementation selected. This implementation generates a cascade of adders for the Sum block.



In the generated code, partial sums are computed by adders arranged in a cascade structure. Each adder computes a partial sum by demultiplexing and adding several inputs in succession. These computation take several clock cycles. On each cycle, an addition is performed; the result is then added to the next input.

To complete computations within one sample period, the system master clock runs faster than the nominal sample rate of the system. A latency of one clock cycle (in the case of this model) is required to transmit the final result to the



output. The inputs cannot change until the computations are complete and the final result is presented at the output.

The generated HDL code runs at two effective rates: a faster rate for internal computations, and a slower rate for input/output. A special timing controller entity (`vsum_tc`) generates these rates from a single master clock using counters and multiple clock enables. The `vsum_tc` entity definition is written to a separate code file.

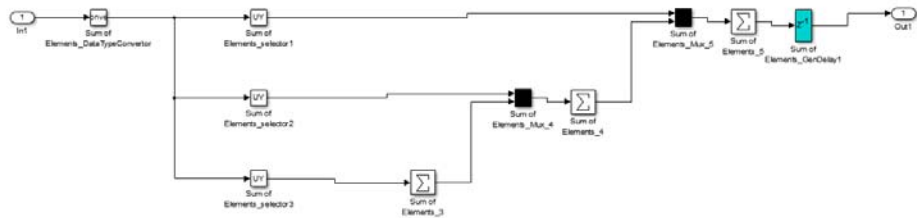
The generated model looks like this:



The subsystem is highlighted in cyan. This highlighting indicates that the subsystem differs in some respect from the `vsum` subsystem of the original model.

The following block diagram shows the `vsum` subsystem in the generated model. The subsystem has been restructured to reflect the structure of the generated HDL code; inputs are grouped and routed to three adders for partial sum computations.

A Unit Delay (highlighted in cyan) has been inserted before the final output. This block delays (in this case, for one sample period) the appearance of the final sum at the output. The delay reflects the latency of the generated HDL code.



---

**Note** The HDL code generated from the example model used in this section is bit-true to the original model.

However, in some cases, cascaded block implementations can produce numeric differences between the original model and the generated HDL code, in addition to the introduction of latency. Numeric differences can arise from saturation and rounding operations.

---

## Defaults and Options for Generated Models

In this section...
“Defaults for Model Generation” on page 12-11
“GUI Options” on page 12-12
“Generated Model Properties for makehdl” on page 12-14

### Defaults for Model Generation

This section summarizes the defaults that the coder uses when building generated models.

#### Model Generation

The coder creates a generated model as part of the code generation process. The coder builds the generated model in memory, before actual generation of HDL code. The HDL code and the generated model are bit-true and cycle-accurate with respect to one another.

---

**Note** The in-memory generated model is not written to a model file unless you explicitly save it.

---

#### Naming of Generated Models

The naming convention for generated models is:

```
prefix_modelName
```

where the default prefix is `gm_`, and the default `modelName` is the name of the original model.

If code is generated more than once from the same original model, and previously generated models exist in memory, an integer is suffixed to the name of each successively generated model. The suffix provides a unique name for each generated model. For example, if the original model is named `test`, generated models will be named `gm_test`, `gm_test0`, `gm_test1`, etc.

---

**Note** When regenerating code from your models, be sure to select the original model for code generation, not a previously generated model. Generating code from a generated model might introduce unintended delays or numeric differences that make the model operate incorrectly.

---

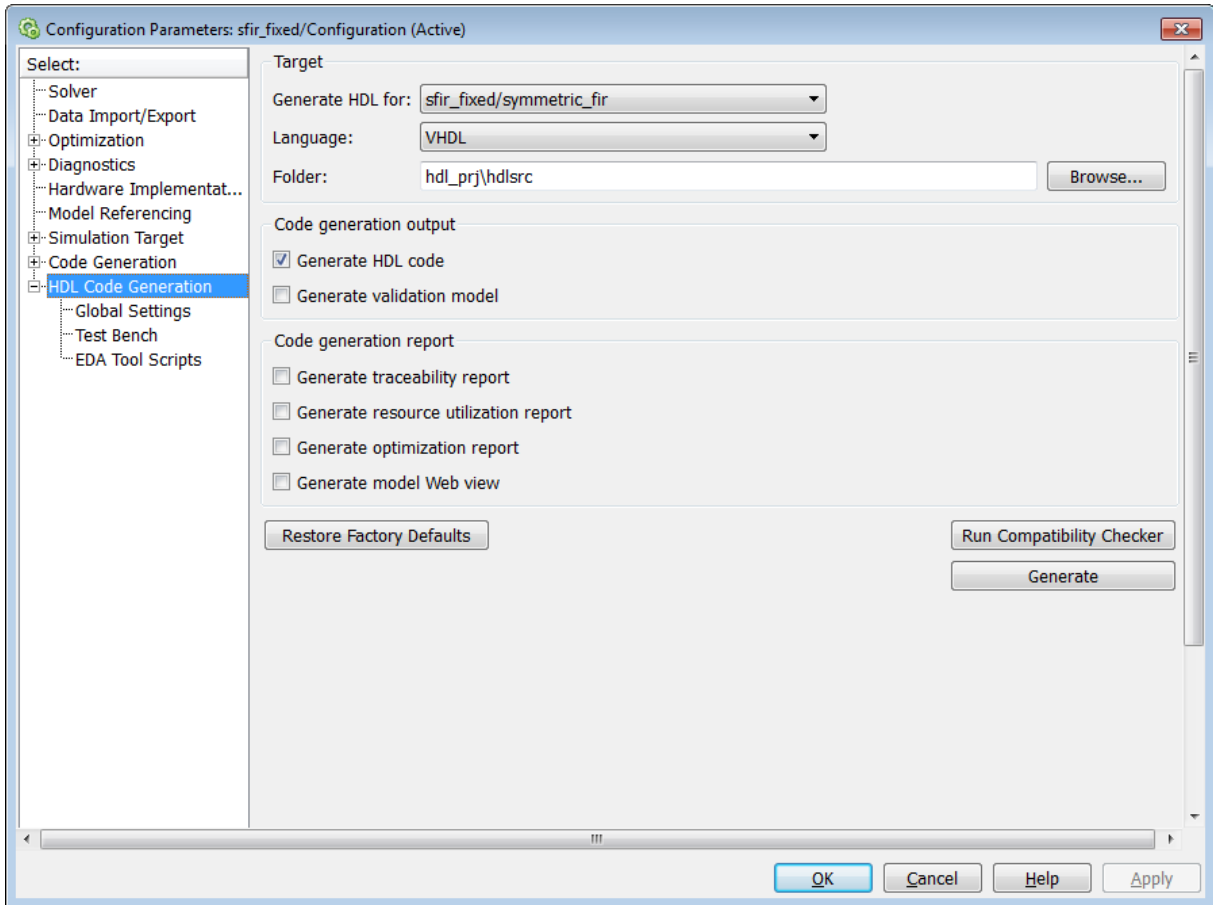
### Block Highlighting

By default, blocks in a generated model that differ from the original model, and their ancestor (parent) blocks in the model hierarchy, are highlighted in the default color, cyan. You can quickly see whether differences have been introduced, by examining the root level of the generated model.

If the original and generated models match, no blocks appear highlighted.

### GUI Options

The HDL Coder GUI provides high-level options controlling the generation and display of generated models. More detailed control is available through the `makehdl` command (see “Generated Model Properties for `makehdl`” on page 12-14). Generated model options are located in the top-level **HDL Code** pane of the Model Configuration Parameters dialog box:



Options include:

- **Generate HDL code:** Generate HDL code for the device under test (DUT). By default, this check box is selected.
- **Generate validation model:** Generate a validation model to verify functional equivalence of the generated model with the original model. By default, this check box is cleared.

## Generated Model Properties for makehdl

The following summary describes makehdl properties that provide detailed controls for the generated model.

Property and Value(s)	Description
'GeneratedmodelNameprefix', ['string']	The default name for the generated model is gm_modelname, where gm_ is the default prefix and modelname is the original model name. To override the default prefix, assign a string value to this property.
'Generatemodelname', ['string']	By default, the original model name is used as the modelname substring of the generated model name. To specify a different model name, assign a string value to this property.
'CodeGenerationOutput', 'string'	Controls the production of generated code and display of the generated model. Values are: <ul style="list-style-type: none"> <li>• <b>GenerateHDLCode:</b> (Default) Generate code, but do not display the generated model.</li> <li>• <b>GenerateHDLCodeAndDisplayGeneratedModel:</b> Create and display generated model, but do not proceed to code generation.</li> <li>• <b>DisplayGeneratedModelOnly:</b> Generate both code and model, and display model when completed.</li> </ul>
'GenerateHDLCode', ['on'   'off']	Controls whether or not to generate HDL code for the DUT. The default is 'on'.
'GenerateValidationModel', ['on'   'off']	Controls whether or not to generate a validation model. The default is 'off'.

<b>Property and Value(s)</b>	<b>Description</b>
'Highlightancestors', ['on'   'off']	By default, blocks in a generated model that differ from the original model, and their ancestor (parent) blocks in the model hierarchy, are highlighted in a color specified by the <code>Highlightcolor</code> property. If you do not want the ancestor blocks to be highlighted, set this property to 'off'.
'Highlightcolor', 'RGBName'	Specify the color used to highlight blocks in a generated model that differ from the original model (default: cyan). Specify the color (RGBName) as one of the following color string values: <ul style="list-style-type: none"><li>• cyan (default)</li><li>• yellow</li><li>• magenta</li><li>• red</li><li>• green</li><li>• blue</li><li>• white</li><li>• black</li></ul>

## Limitations for Generated Models

### In this section...

“Fixed-Point Limitation” on page 12-16

“Double-Precision Limitation” on page 12-16

“Model Properties Not Supported for Generated Models” on page 12-17

### Fixed-Point Limitation

The maximum Simulink fixed-point word size is 128 bits. HDL does not have such a limit. This can lead to cases in which the generated HDL code is not bit-true to the generated model.

When the result of a computation in the generated HDL code has a word size greater than 128 bits:

- The coder issues a warning.
- Computations in the generated model (and the generated HDL test bench) are limited to a result word size of 128 bits.
- This word size limitation does not apply to the generated HDL code, so results returned from the HDL code may not match the HDL test bench or the generated model.

### Double-Precision Limitation

When the binary point in double-precision computations is very large or very small, the scaling can become `inf` or `0`. The limits of precision can be expressed as follows:

```
log2(realmin) ==> -1022
```

```
log2(realmax) ==> 1024
```

Where these limits are exceeded, the binary point is saturated and a warning is issued. If the generated HDL code has binary point scaling greater than  $2^{1024}$ , the generated model has a maximum scaling of  $2^{1024}$ .



Similarly if the generated HDL code has binary point scaling smaller than  $2^{-1022}$ , then the generated model has scaling of  $2^{-1022}$ .

## **Model Properties Not Supported for Generated Models**

The coder disables the following model parameters during code generation, and restores them after code generation completes:

- **Block Reduction** (BlockReductionOpt)
- **Conditional input branch execution** (ConditionallyExecuteInputs)

These properties are disabled in the generated model, even if they are enabled in the source model.



# Optimization

---

- “Streaming” on page 13-2
- “Specify Streaming” on page 13-3
- “Area Reduction with Streaming” on page 13-6
- “What is a Validation Model?” on page 13-17
- “Resource Sharing” on page 13-18
- “Specify Resource Sharing” on page 13-20
- “Check Compatibility for Resource Sharing” on page 13-22
- “Resource Sharing For Area Optimization” on page 13-23
- “Delay Balancing” on page 13-34
- “Balance Delays” on page 13-36
- “Numerical Mismatch Resolution with Delay Balancing” on page 13-37
- “Hierarchy Flattening” on page 13-41
- “Flatten Hierarchy” on page 13-42
- “Loop Optimization” on page 13-44
- “Optimize Loops in the MATLAB Function Block” on page 13-45
- “RAM Mapping” on page 13-47

## Streaming

### What is Streaming?

By default, the coder generates *fully parallel* implementations for vector computations. For example, the coder realizes a vector sum as a number of adders, executing in parallel during a single clock cycle. This technique can consume a large number of hardware resources.

*Streaming* is an optimization in which the coder transforms a vector data path to a scalar data path (or to several smaller-sized vector data paths) that executes at a faster rate. The generated code saves chip area by multiplexing the data over a smaller number of hardware resources. Streaming allows some number of computations to share a hardware resource.

By specifying a *streaming factor* for a subsystem, you can control the degree to which such resources are shared within that subsystem. Higher streaming values imply both a higher degree of sharing, and a higher clock rate. Where the ratio of streaming factor ( $N_{st}$ ) to subsystem data path width ( $V_{dim}$ ) is 1:1, the coder implements an entirely scalar data path. A streaming factor of 0 (the default) produces a fully parallel implementation (i.e., without sharing) for vector computations. Depending on the width of the data path, you can also specify streaming factors between these extrema.

If you know the maximal vector dimensions and the sample rate for a subsystem, you can compute the possible streaming factors and resulting sample rates for the subsystem. However, even if the requested streaming factor is mathematically possible, the subsystem must meet other criteria for streaming. See “How to Specify Streaming” on page 13-3 for details.

You can use the validation model to verify that the output of the optimized DUT is bit-true to the results produced by the original DUT. To learn more about the validation model, see “What is a Validation Model?” on page 13-17.

## Specify Streaming

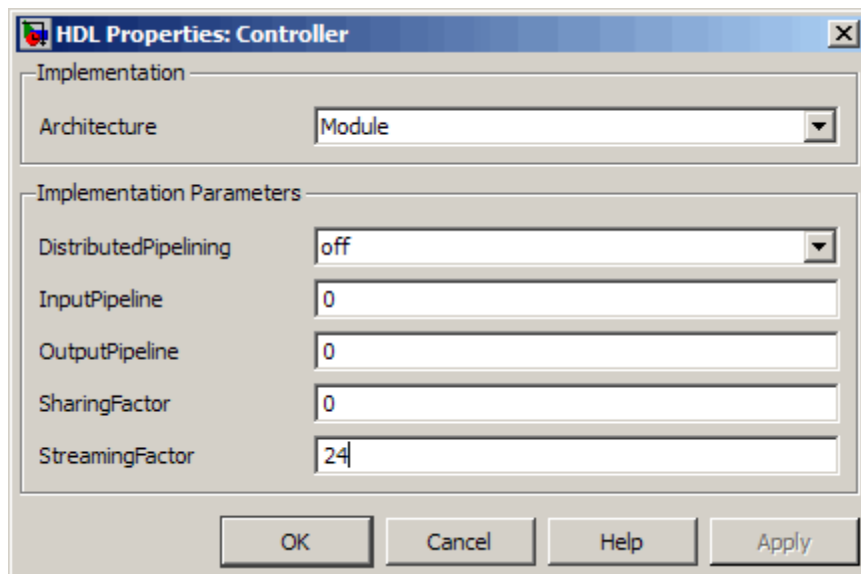
### In this section...

“How to Specify Streaming” on page 13-3

“Requirements and Limitations for Streaming” on page 13-4

### How to Specify Streaming

You apply streaming at the subsystem level. Specify the streaming factor by setting the subsystem HDL parameter `StreamingFactor`. You can set `StreamingFactor` in the HDL Properties dialog for a subsystem, as shown in the following figure.



Alternatively, you can set `StreamingFactor` using the `hdlset_param` function, as in the following example.

```
dut = 'ex_pdcontroller_multi_instance/Controller';  
hdlset_param(dut, 'StreamingFactor', 24);
```

## Requirements and Limitations for Streaming

This section describes the criteria for streaming that subsystems must meet.

### Blocks That Support Streaming

The coder supports a large number of blocks for streaming. As a best practice, run the `checkhdl` function before generating streaming code for a subsystem. `checkhdl` reports blocks in your subsystem that are incompatible with streaming. If you initiate streaming code generation for a subsystem that contains incompatible blocks, the streaming request fails.

### How To Determine Streaming Factor and Sample Time

In a given subsystem, if  $N_{st}$  is the streaming factor, and  $V_{dim}$  is the maximum vector dimension, then the data path of the resultant streamed subsystem can be either of the following:

- Of width  $V_{stream} = (V_{dim}/N_{st})$
- Scalar

If the original subsystem operated with a sample time  $S$ , then the streamed subsystem operates with a sample time of  $S/N_{st}$ .

### Checks and Requirements for Streaming Subsystems

Before applying streaming, the coder performs a series of checks on the subsystems to be streamed. You can stream a subsystem if it meets all the following criteria:

- The streaming factor  $N_{st}$  must be a perfect divisor of the vector width  $V_{dim}$ .
- The subsystem must be a single-rate subsystem that does not contain rate changes or rate transitions.

Because of this requirement, do not specify HDL implementations that are inherently multirate for blocks within the subsystem. For example, using the Cascade implementation (for the Sum, Product, MinMax, and other blocks) is not allowed within a streamed subsystem.

- All vector data paths in the subsystem must have the same widths.
- The subsystem must not contain nested subsystems.

- All blocks within the subsystem must support streaming. The coder supports a large number of blocks for streaming. As a best practice, run `checkhdl` before generating streaming code for a subsystem. `checkhdl` reports blocks in your subsystem that are incompatible with streaming. If you initiate streaming code generation for a subsystem that contains incompatible blocks, the streaming request will fail.

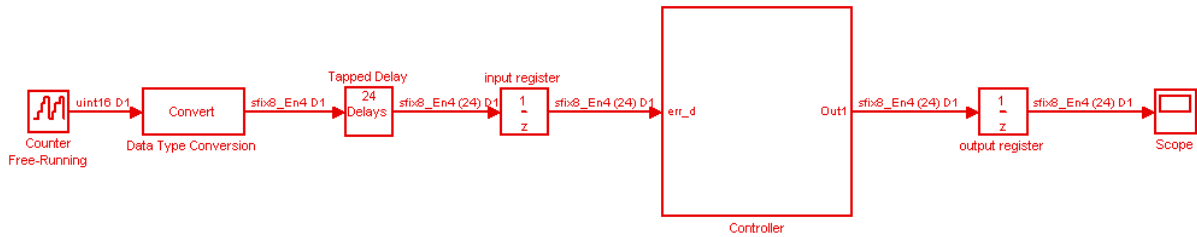
If the requested streaming factor cannot be implemented, the coder generates non-streaming code. It is good practice to generate an Optimization Report. The Streaming and Sharing page of the report provides information about conditions that prevent streaming.

## Area Reduction with Streaming

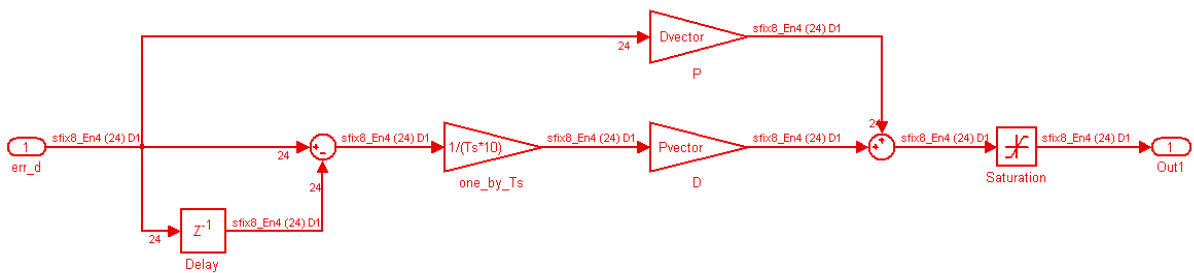
This example illustrates:

- Specification of a streaming factor for a subsystem
- Generation of HDL code and a validation model for the subsystem.

The following example is a single-rate model that drives the Controller subsystem with a vector signal of width 24.



The following figure shows the Controller subsystem, which is the DUT in this example.



By generating HDL code and a report on resource utilization, you can determine how many multipliers, adders/subtractors, registers, RAMs, and multiplexers are generated from this DUT in the default case. To do so, type the following commands:

```
dut = 'ex_pdcontroller_multi_instance/Controller';
hdlset_param(dut, 'StreamingFactor', 0);
```



```
makehdl(dut, 'ResourceReport', 'on');
```

The following figure shows the Resource Utilization Report for the Controller subsystem. The report shows the number of multipliers, adders/subtractors, registers, RAMs, and multiplexers that the coder generates.

## Resource Utilization Report for ex\_pdcontroller\_multi\_instance

### Summary

Multipliers	46
Adders/Subtractors	48
Registers	24
RAMs	0
Multiplexers	24

### Detailed Report

[Expand all] [Collapse all]

---

#### Report for Subsystem: [Controller](#)

##### Multipliers (46)

[+] 8x8-bit Multiply : 46

##### Adders/Subtractors (48)

[+] 32x32-bit Adder : 24

[+] 32x32-bit Subtractor : 24

##### Registers (24)

[+] 8-bit Register : 24

##### Multiplexers (24)

[+] 8-bit 3-to-1 Multiplexer : 24

---

If you choose an optimal `StreamingFactor` for the DUT, you can achieve a drastic reduction in the number of multipliers and adders/subtractors generated. The following commands set `StreamingFactor` to the largest possible value for this subsystem and then generate VHDL code and a Resource Utilization Report.

```
dut = 'ex_pdcontroller_multi_instance/Controller';
hdlset_param(dut, 'StreamingFactor', 24);
makehdl(dut, 'ResourceReport', 'on');
```

During code generation, the coder reports latency in the generated model. It also reports generation of the validation model.

```
### Starting HDL Check.
### HDL Check Complete with 0 errors, 0 warnings and 0 messages.

### The DUT requires an initial pipeline setup latency. Each output port experiences
    these additional delays
### Output port 0: 1 cycles

### Generating new validation model: gm_ex_pdcontroller_multi_instance4_vn1.mdl
### Validation Model Generation Complete.

### Begin VHDL Code Generation
### MESSAGE: The design requires 24 times faster clock with respect to the base rate = 2.
### Working on ex_pdcontroller_multi_instance/Controller/err_d_serializercomp
    as hdlsrc\err_d_serializercomp.vhd
### Working on ex_pdcontroller_multi_instance/Controller/Saturation_out1_serialcomp
    as hdlsrc\Saturation_out1_serialcomp.vhd
### Working on ex_pdcontroller_multi_instance/Controller/kconst_serializercomp
    as hdlsrc\kconst_serializercomp.vhd
### Working on ex_pdcontroller_multi_instance/Controller/kconst_serializercomp1
    as hdlsrc\kconst_serializercomp1.vhd
### Working on Controller_tc as hdlsrc\Controller_tc.vhd
### Working on ex_pdcontroller_multi_instance/Controller as hdlsrc\Controller.vhd
### Generating package file hdlsrc\Controller_pkg.vhd
### Generating HTML files for code generation report in
    C:\hdlsrc\html\ex_pdcontroller_multi_instance directory ...
```

```
### HDL Code Generation Complete.
```

After code generation completes, you can view the results of the `StreamingFactor` optimization. In the Resource Utilization Report, you can see that the coder generates only 2 multipliers and 2 adders for the Controller subsystem.

# Resource Utilization Report for ex\_pdcontroller\_multi\_instance

## Summary

Multipliers	2
Adders/Subtractors	2
Registers	210
RAMs	0
Multiplexers	97

## Detailed Report

[Expand all] [Collapse all]

### Report for Subsystem: [Controller](#)

#### Multipliers (2)

[+] 8x8-bit Multiply : 2

#### Adders/Subtractors (2)

[+] 32x32-bit Adder : 1

[+] 32x32-bit Subtractor : 1

#### Registers (210)

1-bit Register : 3

[+] 8-bit Register : 207

#### Multiplexers (97)

1-bit 2-to-1 Multiplexer : 3

8-bit 2-to-1 Multiplexer : 27

8-bit 45-to-1 Multiplexer : 66

[+] 8-bit 3-to-1 Multiplexer : 1

The coder also produces a Streaming and Sharing report that shows:

- The `StreamingFactor` that you specified
- The other usable `StreamingFactor` values for this subsystem
- Latency (delays) introduced in the generated model
- A hyperlink to the validation model

## Streaming and Sharing Report for ex\_pdcontroller\_multi\_instance

Subsystem	StreamingFactor	SharingFactor
<a href="#">Controller</a>	24	0

### Streaming Report

Subsystem: [Controller](#)

StreamingFactor: 24

Streaming successful with factor 24. Other possible factors: [ 2 3 4 6 8 12 24]

### Sharing Report

No subsystem(s) found with SharingFactor > 0

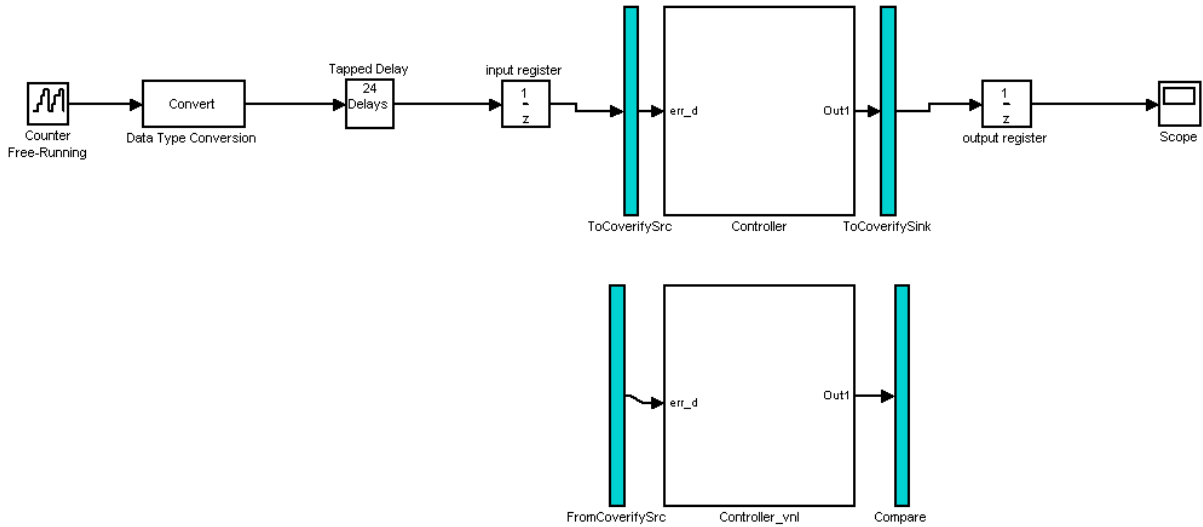
### Path Delay Summary

Port	Path Delay
Controller/ce_out	1
Controller/Out1	1

Validation model: [gm\\_ex\\_pdcontroller\\_multi\\_instance4\\_vnl](#)

## The Validation Model

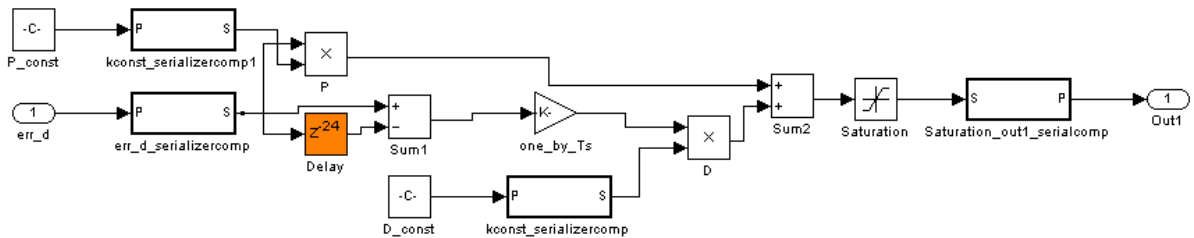
The following figure shows the validation model generated for the Controller subsystem.



The lower section of the validation model contains a copy of the original DUT (Controller\_vnl). This single-rate subsystem runs at its original rate.

The upper section of the validation model contains the streaming version of the DUT (Controller). Internally, this subsystem runs at a different rate than the original DUT.

The following figure shows the interior of the Controller subsystem.

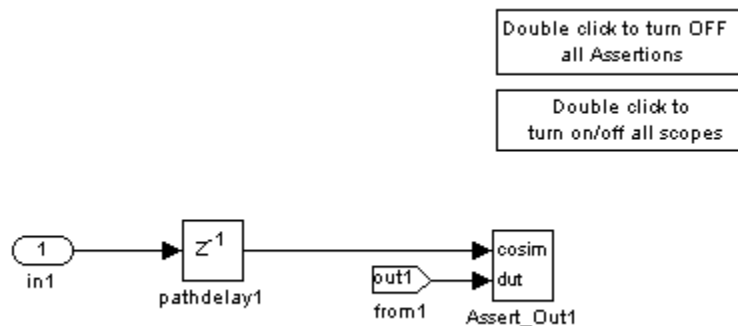


Inspection of the Controller subsystem shows that it is a multirate subsystem, having two rates that operate as follows:



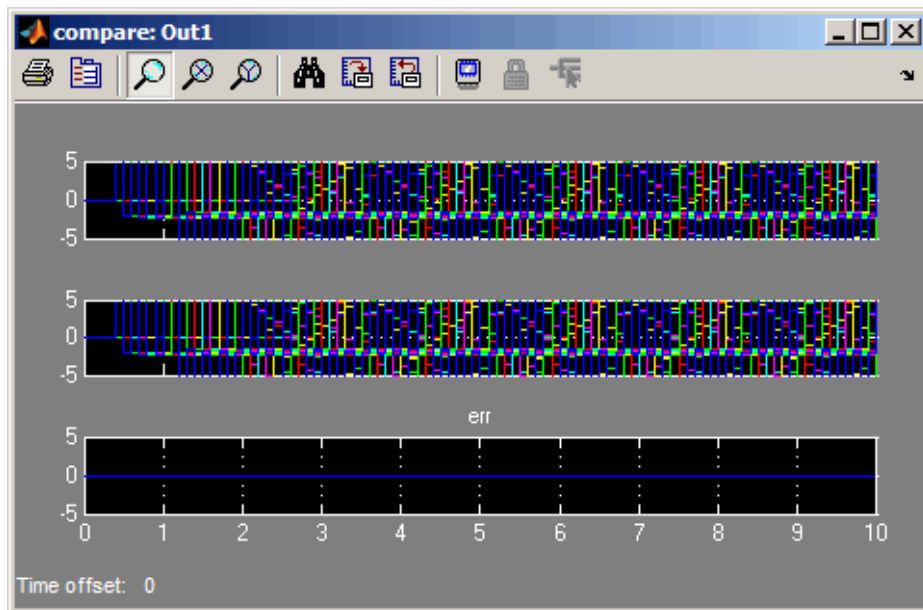
- Inputs and outputs run at the same rate as the exterior model.
- Dual-rate Serializer blocks receive vector data at the original rate and output a stream of scalar values at the higher (24x) rate.
- Interior blocks between Serializers and Deserializer run at the higher rate.
- The Deserializer block receives scalar values at the higher rate and buffers values into a 24-element output vector running at the original rate.

The Compare subsystem (see following figure) receives and compares outputs from the Controller and Controller\_vnl subsystems. To compensate for the latency of the Controller subsystem (reported during code generation), input from the Controller\_vnl subsystem is delayed by one clock cycle. A discrepancy between the outputs of the two subsystems triggers an assertion.



To verify that a generated model with streaming is bit-true to its original counterpart in a validation model:

- 1 Open the Compare subsystem.
- 2 Double click the **Double click to turn on/off all scopes** button.
- 3 Run the validation model.
- 4 Observe the **compare:Out1** scope. The error signal display should show a line through zero, indicating that the data comparisons were equal.



## What is a Validation Model?

Before generating code, the coder creates a behavioral model of the HDL code, called the *generated model*. The generated model uses HDL-specific block implementations, and it implements the area and speed optimizations that you specify.

Because the generated model is often substantially different from the original model, the coder also creates a *validation model* to compare the original model with the generated model. The validation model inserts delays at the outputs of the original model to compensate for latency differences, and compares the outputs of the two models. When you simulate the validation model, numeric differences in the output data trigger an assertion.

A validation model contains:

- A generated model.
- An original model, with compensating delays inserted.
- Original inputs, routed to both the original model and generated model.
- Scopes for comparing and viewing the outputs of the original model and generated model.

## Resource Sharing

### In this section...

“What Is Resource Sharing?” on page 13-18

“Benefits of Resource Sharing” on page 13-19

“Costs of Resource Sharing” on page 13-19

“Resource Sharing Information in Reports” on page 13-19

### What Is Resource Sharing?

*Resource sharing* is an area optimization in which the coder identifies multiple functionally equivalent resources within a subsystem and replaces them with a single resource. The coder time-multiplexes the data over the shared resource to perform the same operations.

The *sharing factor* for a subsystem is the number of blocks that can share a single resource. A higher sharing factor value implies both a higher number of blocks and a higher clock rate.

If you specify a nonzero sharing factor for a subsystem, the coder tries to identify and share that number of functionally equivalent instances of the following types of blocks:

- Gain
- Product
- Atomic Subsystem
- MATLAB Function

You can use the validation model to verify that the output of the optimized DUT is bit-true to the results produced by the original DUT. To learn more about the validation model, see “What is a Validation Model?” on page 13-17.

## Benefits of Resource Sharing

Resource sharing can substantially reduce your chip area. For example, the generated code may use one multiplier to perform the operations of several identically configured multipliers from the original model.

## Costs of Resource Sharing

Resource sharing has the following costs:

- Uses more multiplexers and may use more registers.
- Requires overclocking, which is not feasible if your clock rate is already high.
- Reduces opportunities for distributed pipelining or retiming, because the coder does not pipeline across clock rate boundaries.

## Resource Sharing Information in Reports

If you generate a code generation report, for each subsystem that implements sharing, the report includes the following information:

- Success: Provides a list of resource usage changes caused by sharing.
- Failure: Identifies which criterion was violated.
- Recommendations on other `SharingFactor` values that you could try for the subsystem.
- Latency changes.

## Specify Resource Sharing

### In this section...

“Specify Resource Sharing from the GUI” on page 13-20

“Specify Resource Sharing from the Command Line” on page 13-20

“Requirements for Resource Sharing” on page 13-20

### Specify Resource Sharing from the GUI

To specify resource sharing from the GUI:

- 1 Right-click the subsystem.
- 2 Select **HDL Code > HDL Block Properties**.
- 3 In the **SharingFactor** field, enter the number of shareable resources.

### Specify Resource Sharing from the Command Line

Set the SharingFactor using `hdlset_param`, as in the following example.

```
dut = 'ex_dimcheck/Channel';
hdlset_param(dut, 'SharingFactor', 3);
```

### Requirements for Resource Sharing

On a Subsystem block, you can specify the resource sharing optimization.

Blocks to be shared within a subsystem have the following requirements:

- Single-rate.
- If the block is within a feedback loop, at least one Unit Delay or Delay block connected to each output port.

If you want to share Atomic Subsystem blocks:

- The only state elements that these blocks can contain are Unit Delay and Delay blocks.
- These blocks must not contain enabled or triggered subsystems.

- These blocks must not contain a subsystem that does not meet the requirements for resource sharing.

If you want to share MATLAB Function blocks, they must not use:

- Persistent variables
- Loop streaming
- Output pipelining

### Functionally Equivalent Blocks for Resource Sharing

Block Type	Functionally equivalent if they have...
Product	<ul style="list-style-type: none"> <li>• Equivalent input and output data types</li> <li>• Equivalent rounding and saturation modes</li> </ul>
Gain	<ul style="list-style-type: none"> <li>• Equivalent input and output data types</li> <li>• Equivalent rounding and saturation modes</li> </ul> <p>Gain constants can have different values, but they must have the same data type.</p>
Atomic Subsystem	The same checksum. Atomic subsystems must be identical to be shared.

## Check Compatibility for Resource Sharing

To determine whether or not your model is compatible for resource sharing:

- 1** Before generating code, run `checkhdl` and eliminate general compatibility issues.
- 2** In the Model Configuration Parameters dialog box, on the **HDL Code** pane, select **Generate optimization report**.
- 3** Set the sharing factor for the DUT and generate code.
- 4** After code generation completes, inspect the Optimization Report. The report shows incompatible blocks or other conditions that can cause a resource sharing request to fail.
- 5** If the Optimization Report shows problems, fix them and repeat these steps.

See also “Requirements for Resource Sharing” on page 13-20.



# Resource Sharing For Area Optimization

This example shows how to use the subsystem level sharing optimization in HDL Coder.

## Introduction

Sharing is a subsystem-level optimization supported by HDL Coder for implementing area-efficient hardware.

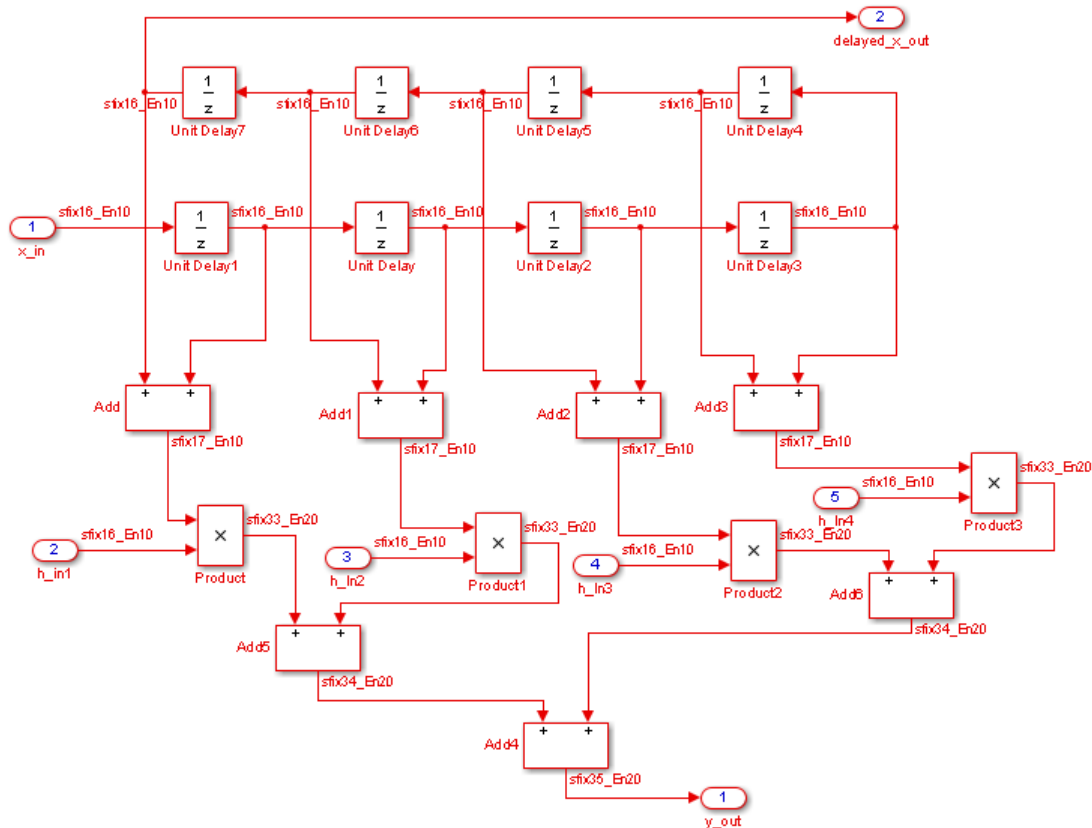
By default, the coder implements hardware that is a 1-to-1 mapping of Simulink blocks to hardware module implementations. The resource sharing optimization enables users to share hardware resources by enabling an N-to-1 mapping of 'N' functionally-equivalent Simulink blocks to a single hardware module. The user specifies 'N' using the 'SharingFactor' implementation parameter.

Consider the following symmetric FIR filter model. It contains 4 product blocks that are functionally equivalent and which map to 4 multipliers in hardware. The Resource Utilization Report lists the hardware resources used.

```
bdclose all;
load_system('sfir_fixed');
open_system('sfir_fixed/symmetric_fir');
hdlset_param('sfir_fixed', 'ResourceReport', 'on');
makehdl('sfir_fixed/symmetric_fir');

### Generating HDL for 'sfir_fixed/symmetric_fir'.
### Starting HDL check.
### HDL check complete with 0 errors, 0 warnings and 0 messages.

### Begin VHDL Code Generation
### Working on sfir_fixed/symmetric_fir as hdlsrc\symmetric_fir.vhd
### Generating HTML files for code generation report in C:\TEMP\R2012bd_614
### HDL code generation complete.
```



### Sharing to Realize an N-to-1 Mapping

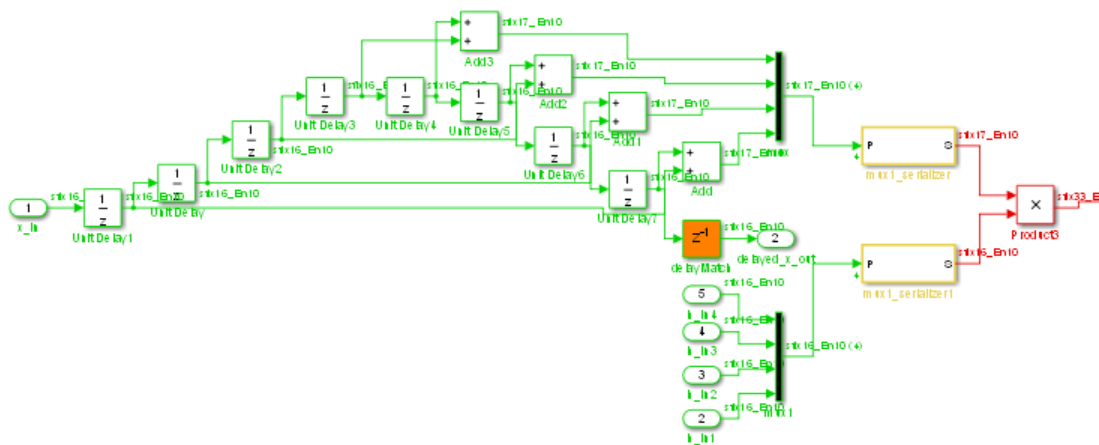
To reduce area resources, you can invoke the sharing optimization by setting the 'SharingFactor' parameter on the subsystem to a positive integer value. This parameter specifies 'N' in the N-to-1 hardware mapping. In this example, there are 4 product blocks, so generating HDL with 'SharingFactor' set to 4 generates HDL with 1 multiplier.

The code generation model reflects the sharing architecture. The inputs to the shared blocks are time-multiplexed over the shared resource at a faster rate (in this case 4x faster, shown in red). The outputs are then routed to the respective consumers at a slower rate (shown in green).

```
hdlset_param('sfir_fixed/symmetric_fir', 'SharingFactor', 4);
makehdl('sfir_fixed/symmetric_fir');
open_system('gm_sfir_fixed/symmetric_fir');
set_param('gm_sfir_fixed', 'SimulationCommand', 'update');
```

```
### Generating HDL for 'sfir_fixed/symmetric_fir'.
### Starting HDL check.
### HDL check complete with 0 errors, 0 warnings and 0 messages.
### The DUT requires an initial pipeline setup latency. Each output port ex
### Output port 0: 1 cycles.
### Output port 1: 1 cycles.
### Generating new validation model: <a href="matlab:open_system('gm_sfir_f
### Validation model generation complete.
```

```
### Begin VHDL Code Generation
### MESSAGE: The design requires 4 times faster clock with respect to the b
### Working on as hdlsrc\mux1_serializer.vhd
### Working on as hdlsrc\mux1_serializer1.vhd
### Working on as hdlsrc\Product30_deserializer.vhd
### Working on symmetric_fir_tc as hdlsrc\symmetric_fir_tc.vhd
### Working on sfir_fixed/symmetric_fir as hdlsrc\symmetric_fir.vhd
### Generating package file hdlsrc\symmetric_fir_pkg.vhd
### Generating HTML files for code generation report in C:\TEMP\R2012bd_614
### HDL code generation complete.
```

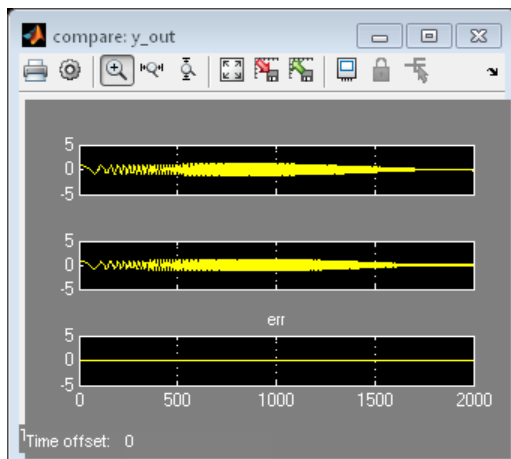


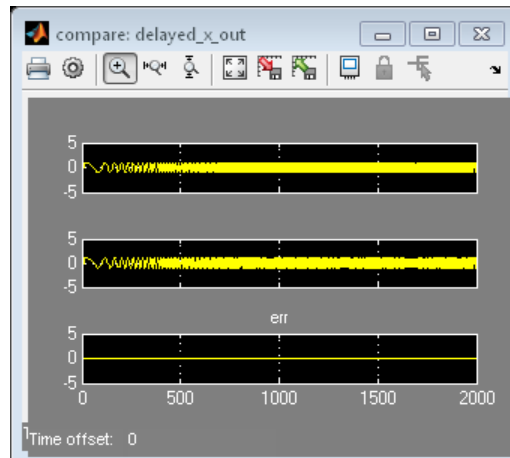
### Delay Balancing and Functional Equivalence

The rate transitions that implement time-multiplexing in the resource sharing architecture introduce additional latency. To maintain functional fidelity, this delay must be balanced across all cut-sets that this path is a member of.

When the resource sharing option is turned on, the coder automatically also turns on the delay balancing option ('BalanceDelays') to automatically balance this additional delay (see the 'Delay Balancing and Validation Model Workflow In Simulink HDL Coder™' example for more details). The coder also automatically turns on the validation model generation option so you can verify that functional equivalence is maintained with respect to the original model.

```
sim('gm_sfir_fixed_vn1');  
set_param('gm_sfir_fixed_vn1/Compare/Assert_y_out/compare: y_out', 'Open',  
set_param('gm_sfir_fixed_vn1/Compare/Assert_delayed_x_out/compare: delayed_
```





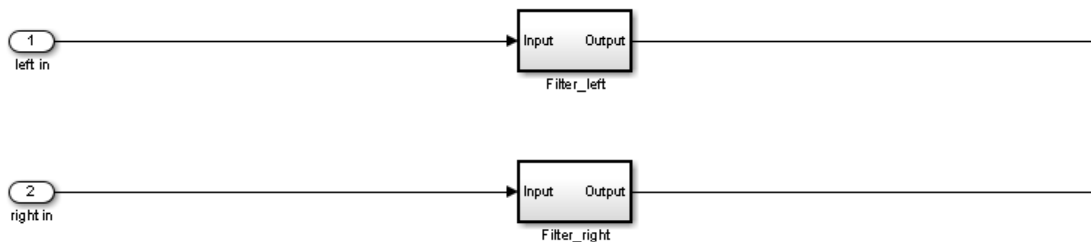
### Block Support, Atomic Subsystems and Extensions

HDL Coder currently supports resource sharing of 4 block types: product blocks, gain blocks, atomic subsystems, and MATLAB Function blocks.

The third block type, atomic subsystems, is useful for expanding the sharing capability beyond this rudimentary support. If two or more atomic subsystems are deemed to be identical, the optimization will share all of them as long as all constraints are satisfied. This means that you can put blocks, and even subgraph regions, into atomic subsystems to enable their sharing.

The following example demonstrates an audio filtering model that applies the same filter on the left and right channels. By default, HDL Coder generates two filter modules in hardware.

```
bdclose all;
load_system('hdlcoder_audiofiltering');
open_system('hdlcoder_audiofiltering/Audio filter');
```



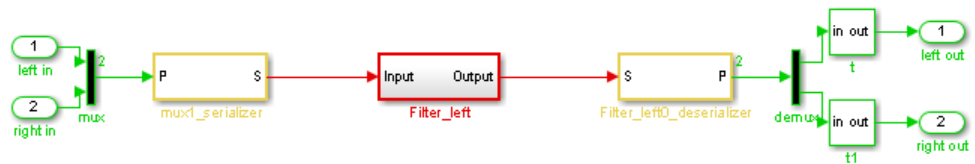
### Sharing Atomic Subsystems

The filters on the two audio channels can be shared by specifying a 'SharingFactor' value of 2 on the encompassing subsystem. This generates an architecture that uses only one filter, as shown below.

```
hdlset_param('hdlcoder_audiofiltering/Audio filter', 'SharingFactor', 2);
makehdl('hdlcoder_audiofiltering/Audio filter');
open_system('gm_hdlcoder_audiofiltering/Audio filter');
set_param('gm_hdlcoder_audiofiltering', 'SimulationCommand', 'update');

### Generating HDL for 'hdlcoder_audiofiltering/Audio filter'.
### Starting HDL check.
### HDL check complete with 0 errors, 0 warnings and 0 messages.
### The DUT requires an initial pipeline setup latency. Each output port ex
### Output port 0: 1 cycles.
### Output port 1: 1 cycles.
### Generating new validation model: <a href="matlab:open_system('gm_hdlcod
### Validation model generation complete.

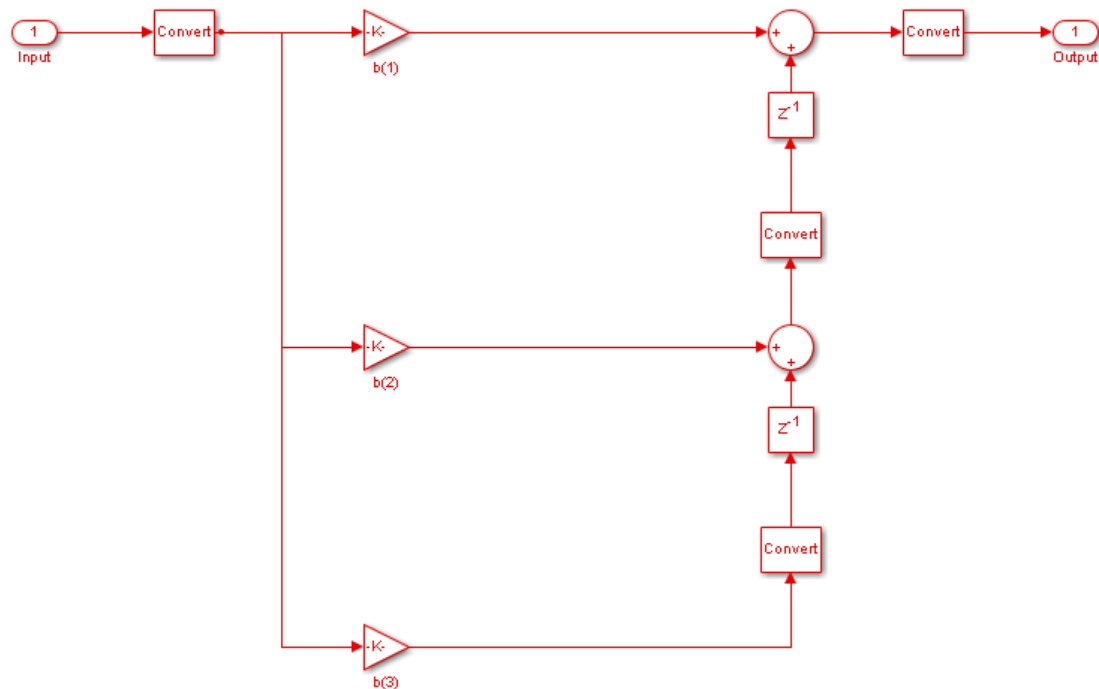
### Begin VHDL Code Generation
### MESSAGE: The design requires 2 times faster clock with respect to the b
### Working on hdlcoder_audiofiltering/Audio filter/Filter_left as hdlsrc\F
### Working on  as hdlsrc\mux1_serializer.vhd
### Working on  as hdlsrc\Filter_left0_deserializer.vhd
### Working on Audio filter_tc as hdlsrc\Audio_filter_tc.vhd
### Working on hdlcoder_audiofiltering/Audio filter as hdlsrc\Audio_filter.
### Generating package file hdlsrc\Audio_filter_pkg.vhd
### HDL code generation complete.
```



### Opportunities Across Hierarchies

Since 'SharingFactor' is a subsystem-level parameter, different subsystems at different levels of the hierarchy can specify different sharing values. In the audio filter example, the filters on each channel use 3 gain blocks respectively.

```
open_system('hdlcoder_audiofiltering/Audio filter/Filter_left');
```



### Sharing at Higher Level of Hierarchy

We can specify a 'SharingFactor' value of 2 at the top-level of the DUT to share the filters on the two channels. Additionally, we can specify a 'SharingFactor' value of 3 on each of the filter subsystems to enable sharing of the 3 gain blocks in each channel. When HDL code is now generated, notice first that the left and right filters have been shared and we have only one filter at the top-level of the hierarchy.

```
hdlset_param('hdlcoder_audiofiltering/Audio filter', 'SharingFactor', 2);
hdlset_param('hdlcoder_audiofiltering/Audio filter/Filter_left', 'SharingFactor', 3);
hdlset_param('hdlcoder_audiofiltering/Audio filter/Filter_right', 'SharingFactor', 3);
makehdl('hdlcoder_audiofiltering/Audio filter');
open_system('gm_hdlcoder_audiofiltering/Audio filter');
set_param('gm_hdlcoder_audiofiltering', 'SimulationCommand', 'update');
```

```
### Generating HDL for 'hdlcoder_audiofiltering/Audio filter'.
### Starting HDL check.
### HDL check complete with 0 errors, 0 warnings and 0 messages.
### The DUT requires an initial pipeline setup latency. Each output port expects 2 cycles.
### Output port 0: 2 cycles.
### Output port 1: 2 cycles.
### Generating new validation model: matlab:open\_system\('gm\_hdlcoder\_audiofiltering/Audio filter'\)
### Validation model generation complete.
```

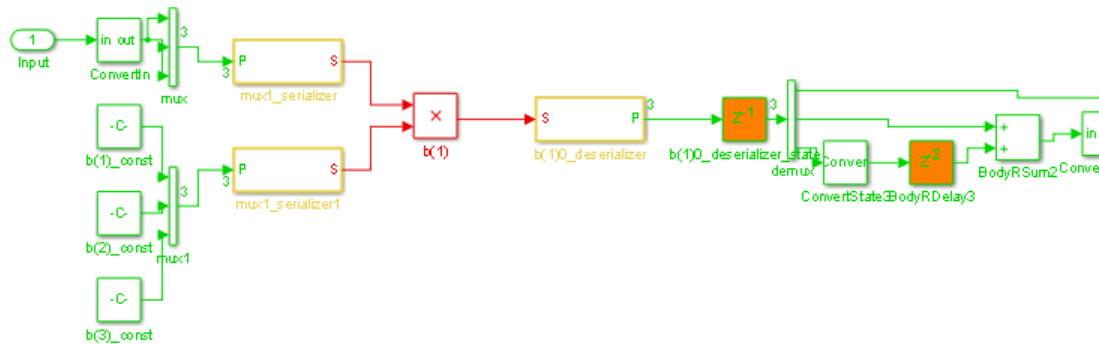
```
### Begin VHDL Code Generation
### MESSAGE: The design requires 6 times faster clock with respect to the block clock.
### Working on as hdlsrc\mux1_serializer.vhd
### Working on as hdlsrc\mux1_serializer1.vhd
### Working on as hdlsrc\b_1_0_deserializer.vhd
### Working on hdlcoder_audiofiltering/Audio filter/Filter_left as hdlsrc\Footer.vhd
### Working on as hdlsrc\mux1_serializer_block.vhd
### Working on as hdlsrc\Footer.vhd
### Working on Audio filter_tc as hdlsrc\Audio_filter_tc.vhd
### Working on hdlcoder_audiofiltering/Audio filter as hdlsrc\Audio_filter.vhd
### Generating package file hdlsrc\Audio_filter_pkg.vhd
### HDL code generation complete.
```

### Sharing at Lower Level of Hierarchy



Additionally, the 3 gain blocks in the lower of the hierarchy (within the filter subsystem) have also been shared. The net result is that we have reduced the resource usage from 6 multipliers to just one.

```
open_system('gm_hdlcoder_audiofiltering/Audio filter/Filter_left');
set_param('gm_hdlcoder_audiofiltering', 'SimulationCommand', 'update');
```

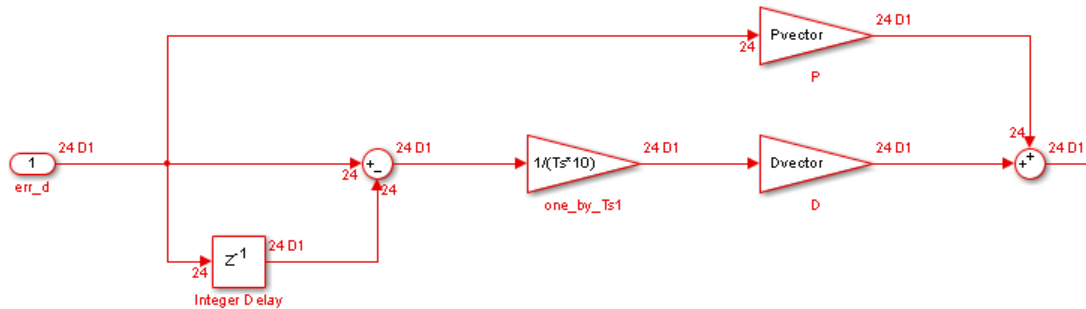


### Combining Optimizations and Sharing

Resource sharing can also be combined with other optimizations like streaming.

Consider the model below: it contains a 24-element vector datapath and 3 vector gain blocks, which will map to 72 multipliers, by default. Streaming can scalarize the vector datapath while sharing can share the 3 gain blocks.

```
bdclose all;
load_system('hdl_areaopt1');
open_system('hdl_areaopt1/Controller');
set_param('hdl_areaopt1', 'SimulationCommand', 'update');
```



### Streaming and Sharing Reduce the Design to Use One Multiplier

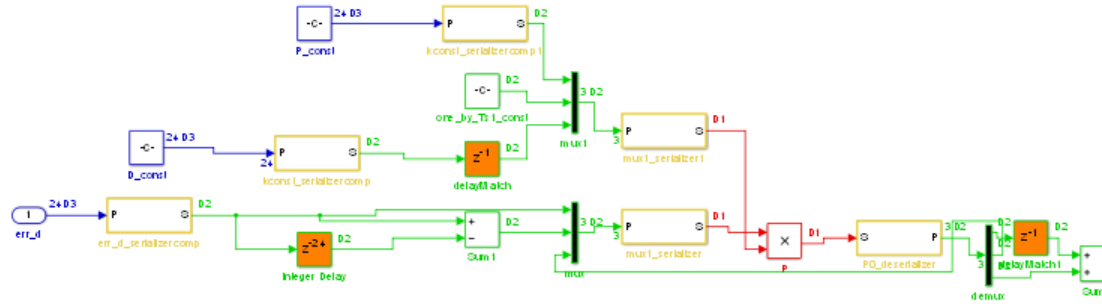
To invoke both optimizations, we set 'StreamingFactor' to 24 and 'SharingFactor' to 3. The former will reduce the number of multipliers from 72 to 3, and the latter reduces the 3 scalar multipliers to 1.

```
hdlset_param('hdl_areaopt1/Controller', 'StreamingFactor', 24);
hdlset_param('hdl_areaopt1/Controller', 'SharingFactor', 3);
makehdl('hdl_areaopt1/Controller');
open_system('gm_hdl_areaopt1/Controller');
set_param('gm_hdl_areaopt1', 'SimulationCommand', 'update');
```

```
### Generating HDL for 'hdl_areaopt1/Controller'.
### Starting HDL check.
### HDL check complete with 0 errors, 0 warnings and 0 messages.
### The DUT requires an initial pipeline setup latency. Each output port ex
### Output port 0: 2 cycles.
### Generating new validation model: <a href="matlab:open_system('gm_hdl_ar
### Validation model generation complete.
```

```
### Begin VHDL Code Generation
### MESSAGE: The design requires 72 times faster clock with respect to the
### Working on as hdlsrc\err_d_serializercomp.vhd
### Working on as hdlsrc\Saturation_out1_serialcomp.vhd
### Working on as hdlsrc\kconst_serializercomp.vhd
### Working on as hdlsrc\mux1_serializer.vhd
### Working on as hdlsrc\PO_deserializer.vhd
### Working on Controller_tc as hdlsrc\Controller_tc.vhd
```

```
### Working on hdl_areaopt1/Controller as hdlsrc/Controller.vhd
### Generating package file hdlsrc/Controller_pkg.vhd
### Generating HTML files for code generation report in C:\TEMP\R2012bd_614
### HDL code generation complete.
```



## Delay Balancing

### In this section...

“Why Use Delay Balancing” on page 13-34

“Delay Balancing Limitations” on page 13-34

### Why Use Delay Balancing

The coder supports several optimizations, block implementations, and options that introduce discrete delays into the model, with the goal of more efficient hardware usage or achieving higher clock rates. Examples include:

- *Optimizations*: Optimizations such as output pipelining, streaming, or resource sharing can introduce delays.
- *Cascading*: Some blocks support cascade implementations, which introduce a cycle of delay in the generated code.
- *Block implementations*: Some block implementations inherently introduce delays in the generated code. “Numerical Mismatch Resolution with Delay Balancing” on page 13-37 discusses one such implementation.

A common problem is that optimizations can introduce delays along the critical path in a model, but equivalent delays are not introduced on other, parallel signal paths. This situation can introduce differences in numerics between the original model and the generated model and HDL code. Manual insertion of compensating delays along the other paths is possible, but is error prone and does not scale well to very large models with many signal paths or multiple sample rates.

To help you solve this problem, the coder supports *delay balancing*. When you enable delay balancing, if the coder detects introduction of new delays along one path, it inserts matching delays on the other paths. When delay balancing is enabled, the generated model is functionally equivalent to the original model.

### Delay Balancing Limitations

The following blocks do not support delay balancing:

- Cosimulation
- Data Type Duplicate
- Decrement To Zero
- Enable Port
- Frame Conversion
- Ground
- HDL FFT
- LMS Filter
- Model Reference
- NCO
- Sine Wave
- To VCD File
- Trigger Port
- Magnitude-Angle to Complex

The following block implementations do not currently support delay balancing:

- `hdldefaults.ConstantSpecialHDL Emission`
- `hdldefaults.NoHDL`

## Balance Delays

Use the following `makehdl` properties to enable delay balancing:

- `BalanceDelays`: To enable delay balancing, set `BalanceDelays` to `'on'`.
- `GenerateValidationModel`: Set `GenerateValidationModel` to `'on'` so that you can view a *validation model* that highlights generated delays and other differences between your original model and the generated model. A validation model is particularly useful for observing the effect of delay balancing. The validation model contains:
  - The delay balanced DUT
  - The original DUT
  - The original inputs to the DUT (for example, test bench), routed to both versions of the DUT
  - Logic for comparison and viewing of the DUT outputs

Using the validation model, you can verify that the output of the optimized DUT is bit-true to the results produced by the original DUT.

For example, the following commands generate HDL code with delay balancing and generate a validation model.

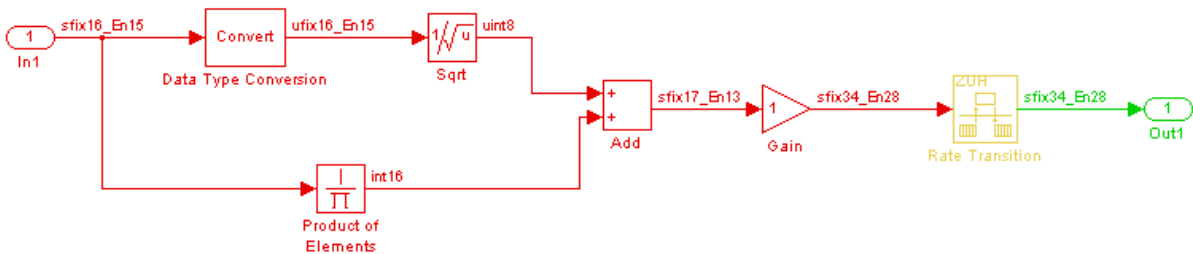
```
dut = 'ex_rsqrtdelaybalancing/Subsystem';  
makehdl(dut, 'BalanceDelays', 'on', 'GenerateValidationModel', 'on');
```

For new models you create, delay balancing is enabled by default but generation of a validation model is disabled by default.

## Numerical Mismatch Resolution with Delay Balancing

This example shows a simple case where the VHDL implementation of a block introduces delays that cause a numerical mismatch between the original DUT and the generated model and HDL code. The example then demonstrates how to use delay balancing to fix the mismatch.

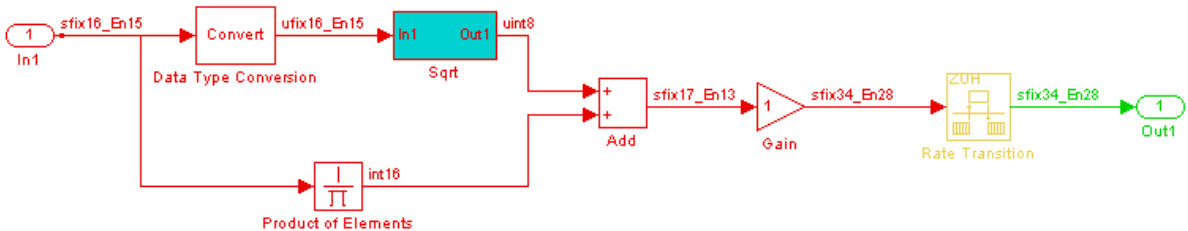
The following figure shows the DUT for the `ex_rsqrtdelaybalancing` model. The DUT is a simple multirate subsystem that includes a Reciprocal Square Root block (`Sqrt`). A Rate Transition block downsamples the output signal to a lower sample rate.



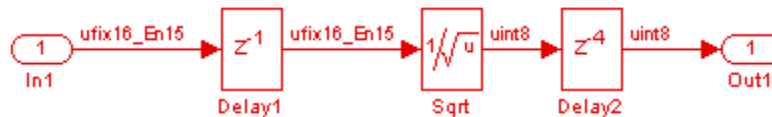
Generate HDL code without delay balancing and generate a validation model:

```
dut = 'ex_rsqrtdelaybalancing/Subsystem';
makehdl(dut, 'BalanceDelays', 'off', 'GenerateValidationModel', 'on');
```

Examination of the generated model shows that the coder has implemented the `Sqrt` block as a subsystem:



The following figure shows that the generated Sqrt subsystem introduces a total of 5 cycles of delay. (This behavior is inherent to the Reciprocal Square Root block implementation.) These delays map to registers in the generated HDL code when **UseRAM** is off.

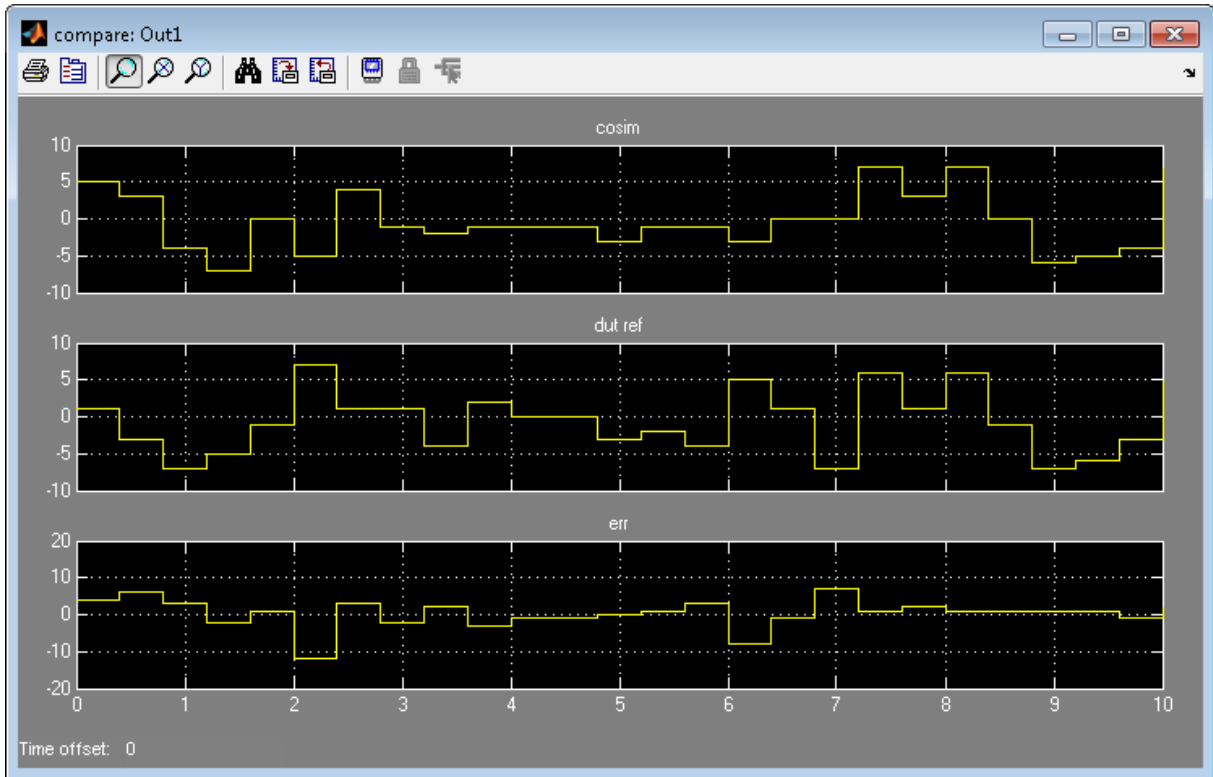


The scope in the following figure shows the results of a comparison run between the original and generated models. The scope displays the following signals, in descending order:

- The outputs from the original model
- The outputs from the generated model
- The difference between the two

The difference is nonzero, indicating a numerical mismatch between the original and generated models.





Two factors cause this discrepancy:

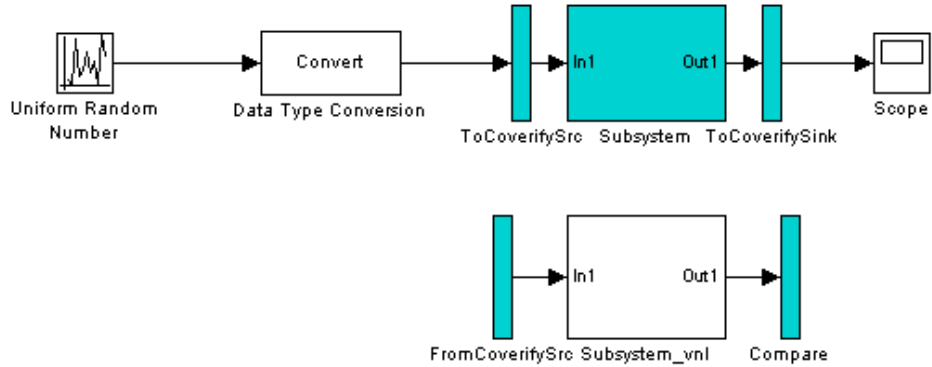
- The input signal branches into two parallel paths (to the `Sqrt` and product blocks) but only the branch to the `Sqrt` block introduces delays.
- The downsampling caused by the rate transition drops samples.

You can solve these problems by manually inserting delays in the generated model. However, using the coder's delay balancing capability produces more consistent results.

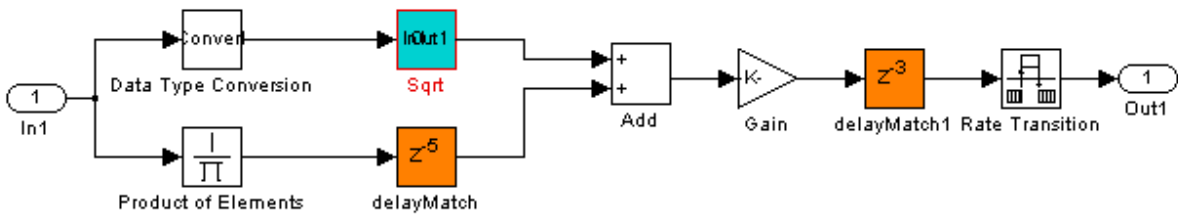
Generate HDL code with delay balancing and generate a validation model:

```
dut = 'ex_rsqrtdelaybalancing/Subsystem';
makehdl(dut, 'BalanceDelays', 'on', 'GenerateValidationModel', 'on');
```

The following figure shows the validation model. The lower subsystem is identical to the original DUT. The upper subsystem represents the HDL implementation of the DUT.



The upper subsystem (shown in the following figure) represents the HDL implementation of the DUT. To balance the 5-cycle delay from the Sqrt subsystem, the coder has inserted a 5-cycle delay on the parallel data path. The coder has also inserted a 3-cycle delay before the Rate Transition to offset the effect of downsampling.



# Hierarchy Flattening

**In this section...**

“What Is Hierarchy Flattening?” on page 13-41

“When To Flatten Hierarchy” on page 13-41

“When Not To Flatten Hierarchy” on page 13-41

## What Is Hierarchy Flattening?

Hierarchy flattening enables you to remove subsystem hierarchy from the HDL code generated from your design.

The coder considers blocks within a flattened subsystem to be at the same level of hierarchy, and no longer grouped into separate subsystems. This consideration allows the coder to reorganize blocks for optimization across the original hierarchical boundaries, while preserving functionality.

## When To Flatten Hierarchy

Flatten hierarchy to:

- Enable more extensive area and speed optimization.
- Reduce the number of HDL output files. For every subsystem flattened, the coder generates one less HDL output file.

## When Not To Flatten Hierarchy

Avoid flattening hierarchy if you want to preserve one-to-one mapping from subsystem name to HDL module or entity name. Not flattening hierarchy makes the HDL code more readable.

## Flatten Hierarchy

### In this section...

“Prerequisites For Hierarchy Flattening” on page 13-42

“How To Flatten Hierarchy” on page 13-42

“Options For Hierarchy Flattening” on page 13-43

“Limitations For Hierarchy Flattening” on page 13-43

### Prerequisites For Hierarchy Flattening

To flatten hierarchy, a subsystem must have the following block properties.

Property	Required value
DistributedPipelining	'off'
StreamingFactor	0
SharingFactor	0

To flatten hierarchy, you must also have the `MaskParameterAsGeneric` global property set to 'off'. For more information, see `MaskParameterAsGeneric`.

### How To Flatten Hierarchy

To set hierarchy flattening using the HDL Block Properties dialog box:

- 1 Right-click the subsystem.
- 2 Select **HDL Code > HDL Block Properties**.
- 3 For **FlattenHierarchy**, select **on**, **off**, or **inherit**.

To set hierarchy flattening from the command line, use `hdlset_param`. For example, to turn on hierarchy flattening for a subsystem, `my_dut`:

```
hdlset_param('my_dut', 'FlattenHierarchy', 'on')
```

See also `hdlset_param`.

## Options For Hierarchy Flattening

By default, a subsystem inherits its hierarchy flattening setting from the parent subsystem. However, you can enable or disable flattening for individual subsystems.

The hierarchy flattening options for a subsystem are listed in the following table.

Hierarchy Flattening Setting	Description
inherit (default)	Use the hierarchy flattening setting of the parent subsystem. If this subsystem is the highest-level subsystem, do not flatten.
on	Flatten this subsystem.
off	Do not flatten this subsystem, even if the parent subsystem is flattened.

## Limitations For Hierarchy Flattening

A subsystem cannot be flattened if the subsystem is:

- Atomic and instantiated in the design more than once.
- A black box implementation or model reference.
- An enabled or triggered subsystem.

---

**Note** This option removes subsystem boundaries before code generation. It does not necessarily generate HDL code with a completely flat hierarchy.

---

## Loop Optimization

In this section...
“Loop Streaming” on page 13-44
“Loop Unrolling” on page 13-44

With loop optimization you can stream or unroll loops in generated code. Loop streaming optimizes for area; loop unrolling optimizes for speed.

### Loop Streaming

The coder streams a loop by instantiating the loop body once and using that instance for each loop iteration.

The advantage of loop streaming is decreased area because the loop body is instantiated only once. The disadvantage of loop streaming is lower speed.

### Loop Unrolling

The coder unrolls a loop by instantiating multiple instances of the loop body in the generated code.

The unrolled code can participate in distributed pipelining and resource sharing optimizations. Distributed pipelining can increase speed; resource sharing can decrease area.

Overall, however, the multiple instances created by loop unrolling are likely to increase area. Loop unrolling also makes the code less readable.

## Optimize Loops in the MATLAB Function Block

### In this section...

“MATLAB Function Block Loop Optimization Options” on page 13-45

“How to Optimize MATLAB Function Block Loops” on page 13-45

“Limitations for MATLAB Function Block Loop Optimization” on page 13-46

### MATLAB Function Block Loop Optimization Options

The loop optimization options for a MATLAB Function block are listed in the following table.

Loop Optimization Setting	Description
none (default)	Do not optimize loops.
Unrolling	Unroll loops.
Streaming	Stream loops.

### How to Optimize MATLAB Function Block Loops

To select a loop optimization using the HDL Block Properties dialog box:

- 1** Right-click the MATLAB Function block.
- 2** Select **HDL Code > HDL Block Properties** .
- 3** For **LoopOptimization**, select **none**, **Unrolling**, or **Streaming**.

To select a loop optimization from the command line, use `hdlset_param`. For example, to turn on loop streaming for a MATLAB Function block, `my_m1fn`:

```
hdlset_param('my_m1fn', 'LoopOptimization', 'Streaming')
```

See also `hdlset_param`.

## **Limitations for MATLAB Function Block Loop Optimization**

The coder cannot stream a loop if:

- The loop index counts down. The loop index must increase by 1 on each iteration.
- There are 2 or more nested loops at the same level of hierarchy within another loop.
- Any particular persistent variable is updated both inside and outside a loop.

The coder can stream the loop when the persistent variable is:

- Updated inside the loop and read outside the loop.
- Read within the loop and updated outside the loop.



## RAM Mapping

RAM mapping is an area optimization. You can map to RAMs in HDL code in by using:

- `UseRAM` to map delays to RAM. For details, see “UseRAM” on page 9-96.
- `MapPersistentVarsToRAM` to map persistent arrays in a MATLAB Function block to RAM. For details, see “MapPersistentVarsToRAM” on page 9-81.
- RAM blocks from the `hdldemo1ib` library. For details, see “RAM Blocks” on page 11-3.
- Blocks with a RAM implementation. For details, see “RAM” on page 9-91.



# Code Generation Reports, HDL Compatibility Checker, Block Support Library, and Code Annotation

---

- “Create and Use Code Generation Reports” on page 14-2
- “Generate Code with Annotations or Comments” on page 14-27
- “Check Your Model for HDL Compatibility” on page 14-31
- “Create a Supported Blocks Library” on page 14-34
- “Trace Code Using the Mapping File” on page 14-36
- “Add or Remove the HDL Configuration Component” on page 14-39

## Create and Use Code Generation Reports

In this section...
“Information Included in Code Generation Reports” on page 14-2
“Summary Section” on page 14-3
“Traceability Report Section” on page 14-5
“Generating a Traceability Report from Configuration Parameters” on page 14-8
“Generating a Traceability Report from the Command Line” on page 14-13
“Keeping the Report Current” on page 14-16
“Tracing from Code to Model” on page 14-16
“Tracing from Model to Code” on page 14-18
“Mapping Model Elements to Code Using the Traceability Report” on page 14-21
“Traceability Report Limitations” on page 14-23
“Resource Utilization Report Section” on page 14-23
“Optimization Report Section” on page 14-25

### Information Included in Code Generation Reports

The coder creates and displays an HDL Code Generation Report when you select one or more of the following options:

GUI option	makehdl Property
Generate traceability report	Traceability, 'on'
Generate resource utilization report	ResourceReport, 'on'
Generate optimization report	OptimizationReport, 'on'

These options appear in the **Code generation report** panel of the **HDL Code** pane of the Model Configuration Parameters dialog box:

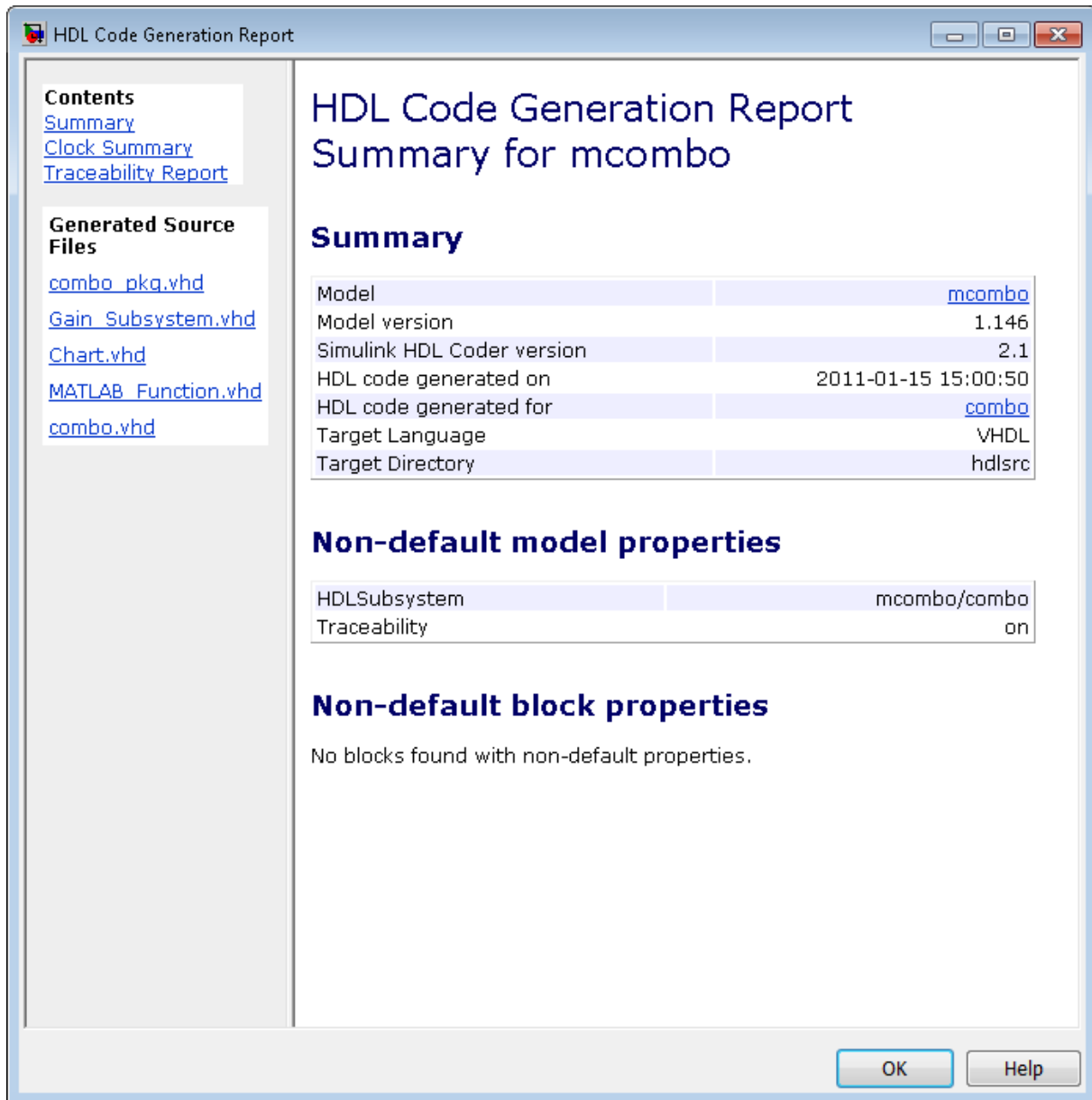


The HDL Code Generation Report is an HTML report that includes a Summary and one or more of the following optional sections:

- Traceability Report
- Resource Utilization Report
- “Optimization Report Section” on page 14-25

## Summary Section

All reports include a Summary section. The Summary lists information about the model, the DUT, the date of code generation, and top-level coder settings. The Summary also lists model properties that have nondefault values. The following report shows a typical Summary section.



## **Traceability Report Section**

Even a relatively small model can generate hundreds of lines of HDL code. The coder provides the traceability report section to help you navigate more easily between the generated code and your source model. When you enable traceability, the coder creates and displays an HTML code generation report. You can generate reports from the Configuration Parameters dialog box or the command line. A typical traceability report looks something like this:

The screenshot shows a window titled "HDL Code Generation Report" with a sidebar on the left and a main content area on the right. The sidebar contains a "Contents" section with links for "Summary", "Clock Summary", and "Traceability Report" (which is selected). Below this is a "Generated Source Files" section with links for "combo\_pkg.vhd", "Gain\_Subsystem.vhd", "Chart.vhd", "MATLAB\_Function.vhd", and "combo.vhd".

The main content area displays the "Traceability Report for mcombo". It features a large title "Traceability Report for mcombo" and a "Table of Contents" section with the following items:

1. [Eliminated / Virtual Blocks](#)
2. [Traceable Simulink Blocks / Stateflow Objects / MATLAB Functions](#)
  - o [mcombo/combo](#)
  - o [mcombo/combo/Chart](#)
  - o [mcombo/combo/Chart:110](#)
  - o [mcombo/combo/Gain\\_Subsystem](#)
  - o [mcombo/combo/MATLAB\\_Function](#)

Below the table of contents is a section titled "Eliminated / Virtual Blocks" which contains a table with two columns: "Block Name" and "Comment".

Block Name	Comment
<a href="#">&lt;S3&gt;/In1</a>	Inport
<a href="#">&lt;S3&gt;/In2</a>	Inport
<a href="#">&lt;S3&gt;/Out1</a>	Outport
<a href="#">&lt;S3&gt;/Out2</a>	Outport
<a href="#">&lt;S3&gt;/Out3</a>	Outport
<a href="#">&lt;S8&gt;:461</a>	Not traceable
<a href="#">&lt;S8&gt;:463</a>	Not traceable
<a href="#">&lt;S8&gt;:467</a>	Not traceable
<a href="#">&lt;S8&gt;:469</a>	Not traceable
<a href="#">&lt;S8&gt;:473</a>	Not traceable
<a href="#">&lt;S8&gt;:475</a>	Not traceable
<a href="#">&lt;S9&gt;/In1</a>	Inport
<a href="#">&lt;S9&gt;/Out1</a>	Outport

At the bottom of the main content area, the section "Traceable Simulink Blocks / Stateflow Objects / MATLAB Functions" is partially visible. The window has "OK" and "Help" buttons at the bottom right.



The traceability report has several subsections:

- The **Traceability Report** lists **Traceable Simulink Blocks / Stateflow Objects / MATLAB Functions**, providing a complete mapping between model elements and code. The **Eliminated / Virtual Blocks** section of the report accounts for blocks that are untraceable.
- The **Generated Source Files** table contains hyperlinks that let you view generated HDL code in a MATLAB Web Browser window. This view of the code includes hyperlinks that let you view the blocks or subsystems from which the code was generated. You can click the names of source code files generated from your model to view their contents in a MATLAB Web Browser window. The report supports two types of linkage between the model and generated code:
  - *Code-to-model* hyperlinks within the displayed source code let you view the blocks or subsystems from which the code was generated. Click the hyperlinks to view the relevant blocks or subsystems in a Simulink model window.
  - *Model-to-code* linkage lets you view the generated code for any block in the model. To highlight a block's generated code in the HTML report, right-click the block and select **HDL Code > Navigate to Code**.

---

**Note** If your model includes blocks that have requirements comments, you can also render the comments as hyperlinked comments within the HTML code generation report. See “Requirements Comments and Hyperlinks” on page 14-28 for more information.

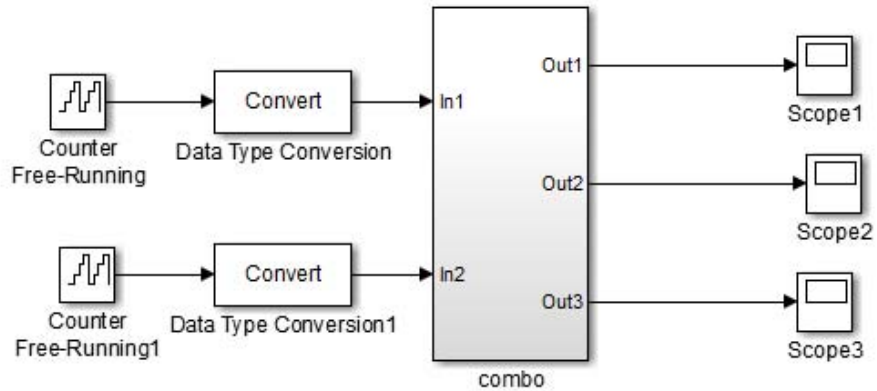
---

In the following sections, the `mcombo` example model illustrates stages in the workflow for generating code generation reports from the Model Configuration Parameters dialog box and from the command line.

To open the model, enter:

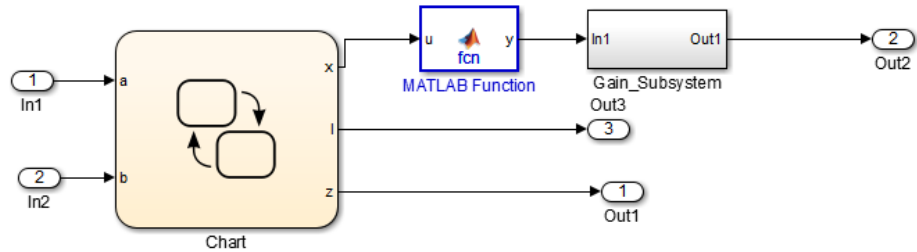
```
mcombo
```

The root-level `mcombo` model appears as follows:



Copyright 2008-2010 The MathWorks, Inc.

HDL Coder supports report generation for models, subsystems, blocks, Stateflow charts, and MATLAB Function blocks. This example uses the combo subsystem, shown in the following figure. The combo subsystem includes a Stateflow chart, a MATLAB Function block, and a subsystem.



## Generating a Traceability Report from Configuration Parameters

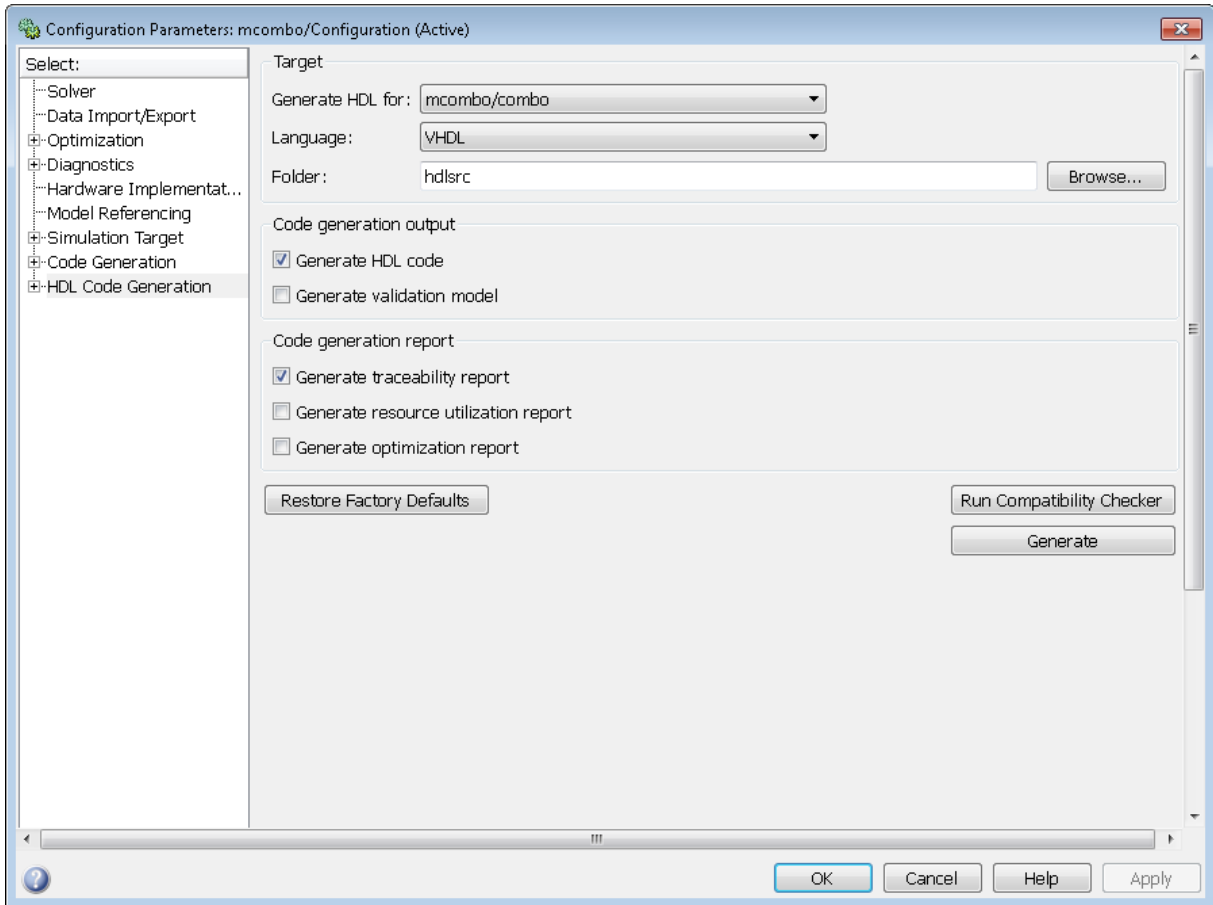
To generate a HDL Coder code generation report from the Model Configuration Parameters dialog box:

- 1 Verify that the model is open.
- 2 Open the Model Configuration Parameters dialog box and navigate to the **HDL Code** pane.
- 3 To enable report generation, select **Generate traceability report**.

If your model includes blocks that have requirements comments, you can also select **Include requirements in block comments** in the **HDL Code > Global Settings > Coding style** pane to render the comments as hyperlinked comments in the HTML code generation report. See “Requirements Comments and Hyperlinks” on page 14-28 for more information.

- 4 Verify that **Generate HDL for** specifies the correct DUT for HDL code generation. You can generate reports for the root-level model or for subsystems, blocks, Stateflow charts, or MATLAB Function blocks.
- 5 Click **Apply**.

The dialog box looks something like this:



6 Click **Generate** to initiate code and report generation.

When you select **Generate traceability report**, the coder generates HTML report files as part of the code generation process. Report file generation is the final phase of that process. As code generation proceeds, the coder displays progress messages. The process completes with messages similar to the following:

```
### Generating HTML files for traceability in slprj\hdl\mcombo\html directory ...
```

```
### HDL Code Generation Complete.
```

When code generation is complete, the HTML report appears in a new window:

The screenshot shows a window titled "HDL Code Generation Report". The window is divided into two main sections. On the left is a sidebar with a "Contents" section containing links for "Summary", "Clock Summary", and "Traceability Report" (which is selected). Below this is a "Generated Source Files" section with links for "combo\_pkg.vhd", "Gain\_Subsystem.vhd", "Chart.vhd", "MATLAB\_Function.vhd", and "combo.vhd".

The main content area is titled "Traceability Report for mcombo". It features a "Table of Contents" with two main items:
 

1. [Eliminated / Virtual Blocks](#)
2. [Traceable Simulink Blocks / Stateflow Objects / MATLAB Functions](#)
  - o [mcombo/combo](#)
  - o [mcombo/combo/Chart](#)
  - o [mcombo/combo/Chart:110](#)
  - o [mcombo/combo/Gain\\_Subsystem](#)
  - o [mcombo/combo/MATLAB\\_Function](#)

Below the table of contents is a section titled "Eliminated / Virtual Blocks" which contains a table with two columns: "Block Name" and "Comment".

Block Name	Comment
<a href="#">&lt;S3&gt;/In1</a>	Inport
<a href="#">&lt;S3&gt;/In2</a>	Inport
<a href="#">&lt;S3&gt;/Out1</a>	Outport
<a href="#">&lt;S3&gt;/Out2</a>	Outport
<a href="#">&lt;S3&gt;/Out3</a>	Outport
<a href="#">&lt;S8&gt;:461</a>	Not traceable
<a href="#">&lt;S8&gt;:463</a>	Not traceable
<a href="#">&lt;S8&gt;:467</a>	Not traceable
<a href="#">&lt;S8&gt;:469</a>	Not traceable
<a href="#">&lt;S8&gt;:473</a>	Not traceable
<a href="#">&lt;S8&gt;:475</a>	Not traceable
<a href="#">&lt;S9&gt;/In1</a>	Inport
<a href="#">&lt;S9&gt;/Out1</a>	Outport

At the bottom of the window, there are "OK" and "Help" buttons.

- 7 To view the different report sections or view the generated code files, click the hyperlinks in the **Contents** pane of the report window.

---

**Tip** The coder writes the code generation report files to a folder in the `hdlsrc\html\` folder of the build folder. The top-level HTML report file is named `system_codegen_rpt.html`, where *system* is the name of the model, subsystem, or other component selected for code generation. However, because the coder automatically opens this file after report generation, you do not need to access the HTML files directly. Instead, navigate the report using the links in the top-level window.

---

For more information on using the report you generate for tracing, see:

- “Tracing from Code to Model” on page 14-16
- “Tracing from Model to Code” on page 14-18
- “Mapping Model Elements to Code Using the Traceability Report” on page 14-21

## Generating a Traceability Report from the Command Line

To generate a HDL Coder code generation report from the command line:

- 1 Open your model by entering:

```
open_system('model_name');
```

- 2 Specify the desired device under test (DUT) for code generation by entering:

```
gcb = 'path_to_DUT';
```

You can generate reports for the root-level model or for subsystems, blocks, Stateflow charts, or MATLAB Function blocks. If you do not specify a subsystem, block, Stateflow chart, or MATLAB Function block, the coder generates a report for the top-level model.

- 3 Enable the `makehdl` property `Traceability` by entering:

```
makehdl(gcb, 'Traceability', 'on');
```

When you enable traceability, the coder generates HTML report files as part of the code generation process. Report file generation is the final phase of that process. As code generation proceeds, the coder displays progress messages. The process completes with messages similar to the following:

```
### Generating HTML files for traceability in slprj\hdl\mcombo\html directory ...
```

```
### HDL Code Generation Complete.
```



When code generation is complete, the HTML report appears in a new window:

The screenshot shows a window titled "HDL Code Generation Report" with a sidebar on the left and a main content area on the right. The sidebar contains a "Contents" section with links for "Summary", "Clock Summary", and "Traceability Report" (which is selected). Below this is a "Generated Source Files" section with links for "combo\_pkg.vhd", "Gain\_Subsystem.vhd", "Chart.vhd", "MATLAB\_Function.vhd", and "combo.vhd".

The main content area displays the "Traceability Report for mcombo". It features a "Table of Contents" with two main items: "Eliminated / Virtual Blocks" and "Traceable Simulink Blocks / Stateflow Objects / MATLAB Functions". Under "Eliminated / Virtual Blocks", there is a list of items: "mcombo/combo", "mcombo/combo/Chart", "mcombo/combo/Chart:110", "mcombo/combo/Gain\_Subsystem", and "mcombo/combo/MATLAB\_Function".

Below the table of contents is a section titled "Eliminated / Virtual Blocks" containing a table with two columns: "Block Name" and "Comment".

Block Name	Comment
<a href="#">&lt;S3&gt;/In1</a>	Inport
<a href="#">&lt;S3&gt;/In2</a>	Inport
<a href="#">&lt;S3&gt;/Out1</a>	Outport
<a href="#">&lt;S3&gt;/Out2</a>	Outport
<a href="#">&lt;S3&gt;/Out3</a>	Outport
<a href="#">&lt;S8&gt;:461</a>	Not traceable
<a href="#">&lt;S8&gt;:463</a>	Not traceable
<a href="#">&lt;S8&gt;:467</a>	Not traceable
<a href="#">&lt;S8&gt;:469</a>	Not traceable
<a href="#">&lt;S8&gt;:473</a>	Not traceable
<a href="#">&lt;S8&gt;:475</a>	Not traceable
<a href="#">&lt;S9&gt;/In1</a>	Inport
<a href="#">&lt;S9&gt;/Out1</a>	Outport

At the bottom of the window, there are "OK" and "Help" buttons.

- 4 To view the different report sections or view the generated code files, click the hyperlinks in the **Contents** pane of the report window.

---

**Tip** The coder writes the code generation report files to a folder in the `hdlsrc\html\` folder of the build folder. The top-level HTML report file is named `system_codegen_rpt.html`, where *system* is the name of the model, subsystem, or other component selected for code generation. However, because the coder automatically opens this file after report generation, you do not need to access the HTML files directly. Instead, navigate the report using the links in the top-level window.

---

For more information on using the report you generate for tracing, see:

- “Tracing from Code to Model” on page 14-16
- “Tracing from Model to Code” on page 14-18
- “Mapping Model Elements to Code Using the Traceability Report” on page 14-21

### Keeping the Report Current

If you generate a code generation report for a model, and subsequently make changes to the model, the report might become invalid.

To keep your code generation report current, you should regenerate HDL code and the report after modifying the source model.

If you close and then reopen a model without making changes, the report remains valid.

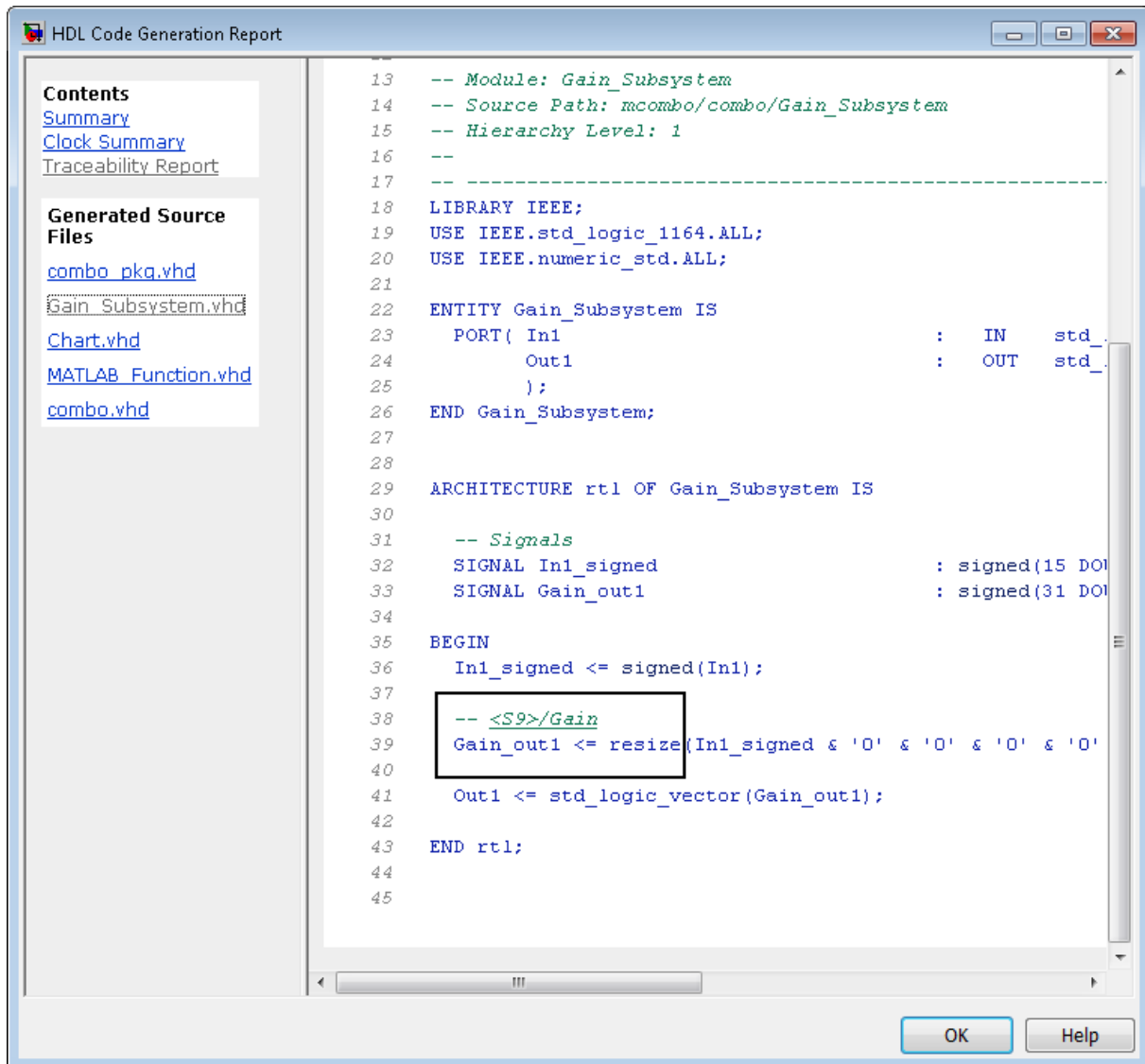
### Tracing from Code to Model

To trace from generated code to your model:

- 1 Generate code and open an HTML report for the desired DUT (see “Generating a Traceability Report from Configuration Parameters” on page 14-8 or “Generating a Traceability Report from the Command Line” on page 14-13).

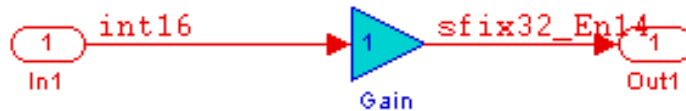
- 2 In the left pane of the HTML report window, click the desired file name in the **Generated Source Files** table to view a source code file.

The following figure shows a view of the source file `Gain_Subsystem.vhd`.



- 3 In the HTML report window, click a link to highlight the corresponding source block.

For example, in the HTML report shown in the previous figure, you could click the hyperlink for the Gain block (highlighted) to view that block in the model. Clicking the hyperlink locates and displays the corresponding block in the Simulink model window.



## Tracing from Model to Code

Model-to-code traceability lets you select a component at any level of the model, and view the code references to that component in the HTML code generation report. You can select the following objects for tracing:

- Subsystem
- Simulink block
- MATLAB Function block
- Stateflow chart, or the following elements of a Stateflow chart:
  - State
  - Transition
  - Truth table
  - MATLAB function inside a chart

To trace a model component:

- 1 Generate code and open an HTML report for the desired DUT (see “Generating a Traceability Report from Configuration Parameters” on page 14-8 or “Generating a Traceability Report from the Command Line” on page 14-13).

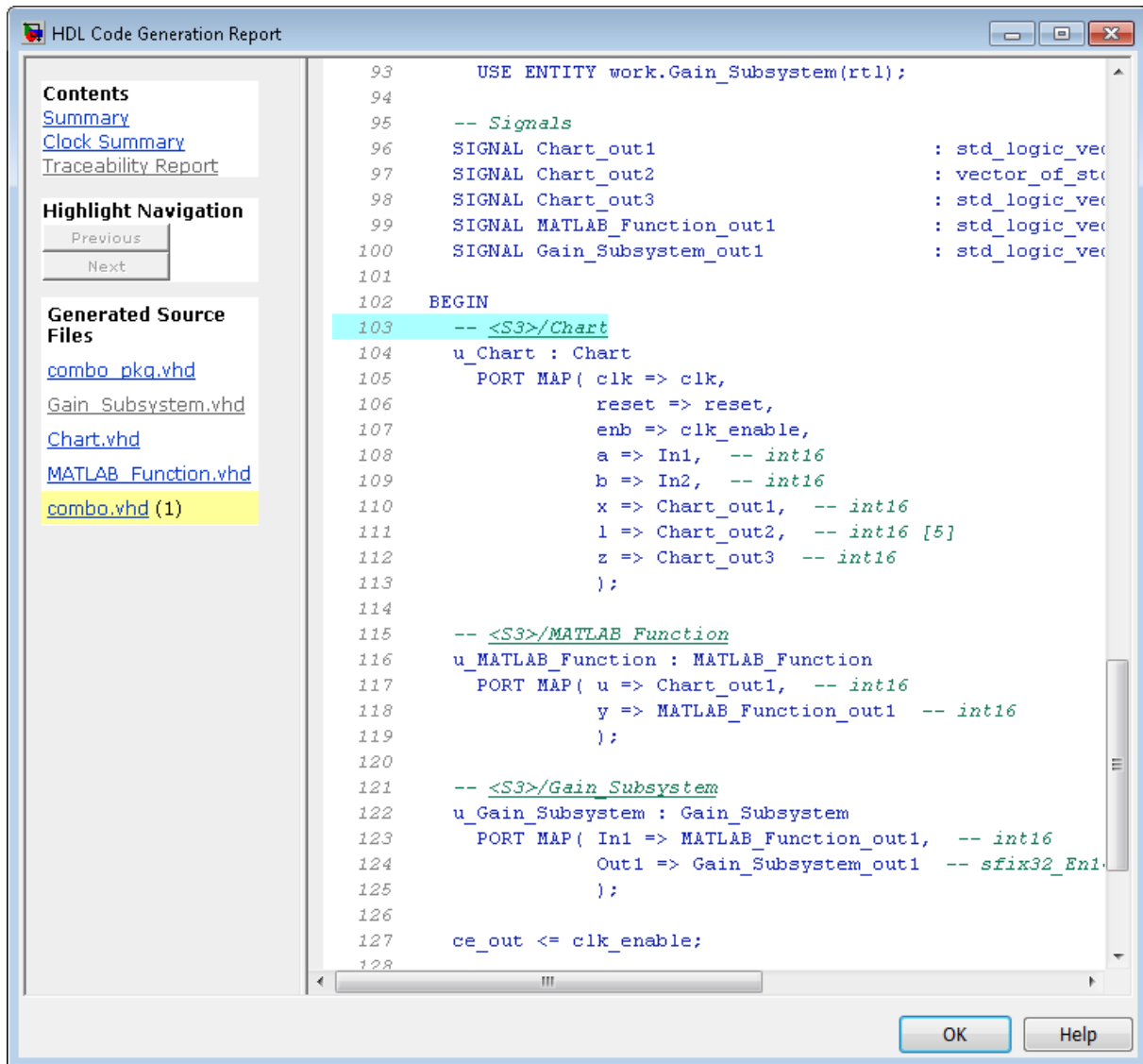
---

**Tip** If you have not generated code for the model, the coder disables the **HDL Code > Navigate to Code** menu item.

---

- 2 In the model window, right-click the component and select **HDL Code > Navigate to Code**.
- 3 Selecting **Navigate to Code** activates the HTML code generation report.

The following figure shows the result of tracing the Stateflow chart within the combo subsystem.



In the right pane of the report, the highlighted tag `<S3>/Chart` indicates the beginning of the code generated code for the chart.

In the left pane of the report, the total number of highlighted lines of code (in this case, 1) appears next to the source file name `combo.vhd`.

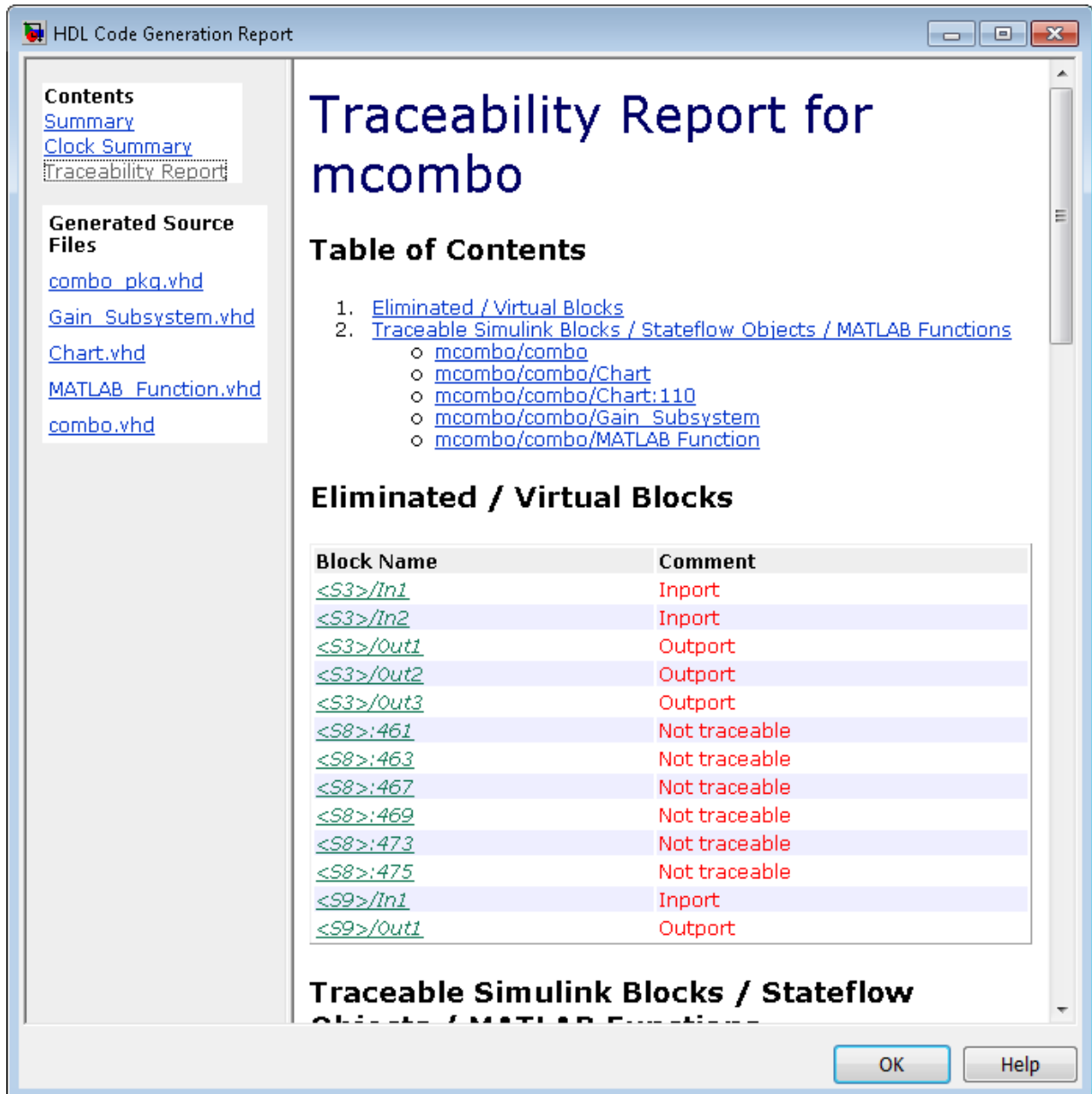
The left pane of the report also contains **Previous** and **Next** buttons. These buttons help you navigate through multiple instances of code generated for a selected component. In this example, there is only one instance, so the buttons are disabled.

## Mapping Model Elements to Code Using the Traceability Report

The **Traceability Report** section of the report provides a complete mapping between model elements and code. The **Traceability Report** summarizes:

- **Eliminated / virtual blocks:** accounts for blocks that are untraceable because they are not included in generated code
- Traceable model elements, including:
  - **Traceable Simulink blocks**
  - **Traceable Stateflow objects**
  - **Traceable MATLAB functions**

The following figure shows the beginning of a traceability report generated for the combo subsystem of the mcombo model.





## Traceability Report Limitations

The following limitations apply to HDL Coder HTML code generation reports:

- If a block name in your model contains a single quote ('), code-to-model and model-to-code traceability are disabled for that block.
- If an asterisk (\*) in a block name in your model causes a name-mangling ambiguity relative to other names in the model, code-to-model highlighting and model-to-code highlighting are disabled for that block. This is most likely to occur if an asterisk precedes or follows a slash (/) in a block name or appears at the end of a block name.
- If a block name in your model contains the character ÿ (char(255)), code-to-model highlighting and model-to-code highlighting are disabled for that block.
- Some types of subsystems are not traceable from model to code at the subsystem block level:
  - Virtual subsystems
  - Masked subsystems
  - Nonvirtual subsystems for which code has been optimized away

If you cannot trace a subsystem at the subsystem level, you might be able to trace individual blocks within the subsystem.

## Resource Utilization Report Section

When you select **Generate resource utilization report**, the coder adds a Resource Utilization Report section. The Resource Utilization Report summarizes multipliers, adders/subtractors, and registers consumed by the device under test (DUT). It also includes a detailed report on resources used by each subsystem. The detailed report includes (wherever possible) links back to corresponding blocks in your model.

The Resource Utilization Report is useful for analysis of the effects of optimizations, such as resource sharing and streaming. A typical Resource Utilization Report looks like this:

## Resource Utilization Report for dct8\_fixed

### Summary

Multipliers	13
Adders/Subtractors	29
Registers	0
RAMs	0
Multiplexers	0

### Detailed Report

[Expand all] [Collapse all]

---

#### Report for Subsystem: [OneD\\_DCT8](#)

##### Multipliers (13)

```
[+] 8x8-bit Multiply : 5  
[+] 16x16-bit Multiply : 4  
[+] 32x32-bit Multiply : 4
```

##### Adders/Subtractors (29)

```
[+] 8x8-bit Adder : 8  
[+] 17x17-bit Adder : 3  
[+] 33x33-bit Adder : 2  
[+] 8x8-bit Subtractor : 11  
[+] 17x17-bit Subtractor : 3  
[+] 33x33-bit Subtractor : 2
```

---

## Optimization Report Section

When you select **Generate optimization report**, the coder adds an Optimization Report section, with two subsections:

- **Distributed Pipelining:** this subsection shows details of subsystem-level distributed pipelining if any subsystems have the `DistributedPipelining` option enabled. Details include comparative listings of registers and flip-flops before and after applying the distributed pipelining transform.
- **Streaming and Sharing:** this subsection shows both summary and detailed information about the subsystems for which sharing or streaming is requested.

A typical Distributed Pipelining Report looks something like this:

## Distributed Pipelining Report for dct8\_fixed

### Summary

**HDL Code Generation Parameter:** HierarchicalDistPipelining: 'off'

**Subsystems with 'DistributedPipelining' set 'on':**

Subsystem	InputPipeline	OutputPipeline
<a href="#">OneD_DCT8</a>	2	2

### Detailed Report

**Subsystem:** [OneD\\_DCT8](#)

**Implementation Parameters:** DistributedPipelining: 'on'; InputPipeline: 2; OutputPipeline: 2

---

**Status:** Distributed pipelining successful.

---

#### **Before Distributed Pipelining : 32 registers (640 flip-flops)**

Registers	Count
32-bit	16
8-bit	16

#### **After Distributed Pipelining : 32 registers (552 flip-flops)**

Registers	Count
32-bit	10
8-bit	15
16-bit	7

### Generated Model

Generated model after Distributed Pipelining: [qm\\_dct8\\_fixed0](#)

## Generate Code with Annotations or Comments

In this section...
“Simulink Annotations” on page 14-27
“Text Comments” on page 14-27
“Requirements Comments and Hyperlinks” on page 14-28

The following sections describe how to use the coder to add text annotations to generated code, in the form of model annotations, text comments or requirements comments.

### Simulink Annotations

You can enter text directly on the block diagram as Simulink annotations. The coder renders text from Simulink annotations as plain text comments in generated code. The comments are generated at the same level in the model hierarchy as the subsystem(s) that contain the annotations, as if they were Simulink blocks.

See “Annotate Diagrams” in the Simulink documentation for general information on annotations.

### Text Comments

You can enter text comments at any level of the model by placing a DocBlock at the desired level and entering text comments. The coder renders text from the DocBlock in generated code as plain text comments. The comments are generated at the same level in the model hierarchy as the subsystem that contains the DocBlock.

Set the **Document type** parameter of the DocBlock to Text. The coder does not support the HTML or RTF options.

See DocBlock in the Simulink documentation for general information on the DocBlock.

## Requirements Comments and Hyperlinks

You can assign requirement comments to blocks.

If your model includes requirements comments, you can choose to render the comments in one of the following formats:

- *Text comments in generated code:* To include requirements as text comments in code, use the defaults for **Include requirements in block comments** (on) and **Generate traceability report** (off) in the Configuration Parameters dialog box.

If you generate code from the command line, set the Traceability and RequirementComments properties:

```
makehdl(gcb, 'Traceability', 'off', 'RequirementComments', 'on');
```

The following figure highlights text requirements comments generated for a Gain block from the mcombo model.

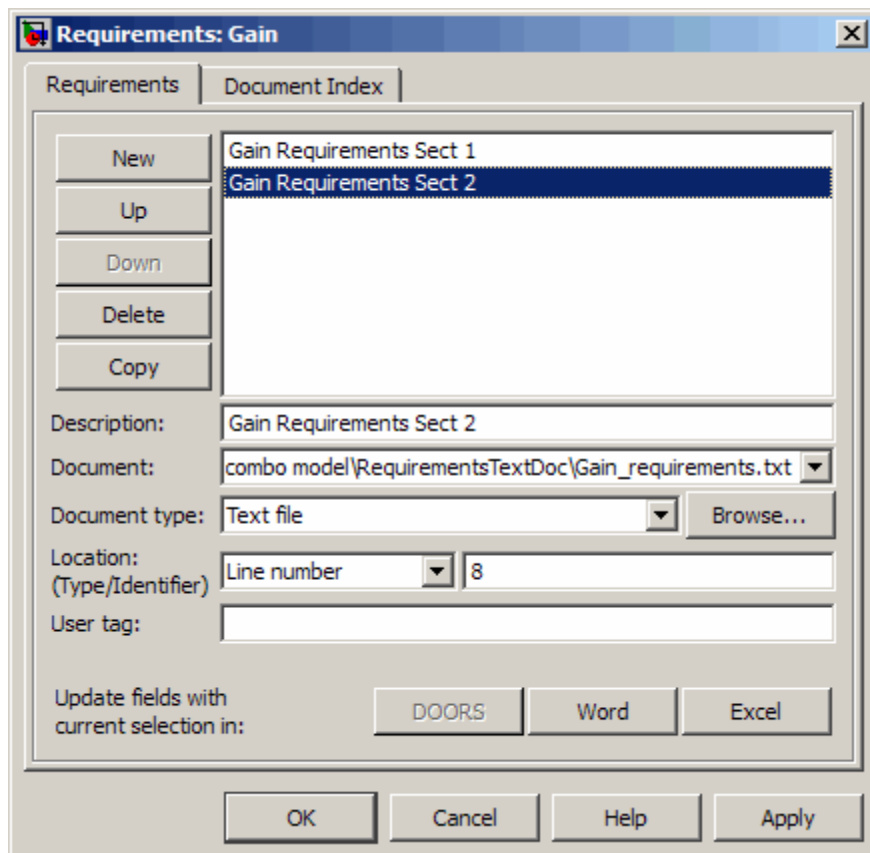
```
36 BEGIN
37     In1_signed <= signed(In1);
38
39     --
40     -- Block requirements for <S10>/Gain
41     -- 1. Gain Requirements Sect 1
42     -- 2. Gain Requirements Sect 2
43     Gain_gainparam <= to_signed(16384, 16);
44
45     Gain_out1 <= resize(In1_signed(15 DOWNT0 0) & '0'
46
47
48     Out1 <= std_logic_vector(Gain_out1);
49
50 END rtl;
```

- *Hyperlinked comments:* To include requirements comments as hyperlinked comments in an HTML code generation report, select both **Generate traceability report** and **Include requirements in block comments** in the Configuration Parameters dialog box.

If you generate code from the command line, set the Traceability and RequirementComments properties:

```
makehdl(gcb, 'Traceability', 'on', 'RequirementComments', 'on');
```

The comments include links back to a requirements document associated with the block and to the block within the original model. For example, the following figure shows two requirements links assigned to a Gain block. The links point to sections of a text requirements file.



The following figure shows hyperlinked requirements comments generated for the Gain block.

```
36 BEGIN
37     In1_signed <= signed(In1);
38
39     -- <S10>/Gain
40     --
41     --
42     -- Block requirements for <S10>/Gain
43     -- 1. Gain Requirements Sect 1
44     -- 2. Gain Requirements Sect 2
45     Gain_gainparam <= to_signed(16384, 16);
46
47     Gain_out1 <= resize(In1_signed(15 DOWNT0 0) &
48
49
50     Out1 <= std_logic_vector(Gain_out1);
51
52 END rtl;
```



## Check Your Model for HDL Compatibility

The HDL compatibility checker lets you check whether a subsystem or model is compatible with HDL code generation. You can run the compatibility checker from the command line or from the GUI.

To run the compatibility checker from the command line, use the `checkhdl` function. The syntax of the function is

```
checkhdl('system')
```

where *system* is the device under test (DUT), typically a subsystem within the current model.

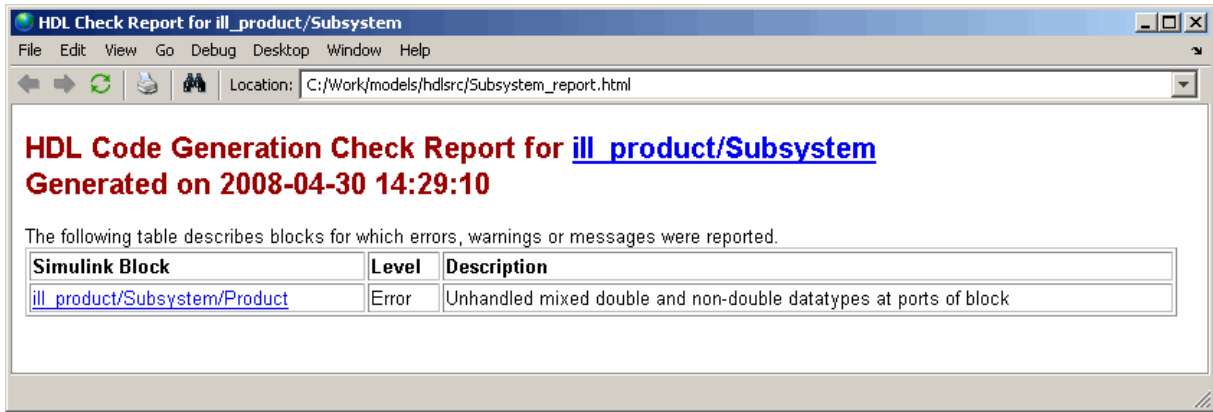
To run the compatibility checker from the GUI:

- 1 Open the Model Configuration Parameters dialog box or the Model Explorer. Select the **HDL Code Generation** pane.
- 2 Select the subsystem you want to check from the **Generate HDL for** list.
- 3 Click the **Run Compatibility Checker** button.

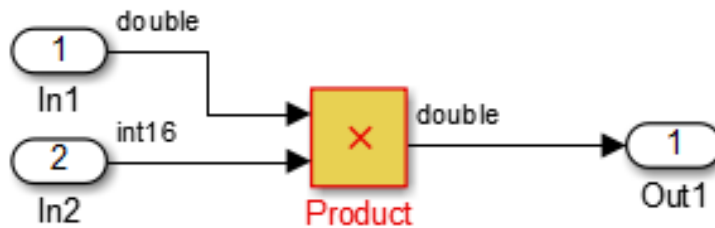
The HDL compatibility checker examines the specified system for compatibility problems, such as use of unsupported blocks, illegal data type usage, etc. The HDL compatibility checker generates an HDL Code Generation Check Report, which is stored in the target folder. The report file naming convention is `system_report.html`, where *system* is the name of the subsystem or model passed to the HDL compatibility checker.

The HDL Code Generation Check Report is displayed in a MATLAB Web Browser window. Each entry in the HDL Code Generation Check Report is hyperlinked to the block or subsystem that caused the problem. When you click the hyperlink, the block of interest highlights and displays (provided that the model referenced by the report is open).

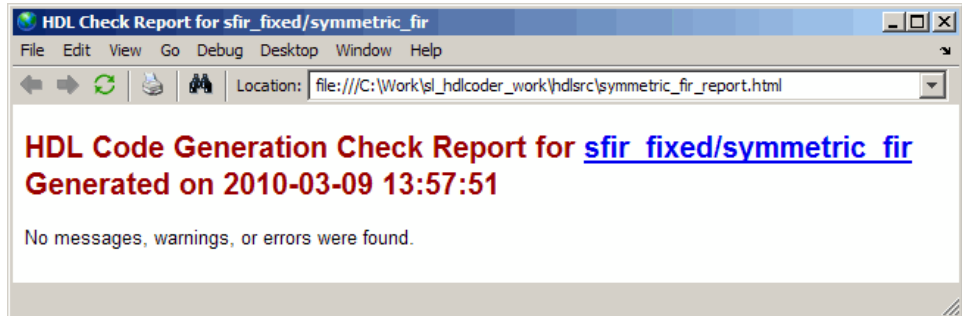
The following figure shows an HDL Code Generation Check Report that was generated for a subsystem with a Product block that was configured with a mixture of double and integer port data types. This configuration is legal in a model, but incompatible with HDL code generation.



When you click the hyperlink in the left column, the subsystem containing the offending block opens. The block of interest is highlighted, as shown in the following figure.



The following figure shows an HDL Code Generation Check Report that was generated for a subsystem that passed its compatibility checks. In this case, the report contains only a hyperlink to the subsystem that was checked.



## Create a Supported Blocks Library

The `hdl1lib.m` utility creates a library of blocks that are currently supported for HDL code generation. The block library, `hdlsupported`, affords quick access to supported blocks. By constructing models using blocks from this library, your models will be compatible with HDL code generation.

The set of supported blocks will change in future releases of the coder. To keep the `hdlsupported` library current, you should rebuild the library each time you install a new release. To create the library:

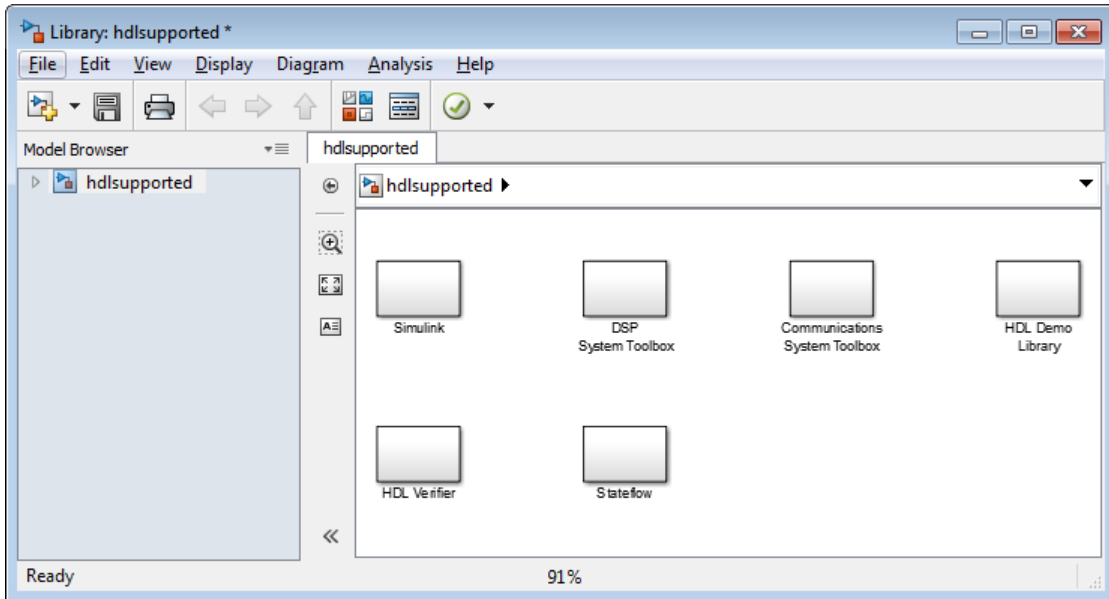
- 1 Type the following at the MATLAB prompt:

```
hdl1lib
```

`hdl1lib` starts generation of the `hdlsupported` library. Many libraries load during the creation of the `hdlsupported` library. When `hdl1lib` completes generation of the library, it does not unload these libraries.

- 2 After the library is generated, you must save it to a folder of your choice. You should retain the file name `hdlsupported`, because this document refers to the supported blocks library by that name.

The following figure shows the top-level view of the `hdlsupported` library.



Parameter settings for blocks in the `hdlsupported` library might differ from corresponding blocks in other libraries.

For detailed information about supported blocks and HDL block implementations, see “Set and View HDL Block Parameters” on page 8-2.

## Trace Code Using the Mapping File

---

**Note** This section refers to generated VHDL entities or Verilog modules generically as “entities.”

---

A *mapping file* is a text report file generated by `makehdl`. Mapping files are generated as an aid in tracing generated HDL entities back to the corresponding systems in the model.

A mapping file shows the relationship between systems in the model and the VHDL entities or Verilog modules that were generated from them. A mapping file entry has the form

```
path --> HDL_name
```

where *path* is the full path to a system in the model and *HDL\_name* is the name of the VHDL entity or Verilog module that was generated from that system. The mapping file contains one entry per line.

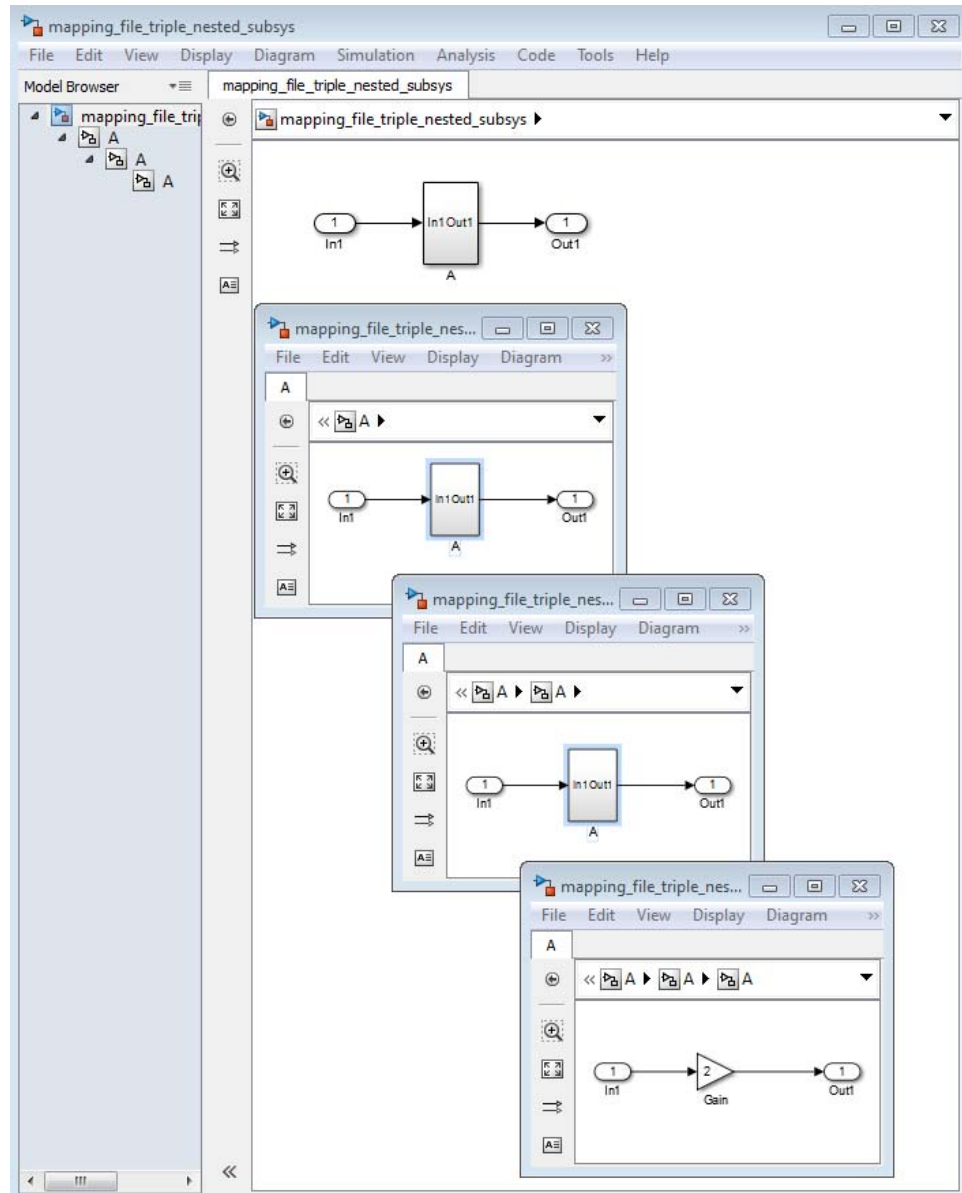
In simple cases, the mapping file may contain only one entry. For example, the `symmetric_fir` subsystem of the `sfir_fixed` model generates the following mapping file:

```
sfir_fixed/symmetric_fir --> symmetric_fir
```

Mapping files are more useful when HDL code is generated from complex models where multiple subsystems generate many entities, and in cases where conflicts between identically named subsystems are resolved by the coder.

If a subsystem name is unique within the model, the coder simply uses the subsystem name as the generated entity name. Where identically named subsystems are encountered, the coder attempts to resolve the conflict by appending a postfix string (by default, `'_entity'`) to the conflicting subsystem. If subsequently generated entity names conflict in turn with this name, incremental numerals (`1, 2, 3, . . . n`) are appended.

As an example, consider the model shown in the following figure. The top-level model contains subsystems named A nested to three levels.



When code is generated for the top-level subsystem A, makehdl works its way up from the deepest level of the model hierarchy, generating unique entity names for each subsystem.

```
makehdl('mapping_file_triple_nested_subsys/A')
### Working on mapping_file_triple_nested_subsys/A/A/A as A_entity1.vhd
### Working on mapping_file_triple_nested_subsys/A/A as A_entity2.vhd
### Working on mapping_file_triple_nested_subsys/A as A.vhd

### HDL Code Generation Complete.
```

The following example lists the contents of the resultant mapping file.

```
mapping_file_triple_nested_subsys/A/A/A --> A_entity1
mapping_file_triple_nested_subsys/A/A --> A_entity2
mapping_file_triple_nested_subsys/A --> A
```

Given this information, you can trace a generated entity back to its corresponding subsystem by using the `open_system` command, for example:

```
open_system('mapping_file_triple_nested_subsys/A/A')
```

Each generated entity file also contains the path for its corresponding subsystem in the header comments at the top of the file, as in the following code excerpt.

```
-- Module: A_entity2
-- Simulink Path: mapping_file_triple_nested_subsys/A
-- Hierarchy Level: 0
```



## Add or Remove the HDL Configuration Component

### In this section...

“What Is the HDL Configuration Component?” on page 14-39

“Adding the HDL Coder Configuration Component To a Model” on page 14-39

“Removing the HDL Coder Configuration Component From a Model” on page 14-40

### What Is the HDL Configuration Component?

The *HDL configuration component* is an internal data structure that the coder creates and attaches to a model. This component lets you view the **HDL Code** pane in the Model Configurations Parameters dialog box and set HDL code generation options. Normally, you do not need to interact with the HDL configuration component. However, there are situations where you might want to add or remove the HDL configuration component:

- A model that was created on a system that did not have HDL Coder installed does not have the HDL configuration component attached. In this case, you might want to add the HDL configuration component to the model.
- If a previous user removed the HDL configuration component, you might want to add the component back to the model.
- If a model will be running on some systems that have HDL Coder installed, and on other systems that do not, you might want to keep the model consistent between both environments. If so, you might want to remove the HDL configuration component from the model.

### Adding the HDL Coder Configuration Component To a Model

To add the HDL Coder configuration component to a model:

- 1 In the Simulink Editor, select **Code > HDL Code**.
- 2 Select **Add HDL Coder Configuration to Model**.

3 Save the model.

### **Removing the HDL Coder Configuration Component From a Model**

To remove the HDL Coder configuration component from a model:

1 In the Simulink Editor, select the **Tools** menu.

2 In **Code > HDL Code**, select **Remove HDL Coder Configuration from Model**.

The coder displays a confirmation message.

3 Click **Yes** to confirm that you want to remove the HDL Coder configuration component.

4 Save the model.

# Interfacing Subsystems and Models to HDL Code

---

- “Generate a Black Box Interface” on page 15-2
- “Generate Reusable Code for Atomic Subsystems” on page 15-8
- “Generate Interfaces for Referenced Models” on page 15-17
- “Generate Code for Enabled and Triggered Subsystems” on page 15-18
- “Why Use Xilinx System Generator Subsystems?” on page 15-22
- “Create a Xilinx System Generator Subsystem” on page 15-23
- “Using Xilinx System Generator for DSP with HDL Coder” on page 15-25
- “Code Generation for HDL Cosimulation Blocks” on page 15-29
- “Generate a Cosimulation Model” on page 15-31
- “Customize the Generated Interface” on page 15-54
- “Pass-Through and No-Op Implementations” on page 15-57
- “Limitation on Generated Verilog Interfaces” on page 15-58

## Generate a Black Box Interface

In this section...
“What Is a Black Box Interface?” on page 15-2
“Generate a Black Box Interface for a Subsystem” on page 15-2
“Generate Code for a Black Box Subsystem Implementation” on page 15-6

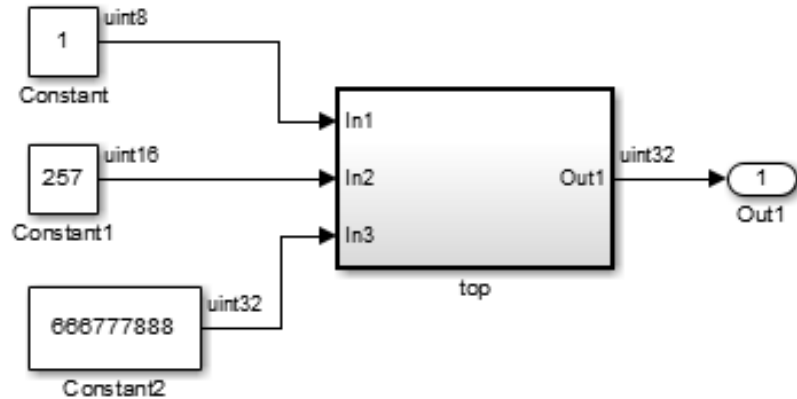
### What Is a Black Box Interface?

A *black box* interface for a subsystem is a generated VHDL component or Verilog module that includes only the HDL input and output port definitions for the subsystem. By generating such a component, you can use a subsystem in your model to generate an interface to existing manually written HDL code, third-party IP, or other code generated by HDL Coder.

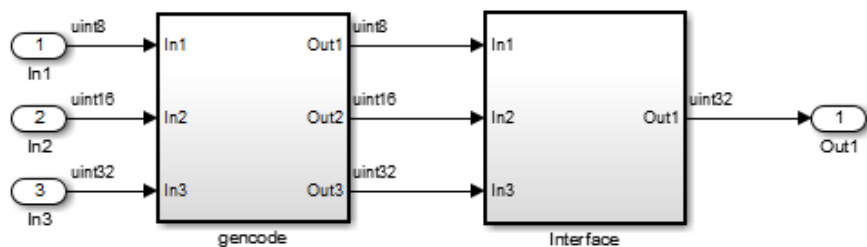
The black box implementation is available only for subsystem blocks below the level of the DUT. Virtual and atomic subsystem blocks of custom libraries that are below the level of the DUT also work with black box implementations.

### Generate a Black Box Interface for a Subsystem

To generate the interface, select the `BlackBox` implementation for one or more Subsystem blocks. Consider the following model that contains a subsystem `top`, which is the device under test.



The subsystem top contains two lower-level subsystems:



Suppose that you want to generate HDL code from top, with a black box interface from the Interface subsystem. To specify a black box interface:

- 1 Right-click the Interface subsystem and select **HDL Code > HDL Block Properties**.

The HDL Properties dialog box appears.

- 2 Set **Architecture** to BlackBox.

The following parameters are available for the black box implementation:

**HDL Properties: Subsystem**

Implementation

Architecture: BlackBox

Implementation Parameters

AddClockEnablePort	on
AddClockPort	on
AddResetPort	on
AllowDistributedPipelining	off
ClockEnableInputPort	clk_enable
ClockInputPort	clk
ConstrainedOutputPipeline	0
EntityName	
GenericList	
ImplementationLatency	-1
InlineConfigurations	on
InputPipeline	0
OutputPipeline	0
ResetInputPort	reset
VHDLArchitectureName	rtl
VHDLComponentLibrary	work

OK Cancel Help Apply

The HDL block parameters available for the black box implementation enable you to customize the generated interface. See “Customize the Generated Interface” on page 15-54 for information about these parameters.

- 3 Change parameters as desired, and click **Apply**.
- 4 Click **OK** to close the HDL Properties dialog box.

## Generate Code for a Black Box Subsystem Implementation

When you generate code for the DUT in the `ex_blackbox_subsys` model, the following messages appear:

```
>> makehdl('ex_blackbox_subsys/top')
### Generating HDL for 'ex_blackbox_subsys/top'
### Starting HDL Check.
### HDL Check Complete with 0 errors, 0 warnings and 0 messages.

### Begin VHDL Code Generation
### Working on ex_blackbox_subsys/top/gencode as hdlsrc\gencode.vhd
### Working on ex_blackbox_subsys/top as hdlsrc\top.vhd
### HDL Code Generation Complete.
```

In the progress messages, observe that the `gencode` subsystem generates a separate file, `gencode.vhd`, for its VHDL entity definition. The `Interface` subsystem does not generate such a file. The interface code for this subsystem is in `top.vhd`, generated from `ex_blackbox_subsys/top`. The following code listing shows the component definition and instantiation generated for the `Interface` subsystem.

```
COMPONENT Interface
  PORT( clk      : IN    std_logic;
        clk_enable : IN    std_logic;
        reset    : IN    std_logic;
        In1      : IN    std_logic_vector(7 DOWNTO 0); -- uint8
        In2      : IN    std_logic_vector(15 DOWNTO 0); -- uint16
        In3      : IN    std_logic_vector(31 DOWNTO 0); -- uint32
        Out1     : OUT   std_logic_vector(31 DOWNTO 0) -- uint32
        );
END COMPONENT;
```



```
...
u_Interface : Interface
  PORT MAP( clk => clk,
            clk_enable => enb,
            reset => reset,
            In1 => gencode_out1, -- uint8
            In2 => gencode_out2, -- uint16
            In3 => gencode_out3, -- uint32
            Out1 => Interface_out1 -- uint32
          );

  enb <= clk_enable;

  ce_out <= enb;

  Out1 <= Interface_out1;
```

By default, the black box interface generated for subsystems includes clock, clock enable, and reset ports. “Customize the Generated Interface” on page 15-54 describes how you can rename or suppress generation of these signals, and customize other aspects of the generated interface.

## Generate Reusable Code for Atomic Subsystems

In this section...
“Generate Reusable Code for Identical Atomic Subsystems” on page 15-8
“Generate Reusable Code for Atomic Subsystems with Tunable Mask Parameters” on page 15-12

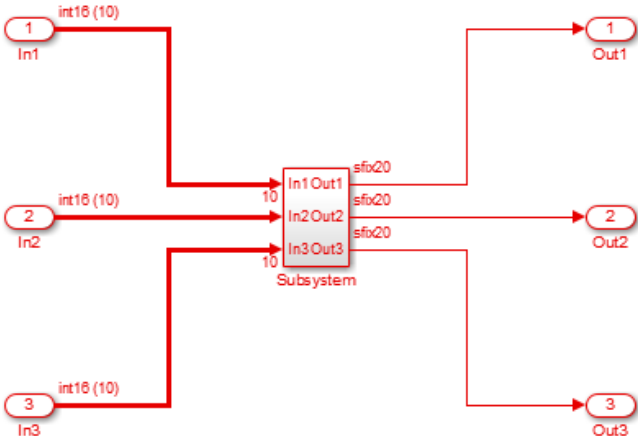
By default, the coder detects and generates reusable code for atomic subsystems that are identical, or identical except for their mask parameter values, at any level of the model hierarchy.

By generating reusable code, you can eliminate the creation of redundant source code files generated for identical subsystems. Each subsystem is configured as an atomic subsystem by selecting **Treat as atomic unit** in the Subsystem block dialog box.

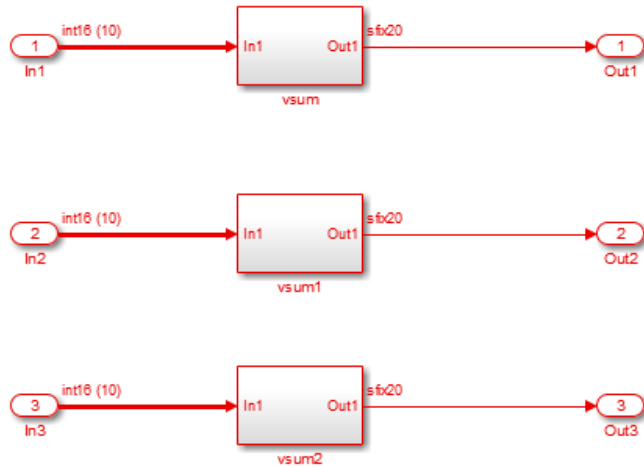
### Generate Reusable Code for Identical Atomic Subsystems

An example of a subsystem containing identical subsystems is shown in the following figures.

simplevectorsum\_3atomics ▶



simplevectorsum\_3atomics ▶ Subsystem ▶



The DUT subsystem contains three subsystems that are identical except for their subsystem names.

By default, the coder generates a single source file, `vsum.vhd`, that provides the required entity and architecture definition for the `vsum` component. The listing below shows the `makehdl` command and its progress messages.

```
>> makehdl('simplevectorsum_3atomics/DUT')
### Generating HDL for 'simplevectorsum_3atomics/DUT'
### Starting HDL Check.
### HDL Check Complete with 0 errors, 0 warnings and 0 messages.

### Begin VHDL Code Generation
### Working on simplevectorsum_3atomics/DUT/vsum as hdlsrc\vsum.vhd
### Working on simplevectorsum_3atomics/DUT as hdlsrc\DUT.vhd
### Generating package file hdlsrc\DUT_pkg.vhd
### HDL Code Generation Complete.
```

The file generated for the DUT subsystem (DUT.vhd) contains three instantiations of the vsum component, as shown in the following listing.

```
ARCHITECTURE rtl OF DUT IS

    -- Component Declarations
    COMPONENT vsum
        PORT( In1          : IN    vector_of_std_logic_vector16(0 TO 9); -- int16 [10]
              Out1         : OUT   std_logic_vector(19 DOWNT0 0) -- sfix20
              );
    END COMPONENT;

    -- Component Configuration Statements
    FOR ALL : vsum
        USE ENTITY work.vsum(rtl);

    -- Signals
    SIGNAL vsum_out1      : std_logic_vector(19 DOWNT0 0); -- ufix20
    SIGNAL vsum1_out1     : std_logic_vector(19 DOWNT0 0); -- ufix20
    SIGNAL vsum2_out1     : std_logic_vector(19 DOWNT0 0); -- ufix20

BEGIN

    u_vsum : vsum
        PORT MAP( In1 => In1, -- int16 [10]
                  Out1 => vsum_out1 -- sfix20
                );

    u_vsum1 : vsum
        PORT MAP( In1 => In2, -- int16 [10]
                  Out1 => vsum1_out1 -- sfix20
                );

    u_vsum2 : vsum
        PORT MAP( In1 => In3, -- int16 [10]
                  Out1 => vsum2_out1 -- sfix20
                );

    Out1 <= vsum_out1;

    Out2 <= vsum1_out1;
```

```

    Out3 <= vsum2_out1;

END rtl;

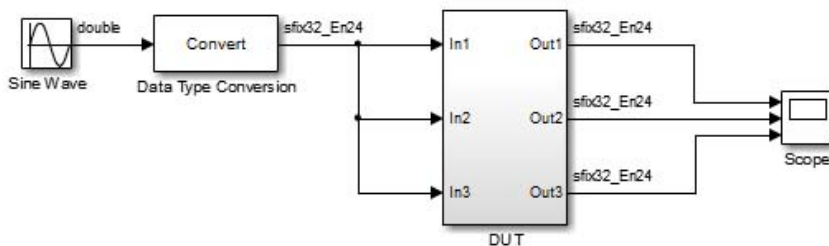
```

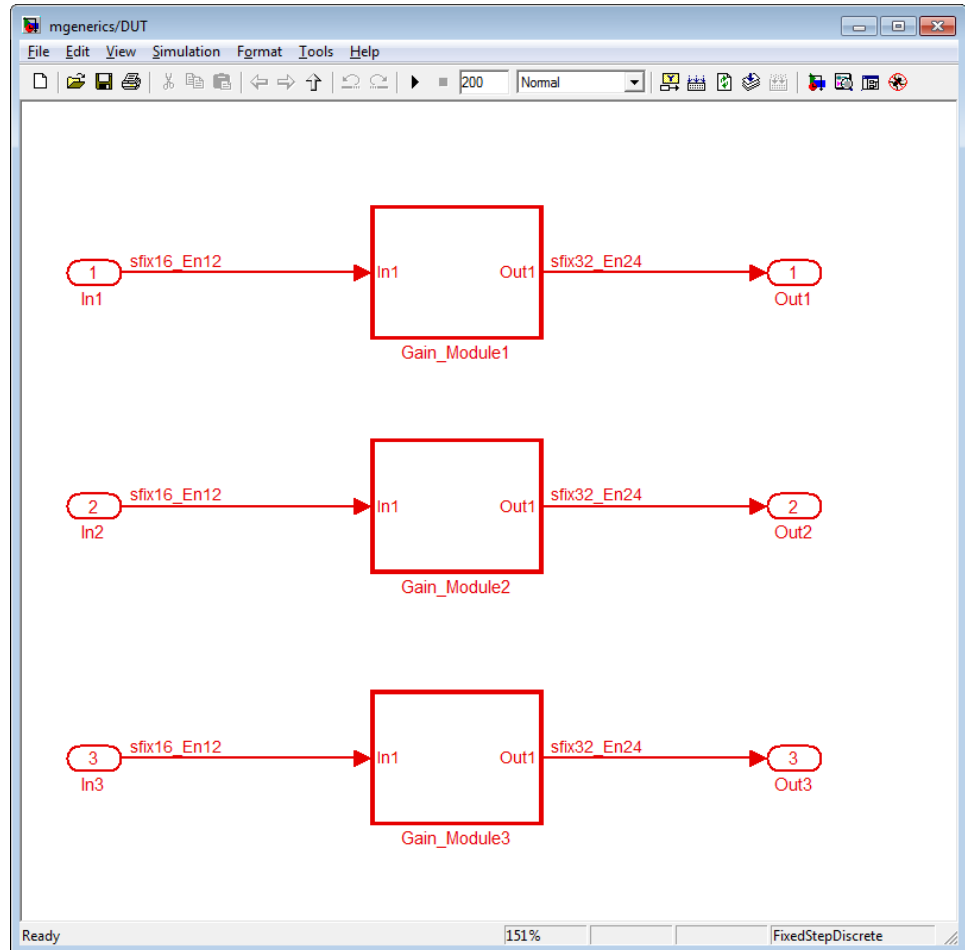
The `HandleAtomicSubsystem` property for `makehdl` lets you control generation of reusable code for atomic subsystems. `HandleAtomicSubsystem` is enabled by default. If you do not wish to generate reusable code for identical atomic subsystems, you can disable `HandleAtomicSubsystem` in your `makehdl` command, as shown in the following example.

```
makehdl(simplevectorsum_3atomics/DUT, 'HandleAtomicSubsystem', 'off')
```

## Generate Reusable Code for Atomic Subsystems with Tunable Mask Parameters

The following figures show an example of a DUT subsystem containing atomic subsystems that are identical except for their tunable mask parameter values.





In mgenerics/DUT, the gain modules are subsystems with gain values represented by tunable mask parameters. Gain values are 0.6 for Gain\_Module1, 2.4 for Gain\_Module2, and 6.8 for Gain\_Module3.

When you enable **Generate parameterized HDL code from masked subsystem**, the coder generates a single source file, Gain\_Module1.v. This file provides the module definition for the gain module component. The listing below shows the makehdl command and its progress messages.

```
>> makehdl('mgenerics/DUT','TargetLanguage','Verilog')
### Generating HDL for 'mgenerics/DUT'
### Starting HDL Check.
### HDL Check Complete with 0 errors, 0 warnings and 0 messages.

### Begin Verilog Code Generation
### Working on mgenerics/DUT/Gain_Module1 as hdl_prj\hdlsrc\Gain_Module1.v
### Working on mgenerics/DUT as hdl_prj\hdlsrc\DUT.v
### Generating HTML files for code generation report
    in s:\mask2generics_example\hdl_prj\hdlsrc\html\mgenerics directory ...

### HDL Code Generation Complete.
```

The file generated for the DUT subsystem (DUT.v) contains three instantiations of the Gain\_Module1 component, as shown in the following listing.

```
module DUT
    (
        In1,
        In2,
        In3,
        Out1,
        Out2,
        Out3
    );

    input  signed [15:0] In1; // sfix16_En12
    input  signed [15:0] In2; // sfix16_En12
    input  signed [15:0] In3; // sfix16_En12
    output signed [31:0] Out1; // sfix32_En24
    output signed [31:0] Out2; // sfix32_En24
    output signed [31:0] Out3; // sfix32_En24

    wire signed [31:0] Gain_Module1_out1; // sfix32_En24
    wire signed [31:0] Gain_Module2_out1; // sfix32_En24
```



```
wire signed [31:0] Gain_Module3_out1; // sfix32_En24

// <S1>/Gain_Module1
Gain_Module1 # (.param_gain(2458)
               )
               u_Gain_Module1 (.In1(In1), // sfix16_En12
                               .Out1(Gain_Module1_out1) // sfix32_En24
                               );

assign Out1 = Gain_Module1_out1;

// <S1>/Gain_Module2
Gain_Module1 # (.param_gain(9830)
               )
               u_Gain_Module2 (.In1(In2), // sfix16_En12
                               .Out1(Gain_Module2_out1) // sfix32_En24
                               );

assign Out2 = Gain_Module2_out1;

// <S1>/Gain_Module3
Gain_Module1 # (.param_gain(27853)
               )
               u_Gain_Module3 (.In1(In3), // sfix16_En12
                               .Out1(Gain_Module3_out1) // sfix32_En24
                               );

assign Out3 = Gain_Module3_out1;

endmodule // DUT
```

The file generated for the Gain\_Module1 block contains a Verilog parameter, param\_gain, as shown in the following listing.

```
module Gain_Module1
(
    In1,
    Out1
);
```

```
input  signed [15:0] In1; // sfix16_En12
output signed [31:0] Out1; // sfix32_En24

parameter signed [15:0] param_gain = 2458; // sfix16_En12

wire signed [15:0] kconst; // sfix16_En12
wire signed [31:0] Gain_out1; // sfix32_En24

assign kconst = param_gain;

// <S2>/Gain
assign Gain_out1 = In1 * kconst;

assign Out1 = Gain_out1;

endmodule // Gain_Module1
```

The `MaskParameterAsGeneric` property for `makehdl` lets you control generation of reusable code for atomic subsystems. `MaskParameterAsGeneric` is disabled by default. If you wish to generate reusable code for identical atomic subsystems, you can enable `MaskParameterAsGeneric` in your `makehdl` command, as shown in the following example.

```
makehdl(mgenerics/DUT, 'MaskParameterAsGeneric', 'on')
```

See also “Generate parameterized HDL code from masked subsystem” on page 7-70.

## Generate Interfaces for Referenced Models

Simulink model referencing enables you to include models in other models as blocks. Included models are referenced through Model blocks. See “Model Reference” in the Simulink documentation for details.

For Model blocks, the coder generates a VHDL component or a Verilog module instantiation. However, `makehdl` does not attempt to generate HDL code for the models referenced from Model blocks. You must generate HDL code for each referenced model individually. To generate code for a referenced model:

- 1 Select the referencing Model block.
- 2 Double-click the Model block to open the referenced model.
- 3 Invoke the `checkhdl` and `makehdl` functions to check and generate code from that model.

---

**Note** The `checkhdl` function does not check port data types within the referenced model.

---

The Model block is useful for blocks you instantiate multiple times, or for blocks for which you already have manually written HDL code. The generated HDL will contain the code that is required to interface to the referenced HDL code. Code is generated with the following assumptions:

- Every HDL entity or module requires clock, clock enable, and reset ports. Therefore, these ports are defined for each generated entity or module.
- Use of Simulink data types is assumed. For VHDL code, port data types are assumed to be `STD_LOGIC` or `STD_LOGIC_VECTOR`.

---

**Tip** If you encounter typing or naming conflicts between vector ports when interfacing two or more generated VHDL code modules, consider using the `ScalarizePorts` property to generate nonconflicting port definitions.

---

## Generate Code for Enabled and Triggered Subsystems

### In this section...

“Code Generation for Enabled Subsystems” on page 15-18

“Code Generation for Triggered Subsystems” on page 15-19

“Best Practices for Using Enabled and Triggered Subsystems” on page 15-21

### Code Generation for Enabled Subsystems

An enabled subsystem is a subsystem that receives a control signal via an Enable block. The enabled subsystem executes at each simulation step where the control signal has a positive value. For detailed information on how to construct and configure enabled subsystems, see “Enabled Subsystems” in the Simulink documentation.

The coder supports HDL code generation for enabled subsystems that meet the following conditions:

- The DUT (i.e., the top-level subsystem for which code is generated) must not be an enabled subsystem.
- The coder does not support subsystems that are *both* triggered *and* enabled for HDL code generation.
- The enable signal must be a scalar.
- The data type of the enable signal must be either `boolean` or `ufix1`.
- Outputs of the enabled subsystem must have an initial value of 0.
- All inputs and outputs of the enabled subsystem (including the enable signal) must run at the same rate.
- The **Show output port** parameter of the Enable block must be set to `Off`.
- The **States when enabling** parameter of the Enable block must be set to `held` (i.e., the Enable block does not reset states when enabled).
- The **Output when disabled** parameter for the enabled subsystem output port(s) must be set to `held` (i.e., the enabled subsystem does not reset output values when disabled).

- The following blocks are not supported in enabled subsystems targeted for HDL code generation:
  - dspmlti4/CIC Decimation
  - dspmlti4/CIC Interpolation
  - dspmlti4/FIR Decimation
  - dspmlti4/FIR Interpolation
  - dspsigops/Downsample
  - dspsigops/Upsample
  - HDL Cosimulation blocks for HDL Verifier
  - simulink/Signal Attributes/Rate Transition
  - hlldemolib/FFT
  - hlldemolib/HDL Streaming FFT
  - hlldemolib/Dual Port RAM
  - hlldemolib/Simple Dual Port RAM
  - hlldemolib/Single Port RAM
  - Subsystem black box (SubsystemBlackBoxHDLInstantiation)

The Automatic Gain Controller example model to shows how you can use enabled subsystems in HDL code generation. To open the example model, enter:

```
hdlcoder_agc
```

## Code Generation for Triggered Subsystems

A triggered subsystem is a subsystem that receives a control signal via a Trigger block. The enabled triggered executes for one clock cycle each time a trigger event occurs. For detailed information on how to define trigger events and configure triggered subsystems, see “Triggered Subsystems” in the Simulink documentation.

The coder supports HDL code generation for triggered subsystems that meet the following conditions:

- The DUT (that is, the top-level subsystem for which code is generated) must not be a triggered subsystem.
- The coder does not support subsystems that are *both* triggered *and* enabled for HDL code generation.
- The trigger signal must be a scalar.
- The data type of the trigger signal must be either `boolean` or `ufix1`.
- Outputs of the triggered subsystem must have an initial value of 0.
- All inputs and outputs of the triggered subsystem (including the trigger signal) must run at the same rate. (See “Note on Use of the Signal Builder Block” on page 15-21 for information on a special case.)
- The **Show output port** parameter of the Trigger block must be set to `Off`.
- The following blocks are not supported in triggered subsystems targeted for HDL code generation:
  - Discrete-Time Integrator
  - `dspmlti4/CIC Decimation`
  - `dspmlti4/CIC Interpolation`
  - `dspmlti4/FIR Decimation`
  - `dspmlti4/FIR Interpolation`
  - `dspsigops/Downsample`
  - `dspsigops/Upsample`
  - HDL Cosimulation blocks for HDL Verifier
  - `simulink/Signal Attributes/Rate Transition`
  - `hlddemolib/FFT`
  - `hlddemolib/HDL Streaming FFT`
  - `hlddemolib/Dual Port RAM`
  - `hlddemolib/Simple Dual Port RAM`
  - `hlddemolib/Single Port RAM`
  - Subsystem black box (`SubsystemBlackBoxHDLInstantiation`)

---

**Tip** For best results the trigger signal should be a synchronous signal.

---

## **Best Practices for Using Enabled and Triggered Subsystems**

It is good practice to consider the following when using enabled and triggered subsystems in models targeted for HDL code generation:

- For synthesis results to match Simulink results, Enable and Trigger ports should be driven by registered logic (with a synchronous clock) on the FPGA.
- The use of enabled or triggered subsystems can affect synthesis results in the following ways:
  - In some cases the system clock speed may drop by a small percentage.
  - Generated code will use more resources, scaling with the number of enabled or triggered subsystem instances and the number of output ports per subsystem.

### **Note on Use of the Signal Builder Block**

When you connect outputs from a Signal Builder block to a triggered subsystem, you may need to use a Rate Transition block. To run all triggered subsystem ports at the same rate:

- If the trigger source is a Signal Builder block, but the other triggered subsystem inputs come from other sources, insert a Rate Transition block into the signal path before the trigger input.
- If all inputs (including the trigger) come from a Signal Builder block, they have the same rate, so special action is not required.

## Why Use Xilinx System Generator Subsystems?

You can generate HDL code from a model with both Simulink and Xilinx blocks using Xilinx System Generator (XSG) subsystems.

Using both Simulink and Xilinx blocks in your model provides the following benefits:

- A single platform for combined Simulink and Xilinx System Generator simulation, code generation, and synthesis.
- Targeted code generation: Xilinx System Generator for DSP generates code from Xilinx blocks; HDL Coder generates code from Simulink blocks.
- HDL Coder area and speed optimizations for Simulink components.



## Create a Xilinx System Generator Subsystem

### In this section...

“How to Create a Xilinx System Generator Subsystem” on page 15-23

“Requirements for Xilinx System Generator Subsystems” on page 15-23

“Limitations for Code Generation from Xilinx System Generator Subsystems” on page 15-24

## How to Create a Xilinx System Generator Subsystem

- 1 Create a subsystem containing the Xilinx blocks and set its architecture to "Module".
- 2 Add a System Generator token at the top level of the subsystem.

You can have subsystem hierarchy in a Xilinx System Generator Subsystem, but there must be a System Generator token at the top level of the hierarchy.

- 3 Connect each subsystem input or output port directly to a Gateway In or Gateway Out block.
- 4 On each Gateway Out block, select the **Propagate data type to output** option.

For an example of HDL code generation from a Xilinx System Generator subsystem, see “Using Xilinx System Generator for DSP with HDL Coder” on page 15-25.

## Requirements for Xilinx System Generator Subsystems

You must group your Xilinx blocks into one or more Xilinx System Generator (XSG) subsystems for code generation. An XSG subsystem can contain a hierarchy of subsystems.

To generate code from a Xilinx System Generator Subsystem, you must use ISE Design Suite 13.4 or later.

An XSG subsystem is a Subsystem block with:

- Architecture set to **Module**.
- One System Generator token, placed at the top level of the XSG subsystem hierarchy.
- Xilinx blocks.
- Simulink blocks not requiring code generation.
- Input and output ports connected directly to Gateway In or Gateway Out blocks.
- **Propagate data type to output** option enabled on Gateway Out blocks.
- Matching input and output data types on Gateway In blocks. See “Limitations for Code Generation from Xilinx System Generator Subsystems” on page 15-24.

## **Limitations for Code Generation from Xilinx System Generator Subsystems**

Code generation from Xilinx System Generator (XSG) subsystems has the following limitations:

- `ConstrainedOutputPipeline`, `InputPipeline`, and `OutputPipeline` are the only valid block properties for an XSG subsystem.
- HDL Coder does not generate code for blocks within an XSG subsystem, including Simulink blocks.
- Gateway In blocks must not do nontrivial data type conversion. For example, a Gateway In block can convert between the `sfixed8_en6` and `fix8_6` data types, but changing data sign, word length, or fraction length is not allowed.
- For Verilog code generation, Simulink block names in your design cannot be the same as Xilinx names. Similarly, Xilinx blocks in your design cannot have the same name as other Xilinx blocks. The coder cannot resolve these name conflicts, and generates an error late in the code generation process.

## Using Xilinx System Generator for DSP with HDL Coder

This example shows how to use Xilinx System Generator for DSP with HDL Coder™.

### Setup for Xilinx System Generator

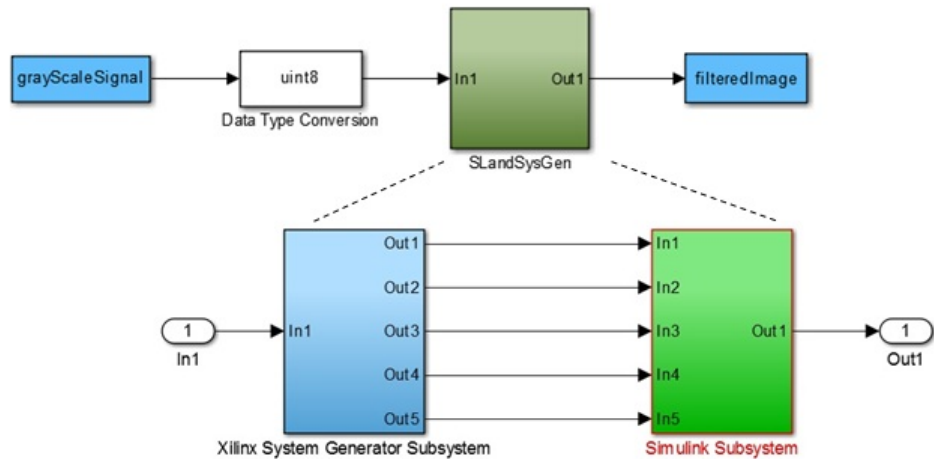
In order to use the Xilinx System Generator Subsystem block, you must have Xilinx ISE 13.4 set up with Simulink.

### Introduction

Using the Xilinx System Generator Subsystem block enables you to model designs using blocks from both Simulink and Xilinx, and to automatically generate integrated HDL code. HDL Coder™ generates HDL code from the Simulink blocks, and uses Xilinx System Generator to generate HDL code from the Xilinx System Generator Subsystem blocks.

In this example, the design, or code generation subsystem, contains two parts: one with Simulink native blocks, and one with Xilinx blocks. The Xilinx blocks are grouped in a Xilinx System Generator Subsystem (hdlcoder\_slsysgen/SLandSysGen/Xilinx System Generator Subsystem). System Generator optimizes these blocks for Xilinx FPGAs. In the rest of the design, Simulink blocks and HDL Coder™ offer many model-based design features, such as distributed pipelining and delay balancing, to perform model-level optimizations.

```
open_system('hdlcoder_slsysgen');  
open_system('hdlcoder_slsysgen/SLandSysGen');
```



## Create Xilinx System Generator Subsystem

To create a Xilinx System Generator subsystem:

- 1 Put the Xilinx blocks in one subsystem and set its architecture to "Module" (the default value).
- 2 Place a System Generator token at the top level of the subsystem. You can have subsystem hierarchy in a Xilinx System Generator Subsystem, but there must be a System Generator token at the top level of the hierarchy.

```
open_system('hdlcoder_slsgen/SLandSysGen/Xilinx System Generator Subsystem')
```



### Configure Gateway In and Gateway Out Blocks

In each Xilinx System Generator subsystem, you must connect input and output ports directly to Gateway In and Gateway Out blocks.

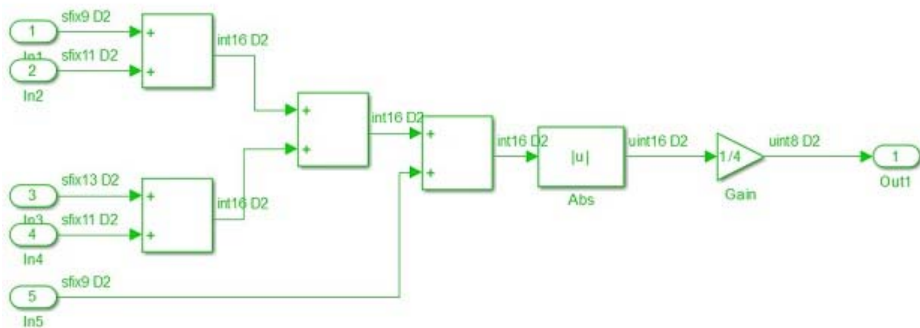
Gateway In blocks must not do non-trivial data type conversion. For example, a Gateway In block can convert between `uint8` and `UFix_8_0`, but changing data sign, word length, or fraction length is not allowed.

### Perform Model-Level Optimizations for Simulink Components

In this example, a sum tree is modeled with Simulink blocks. The distributed pipelining feature can take care of the speed optimization.

Here the Output Pipeline property of `hdlcoder_slsgen/SLandSysGen/Simulink Subsystem` is set to "4" and the Distributed Pipelining property is set to "on". Pipeline registers inserted by the distributed pipelining feature will be pushed into the sum tree to reduce the critical path without changing the model function. Other optimizations, such as resource sharing, are also available, but not used in this example.

```
open_system('hdlcoder_slsgen/SLandSysGen/Simulink Subsystem');
```



### Generate HDL Code

You can use either `makehdl` at the command line or HDL Workflow Advisor to generate HDL code. To use `makehdl`:

```
makehdl('hdlcoder_slsysgen/SLandSysGen');
```

You can also generate a testbench, simulate, and synthesize the design as you would for any other model.

## Code Generation for HDL Cosimulation Blocks

The coder supports HDL code generation for the following HDL Cosimulation blocks:

- HDL Verifier for use with Mentor Graphics ModelSim
- HDL Verifier for use with Cadence Incisive

Each of the HDL Cosimulation blocks cosimulates a hardware component by applying input signals to, and reading output signals from, an HDL model that executes under an HDL simulator.

See the “Define the HDL Cosimulation Block Interface for Component Simulation” section of the HDL Verifier documentation for information on timing, latency, data typing, frame-based processing, and other issues that may be of concern to you when setting up an HDL cosimulation.

You can use an HDL Cosimulation block with the coder to generate an interface to your manually written or legacy HDL code. When an HDL Cosimulation block is included in a model, the coder generates a VHDL or Verilog interface, depending on the selected target language.

When the target language is VHDL, the generated interface includes:

- An entity definition. The entity defines ports (input, output, and clock) corresponding in name and data type to the ports configured on the HDL Cosimulation block. Clock enable and reset ports are also declared.
- An RTL architecture including a component declaration, a component configuration declaring signals corresponding to signals connected to the HDL Cosimulation ports, and a component instantiation.
- Port assignment statements as required by the model.

When the target language is Verilog, the generated interface includes:

- A module defining ports (input, output, and clock) corresponding in name and data type to the ports configured on the HDL Cosimulation block. The module also defines clock enable and reset ports, and wire declarations corresponding to signals connected to the HDL Cosimulation ports.

- A module instance.
- Port assignment statements as required by the model.

The requirements for using the HDL Cosimulation block for code generation are the same as those for cosimulation. If you want to check these conditions before initiating code generation, select **Simulation > Update Diagram**.



## Generate a Cosimulation Model

### In this section...

“What Is A Cosimulation Model?” on page 15-31

“Generating a Cosimulation Model from the GUI” on page 15-32

“Structure of the Generated Model” on page 15-37

“Launching a Cosimulation” on page 15-44

“The Cosimulation Script File” on page 15-46

“Complex and Vector Signals in the Generated Cosimulation Model” on page 15-49

“Generating a Cosimulation Model from the Command Line” on page 15-51

“Naming Conventions for Generated Cosimulation Models and Scripts” on page 15-52

“Limitations for Cosimulation Model Generation” on page 15-52

---

**Note** To use this feature, your installation must include for one or both of the following:

- HDL Verifier for use with Mentor Graphics ModelSim
- HDL Verifier for use with Cadence Incisive

---

## What Is A Cosimulation Model?

A cosimulation model is an automatically generated Simulink model configured for both Simulink simulation and cosimulation of your design with an HDL simulator. HDL Coder supports automatic generation of a cosimulation model as a part of the test bench generation process.

The cosimulation model includes:

- A behavioral model of your design, realized in a Simulink subsystem.

- A corresponding HDL Cosimulation block, configured to cosimulate the design using HDL Verifier. The coder configures the HDL Cosimulation block for use with one of the following cosimulation tools:
  - HDL Verifier for use with Mentor Graphics ModelSim
  - HDL Verifier for use with Cadence Incisive
- Test input data, calculated from the test bench stimulus that you specify.
- Scope blocks, which let you observe and compare the DUT and HDL cosimulation outputs, and any error between these signals.
- Goto and From blocks that capture the stimulus and response signals from the DUT and use these signals to drive the cosimulation.
- A comparison/assertion mechanism that reports discrepancies between the original DUT output and the cosimulation output .

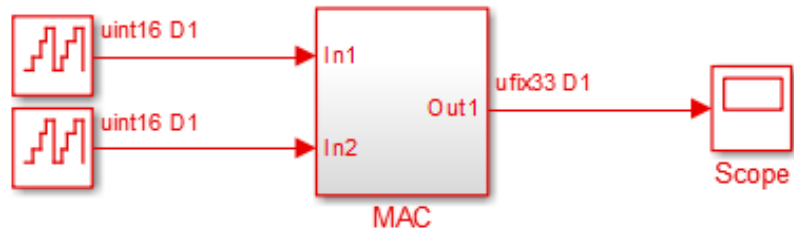
In addition to the generated model, the coder generates a TCL script that launches and configures your cosimulation tool. Comments in the script file document clock, reset, and other timing signal information defined by the coder for the cosimulation tool.

### **Generating a Cosimulation Model from the GUI**

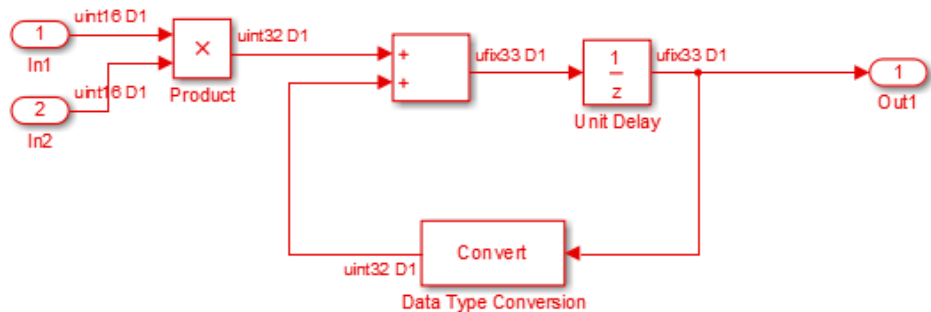
This example demonstrates the process for generating a cosimulation model. The example model, `hdl_cosim_demo1`, implements a simple multiply and accumulate (MAC) algorithm. Open the model by entering the name at the MATLAB command line:

```
hdl_cosim_demo1
```

The following figure shows the top-level model.

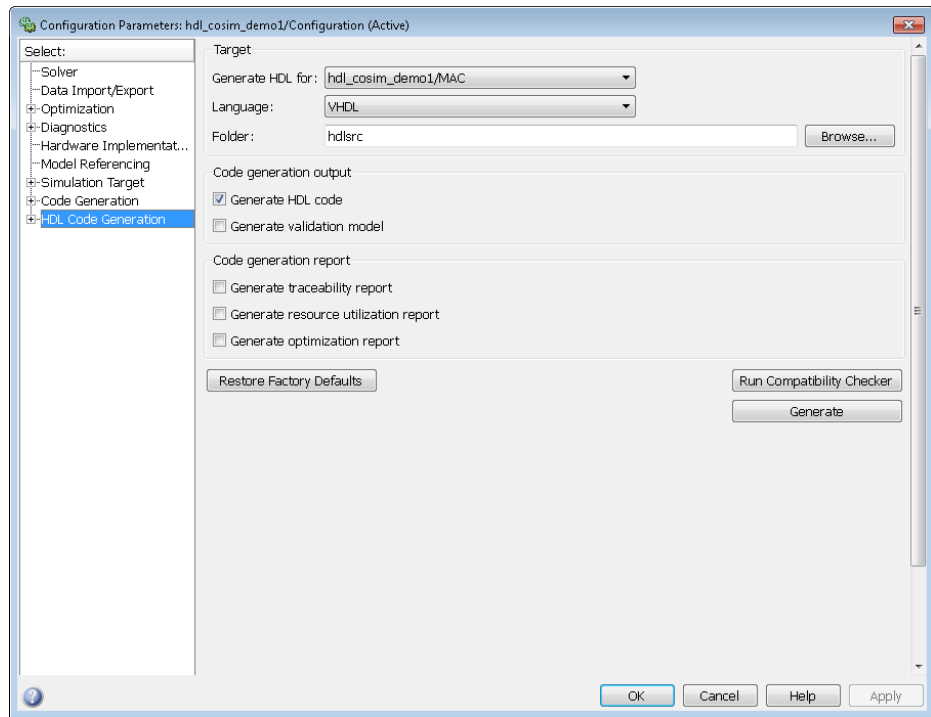


The DUT is the MAC subsystem.



Cosimulation model generation takes place during generation of the test bench. As a best practice, generate HDL code before generating a test bench, as follows:

- 1 In the **HDL Code** pane of the Model Configuration Parameters dialog box, select the DUT for code generation. In this case, it is `hdl_cosim_demo1/MAC`.



**2** Click **Apply**.

**3** Click **Generate**. The coder displays progress messages, as shown in the following listing:

```

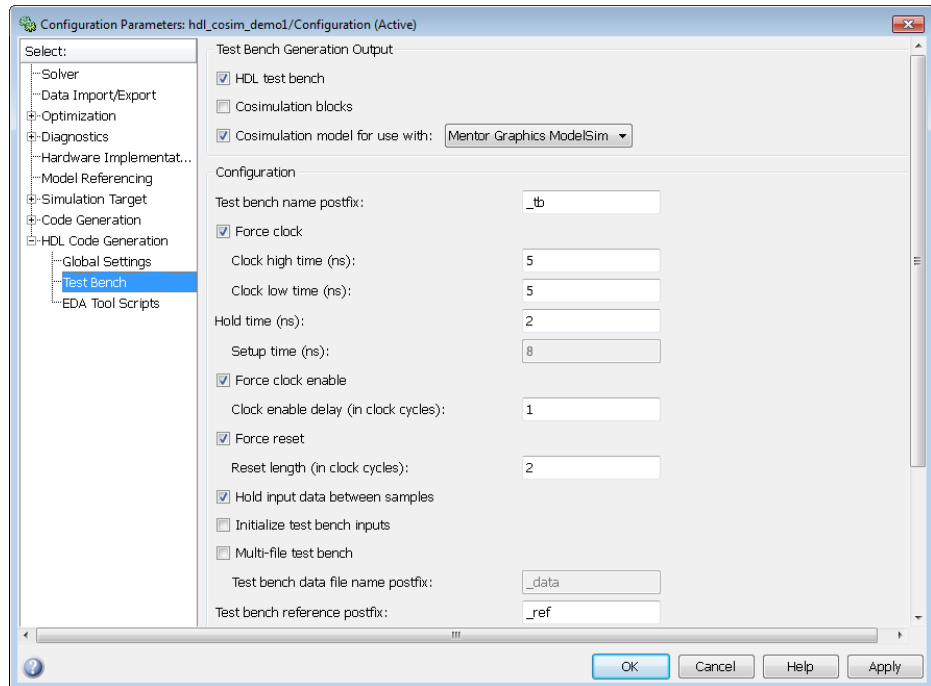
### Applying HDL Code Generation Control Statements
### Starting HDL Check.
### HDL Check Complete with 0 error, 0 warning and 0 message.

### Begin VHDL Code Generation
### Working on hdl_cosim_demo1/MAC as hdlsrc\MAC.vhd
### HDL Code Generation Complete.

```

Next, configure the test bench options to include generation of a cosimulation model:

- 1 Select the **HDL Code Generation > Test Bench** pane of the Configuration Parameters dialog box.
- 2 Select the **Cosimulation model for use with:** option. Selecting this check box enables the pulldown menu to the right.



- 3 Select the desired cosimulation tool from the dropdown menu.
- 4 Configure required test bench options. The coder records option settings in a generated script file (see “The Cosimulation Script File” on page 15-46).
- 5 Click **Apply**.

Next, generate test bench code and the cosimulation model:

- 1 Click **Generate Test Bench**. The coder displays progress messages as shown in the following listing:

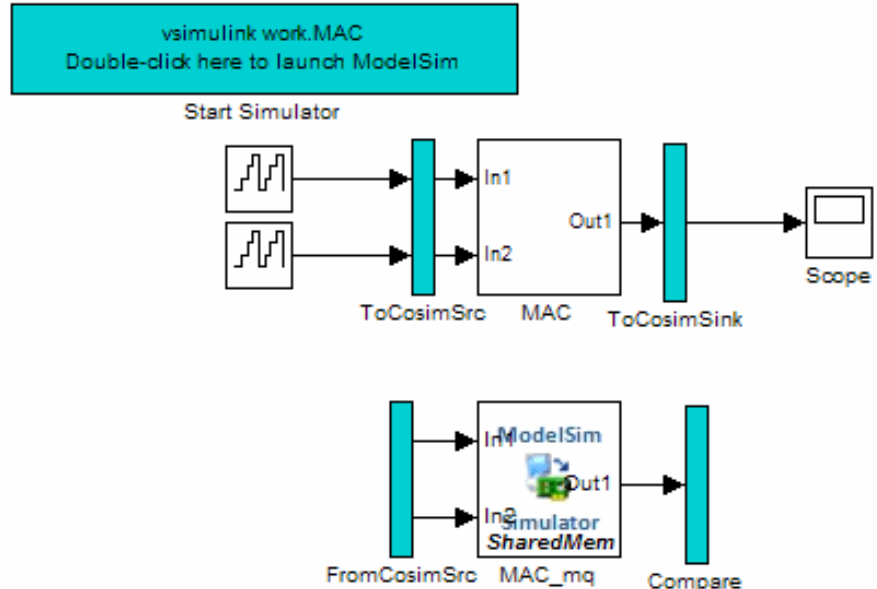
```

### Begin TestBench Generation
### Generating new cosimulation model: gm_hdl_cosim_demo1_mq0.mdl
### Generating new cosimulation tcl script: hdlsrc/gm_hdl_cosim_demo1_mq0_tcl.m
### Cosimulation Model Generation Complete.

### Generating Test bench: hdlsrc\MAC_tb.vhd
### Please wait ...
### HDL TestBench Generation Complete.

```

When test bench generation completes, the coder opens the generated cosimulated model. The following figure shows the generated model.



- 2 Save the generated model. The generated model exists only in memory unless you save it.

As indicated by the code generation messages, the coder generates the following files in addition to the usual HDL test bench file:

- A cosimulation model (gm\_hdl\_cosim\_demo1\_mq)

- A file that contains a TCL cosimulation script and information about settings of the cosimulation model (`gm_hdl_cosim_demo1_mq_tcl.m`)

Generated file names derive from the model name, as described in “Naming Conventions for Generated Cosimulation Models and Scripts” on page 15-52.

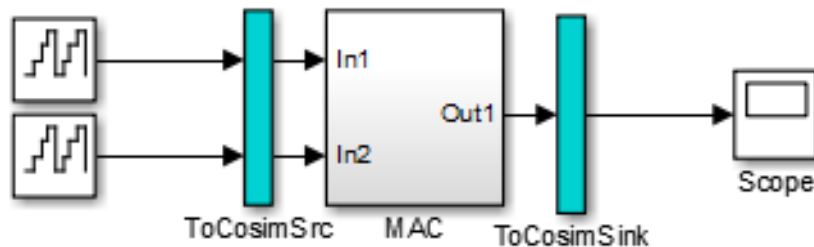
The next section, “Structure of the Generated Model” on page 15-37, describes the features of the model. Before running a cosimulation, become familiar with these features.

## Structure of the Generated Model

You can set up and launch a cosimulation using controls located in the generated model. This section examines the model generated from the example MAC subsystem.

### Simulation Path

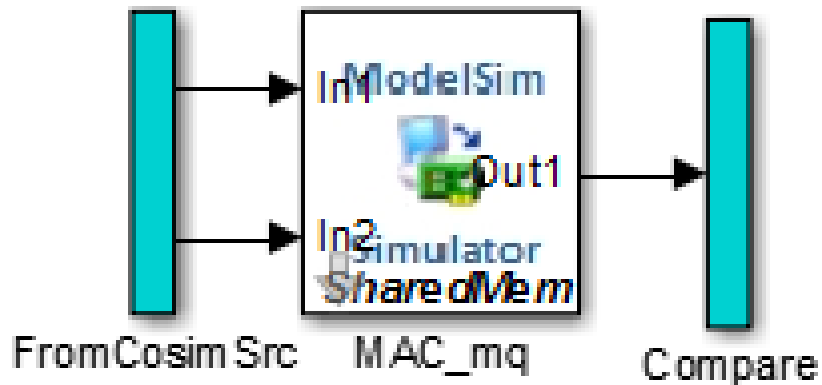
The model comprises two parallel signal paths. The *simulation path*, located in the upper half of the model window, is nearly identical to the original DUT. The purpose of the simulation path is to execute a normal Simulink simulation and provide a reference signal for comparison to the cosimulation results. The following figure shows the simulation path.



The two subsystems labelled `ToCosimSrc` and `ToCosimSink` do not change the performance of the simulation path. Their purpose is to capture stimulus and response signals of the DUT and route them to and from the HDL cosimulation block (see “Signal Routing Between Simulation and Cosimulation Paths” on page 15-40).

### Cosimulation Path

The *cosimulation path*, located in the lower half of the model window, contains the generated HDL Cosimulation block. The following figure shows the cosimulation path.

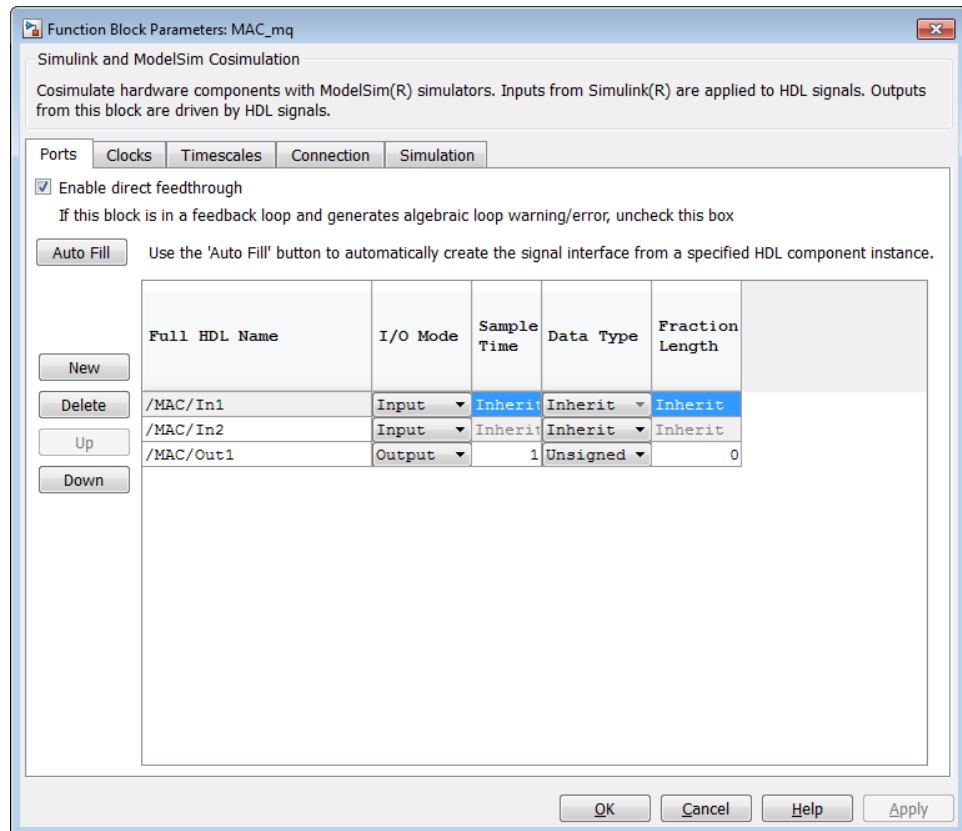


The `FromCosimSrc` subsystem receives the same input signals that drive the DUT. In the `gm_hdl_cosim_demo1_mq0` model, the subsystem simply passes the inputs on to the HDL Cosimulation block. Signals of some other data types require further processing at this stage (see “Signal Routing Between Simulation and Cosimulation Paths” on page 15-40).

The `Compare` subsystem at the end of the cosimulation path compares the cosimulation output to the reference output produced by the simulation path. If the comparison detects a discrepancy, an Assertion block in the `Compare` subsystem displays a warning message. If desired, you can disable assertions and control other operations of the `Compare` subsystem. See “Controlling Assertions and Scope Displays” on page 15-42 for details.

The coder populates the HDL Cosimulation block with the compiled I/O interface of the DUT. The following figure shows the **Ports** pane of the `Mac_mq` HDL Cosimulation block.





The coder sets the **Full HDL Name**, **Sample Time**, **Data Type**, and other fields as required by the model. The coder also configures other HDL Cosimulation block parameters under the **Timescales** and **Tcl** panes.

---

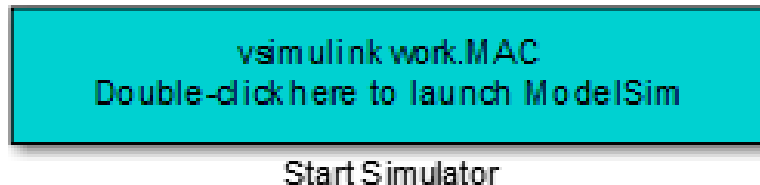
**Tip** The coder configures the generated HDL Cosimulation block for the Shared Memory connection method.

---

### Start Simulator Control

When you double-click the Start Simulator control, it launches the selected cosimulation tool and passes in a startup command to the tool. The Start

Simulator icon displays the startup command, as shown in the following figure.

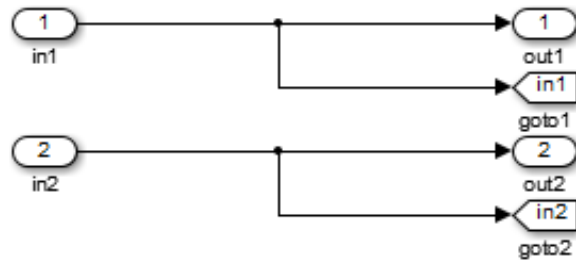


The commands executed when you double-click the Start Simulator icon launch and set up the cosimulation tool, but they do not start the actual cosimulation. “Launching a Cosimulation” on page 15-44 describes how to run a cosimulation with the generated model.

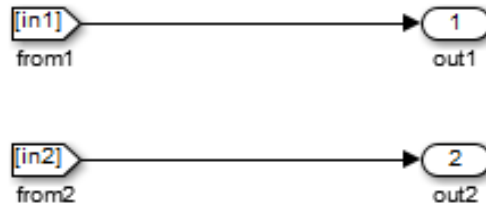
### **Signal Routing Between Simulation and Cosimulation Paths**

The generated model routes signals between the simulation and cosimulation paths using Goto and From blocks. For example, the Goto blocks in the ToCosimSrc subsystem route each DUT input signal to a corresponding From block in the FromCosimSrc subsystem. The following figures show the Goto and From blocks in each subsystem.

gm\_hdl\_cosim\_demo1\_mq ▶ ToCosimSrc



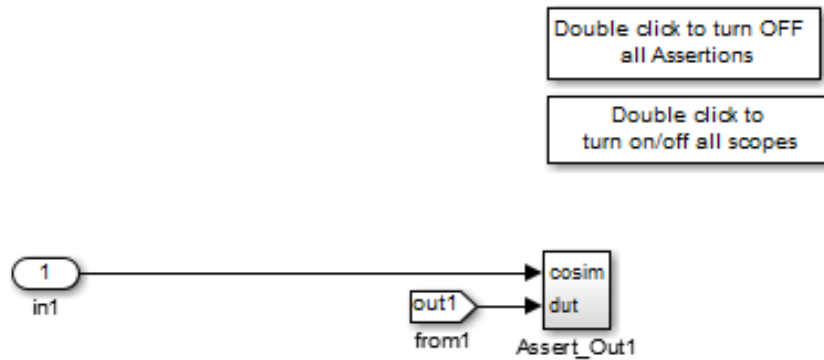
gm\_hdl\_cosim\_demo1\_mq ▶ FromCosimSrc



The preceding figures show simple scalar inputs. Signals of complex and vector data types require further processing. See “Complex and Vector Signals in the Generated Cosimulation Model” on page 15-49 for further information.

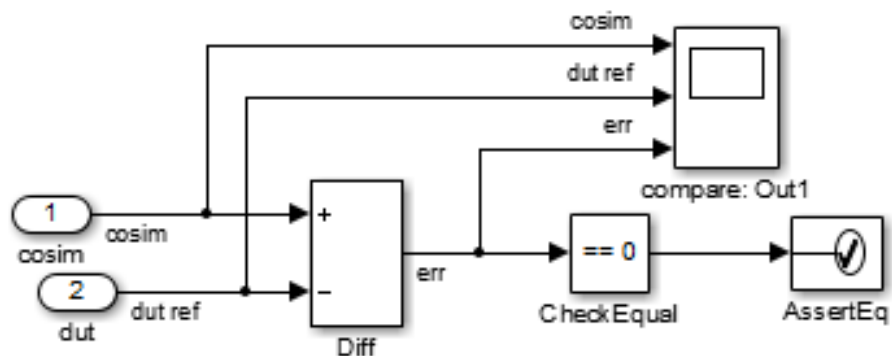
## Controlling Assertions and Scope Displays

The Compare subsystem lets you control the display of signals on scopes, and warning messages from assertions. The following figure shows the Compare subsystem for the gm\_hdl\_cosim\_demo1\_mq0 model.



For each output of the DUT, the coder generates an assertion checking subsystem (Assert\_Out $N$ ). The subsystem computes the difference (err) between the original DUT output (dut ref) and the corresponding cosimulation output (cosim). The subsystem routes the comparison result to an Assertion block. If the comparison result is not zero, the Assertion block reports the discrepancy.

The following figure shows the Assert\_Out1 subsystem for the gm\_hdl\_cosim\_demo1\_mq0 model.



This subsystem also routes the `dut_ref`, `cosim`, and `err` signals to a Scope for display at the top level of the model.

By default, the generated cosimulation model enables all assertions and displays all Scopes. Use the buttons on the Compare subsystem to disable assertions or hide Scopes.

---

**Tip** Assertion messages are warnings and do not stop simulation.

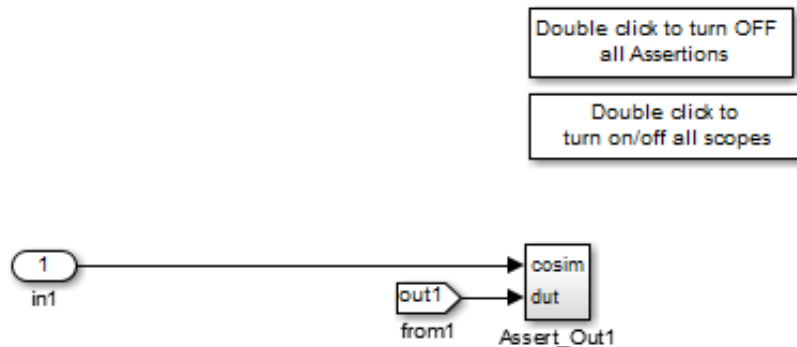
---

## Launching a Cosimulation

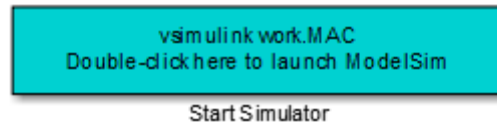
To run a cosimulation with the generated model:

- 1 Double-click the Compare subsystem to configure Scopes and assertion settings.

If you want to disable Scope displays or assertion warnings before starting your cosimulation, use the buttons on the Compare subsystem (shown in the following figure).



- 2 Double-click the Start Simulator control.



The Start Simulator control launches your HDL simulator (in this case, HDL Verifier for use with Mentor Graphics ModelSim).

The HDL simulator in turn executes a startup script. In this case the startup script consists of the TCL commands located in `gm_hdl_cosim_demo1_mq0_tcl.m`. When the HDL simulator finishes executing the startup script, it displays a message like the following.

```
# Ready for cosimulation...
```

**3** In the Simulink Editor for the generated model, start simulation.

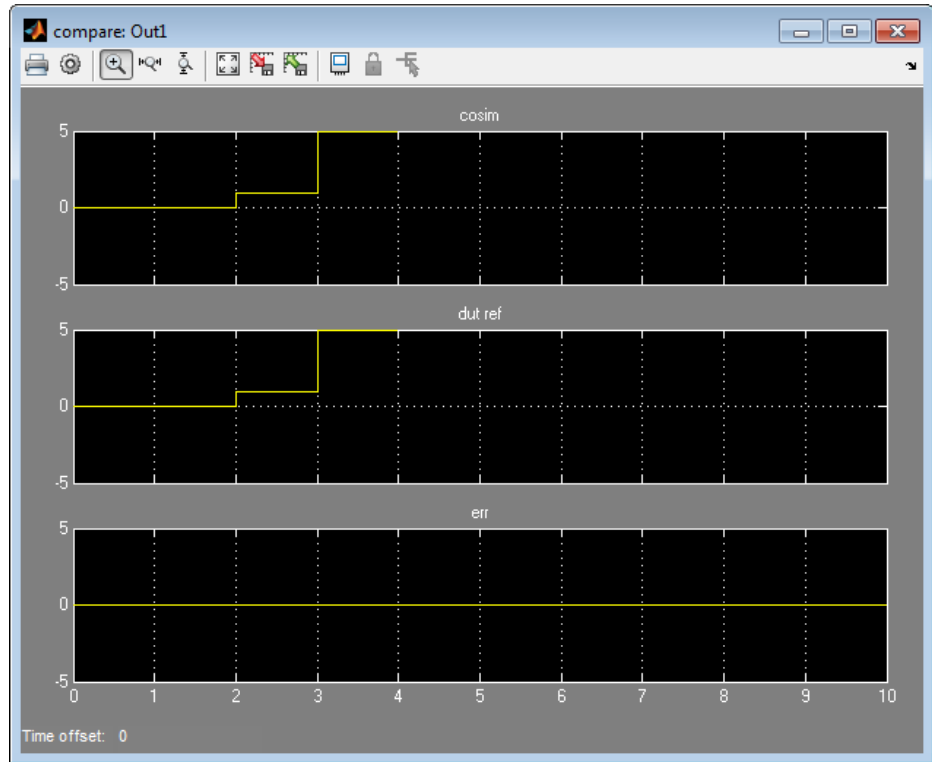
As the cosimulation runs, the HDL simulator displays messages like the following.

```
# Running Simulink Cosimulation block.
# Chip Name: --> hdl_cosim_demo1/MAC
# Target language: --> vhd1
# Target directory: --> hdlsrc
# Fri Jun 05 4:26:34 PM Eastern Daylight Time 2009
# Simulation halt requested by foreign interface.
# done
```

At the end of the cosimulation, if you have enabled Scope displays, the compare scope displays the following signals:

- `cosim`: The result signal output by the HDL Cosimulation block.
- `dut ref`: The reference output signal from the DUT.
- `err`: The difference (error) between these two outputs.

The following figure shows these signals.



## The Cosimulation Script File

The generated script file has two sections:

- A comment section that documents model settings that are relevant to cosimulation.
- A function that stores several lines of TCL code into a variable, `tc1Cmds`. The cosimulation tools execute these commands when you launch a cosimulation.

## Header Comments Section

The following listing shows the comment section of a script file generated for the `hdl_cosim_demo1` model:



```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Auto generated cosimulation 'tclstart' script
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Source Model      : hdl_cosim_demo1.mdl
% Generated Model   : gm_hdl_cosim_demo1.mdl
% Cosimulation Model : gm_hdl_cosim_demo1_mq.mdl
%
% Source DUT       : gm_hdl_cosim_demo1_mq/MAC
% Cosimulation DUT : gm_hdl_cosim_demo1_mq/MAC_mq
%
% File Location    : hdlsrc/gm_hdl_cosim_demo1_mq_tcl.m
% Created          : 2009-06-16 10:51:01
%
% Generated by MATLAB 7.9 and HDL Coder 1.6
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% ClockName        : clk
% ResetName        : reset
% ClockEnableName  : clk_enable
%
% ClockLowTime     : 5ns
% ClockHighTime    : 5ns
% ClockPeriod      : 10ns
%
% ResetLength      : 20ns
% ClockEnableDelay : 10ns
% HoldTime         : 2ns
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% ModelBaseSampleTime : 1
% OverClockFactor      : 1
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Mapping of DutBaseSampleTime to ClockPeriod
%
% 
$$N = (\text{ClockPeriod} / \text{DutBaseSampleTime}) * \text{OverClockFactor}$$

% 1 sec in Simulink corresponds to 10ns in the HDL
```

```

% Simulator(N = 10)
%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% ResetHighAt      : (ClockLowTime + ResetLength + HoldTime)
% ResetRiseEdge    : 27ns
% ResetType        : async
% ResetAssertedLevel : 1
%
% ClockEnableHighAt : (ClockLowTime + ResetLength + ClockEnableDelay + HoldTime)
% ClockEnableRiseEdge : 37ns
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

```

The comments section comprises the following subsections:

- *Header comments*: This section documents the files names for the source and generated models and the source and generated DUT.
- *Test bench settings*: This section documents the makehdltb property values that affect cosimulation model generation. The generated TCL script uses these values to initialize the cosimulation tool.
- *Sample time information*: The next two sections document the base sample time and oversampling factor of the model. The coder uses ModelBaseSampleTime and OverClockFactor to map the clock period of the model to the HDL cosimulation clock period.
- *Clock, clock enable, and reset waveforms*: This section documents the computations of the duty cycle of the clk, clk\_enable, and reset signals.

## TCL Commands Section

The following listing shows the TCL commands section of a script file generated for the hdl\_cosim\_demo1 model:

```

function tclCmds = gm_hdl_cosim_demo1_mq_tcl
tclCmds = {
    'do MAC_compile.do',...% Compile the generated code
    'vsimulink work.MAC',...% Initiate cosimulation
    'add wave /MAC/clk',...% Add wave commands for chip input signals
    'add wave /MAC/reset',...

```

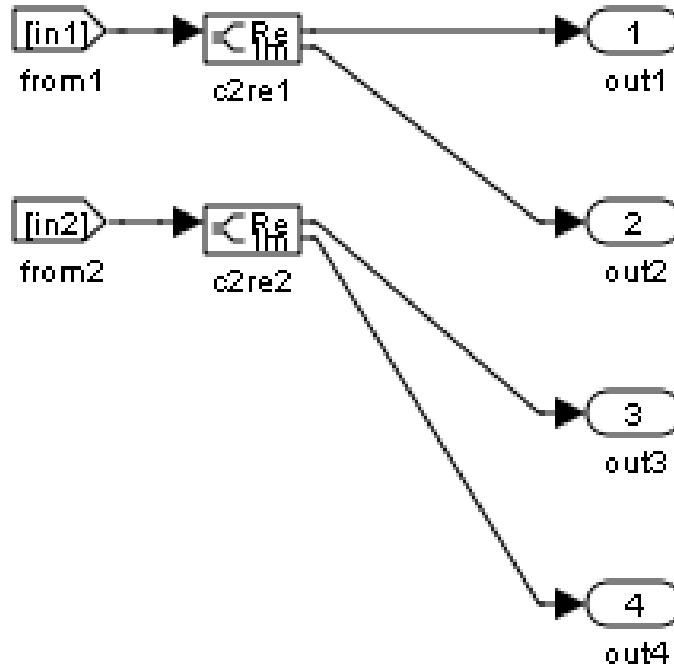
```
'add wave /MAC/c1k_enable',...
'add wave /MAC/In1',...
'add wave /MAC/In2',...
'add wave /MAC/ce_out',...% Add wave commands for chip output signals
'add wave /MAC/Out1',...
'set UserTimeUnit ns',...% Set simulation time unit
'puts "",...
'puts "Ready for cosimulation..."',...
};
end
```

## Complex and Vector Signals in the Generated Cosimulation Model

Input signals of complex or vector data types require insertion of additional elements into the cosimulation path. this section describes these elements.

### Complex Signals

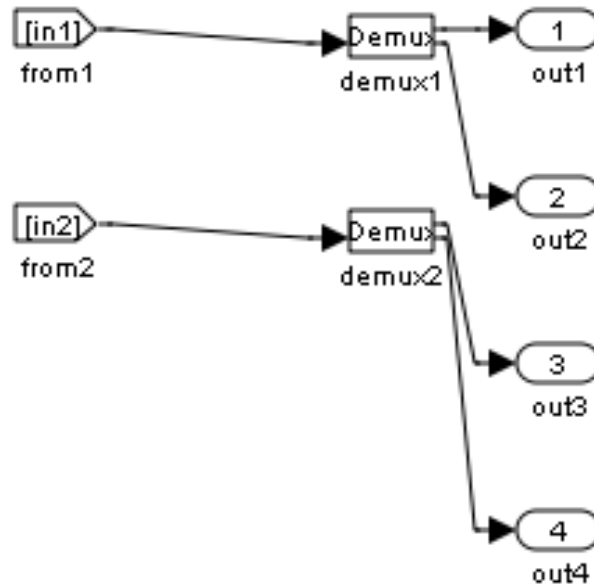
The generated cosimulation model automatically breaks complex inputs into real and imaginary parts. The following figure shows a FromCosimSrc subsystem that receives two complex input signals. The subsystem breaks the inputs into real and imaginary parts before passing them to the subsystem outputs.



The model maintains the separation of real and imaginary components throughout the cosimulation path. The Compare subsystem performs separate comparisons and separate scope displays for the real and imaginary signal components.

### Vector Signals

The generated cosimulation model flattens vector inputs. The following figure shows a FromCosimSrc subsystem that receives two vector input signals of dimension 2. The subsystem flattens the inputs into scalars before passing them to the subsystem outputs.



## Generating a Cosimulation Model from the Command Line

To generate a cosimulation model from the command line, pass the `GenerateCosimModel` property to the `makehdltb` function. `GenerateCosimModel` takes one of the following property values:

- `'ModelSim'`: generate a cosimulation model configured for HDL Verifier for use with Mentor Graphics ModelSim.
- `'Incisive'`: generate a cosimulation model configured for HDL Verifier for use with Cadence Incisive.

In the following command, `makehdltb` generates a cosimulation model configured for HDL Verifier for use with Mentor Graphics ModelSim.

```
makehdltb('hdl_cosim_demo1/MAC', 'GenerateCosimModel', 'ModelSim');
```

## Naming Conventions for Generated Cosimulation Models and Scripts

The naming convention for generated cosimulation models is

`prefix_modelname_toolid_suffix`, where:

- `prefix` is the string `gm`.
- `modelname` is the name of the generating model.
- `toolid` is an identifier indicating the HDL simulator chosen by the **Cosimulation model for use with:** option. Valid `toolid` strings are `'mq'` and `'in'`.
- `suffix` is an integer that provides each generated model with a unique name. The suffix increments with each successive test bench generation for a given model. For example, if the original model name is `test`, then the sequence of generated cosimulation model names is `gm_test_toolid_0`, `gm_test_toolid_1`, and so on.

The naming convention for generated cosimulation scripts is the same as that for models, except that the file name extension is `.m`.

## Limitations for Cosimulation Model Generation

When you configure a model for cosimulation model generation, observe the following limitations:

- Explicitly specify the sample times of source blocks to the DUT in the simulation path. Use of the default sample time (`-1`) in the source blocks may cause sample time propagation problems in the cosimulation path of the generated model.
- The coder does not support continuous sample times for cosimulation model generation. Do not use sample times `0` or `Inf` in source blocks in the simulation path.
- Combinatorial output paths (caused by absence of registers in the generated code) have a latency of one extra cycle in cosimulation. This causes a one cycle discrepancy in the comparison between the simulation and cosimulation outputs. To avoid this discrepancy, the **Enable direct feedthrough for HDL design with pure combinational datapath**

option on the **Ports** pane of the HDL Cosimulation block is automatically selected. For more information, see “Direct Feedthrough Cosimulation”.

Alternatively, you can avoid the latency by specifying output pipelining (see “OutputPipeline” on page 9-85). This will fully register outputs during code generation.

- Double data types are not supported for the HDL Cosimulation block. Avoid use of double data types in the simulation path when generating HDL code and a cosimulation model.

## Customize the Generated Interface

You can customize port names and set attributes of the external component when you generate an interface from the following block types:

- Model
- Subsystem
- HDL Cosimulation

Open the HDL Properties dialog box to see the interface generation parameters.

The following table summarizes the names, value settings, and purpose of the interface generation parameters.

Parameter Name	Values	Description
AddClockEnablePort	'on'   'off' Default: 'on'	If 'on', add a clock enable input port to the interface generated for the block. The name of the port is specified by <code>ClockEnableInputPort</code> .
AddClockPort	'on'   'off' Default: 'on'	If 'on', add a clock input port to the interface generated for the block. The name of the port is specified by <code>ClockInputPort</code> .
AddResetPort	'on'   'off' Default: 'on'	If 'on', add a reset input port to the interface generated for the block. The name of the port is specified by <code>ResetInputPort</code> .
AllowDistributedPipelining	'on'   'off' Default: 'off'	If 'on', allow the coder to move registers across the block, from input to output or output to input.
ClockEnableInputPort	Default: 'clk_enable'	Specifies HDL name for block's clock enable input port.



Parameter Name	Values	Description
ClockInputPort	Default: 'clk'	Specifies HDL name for block's clock input signal.
EntityName	Default: Entity name string is derived from the block name, and modified when necessary to generate a legal VHDL entity name.	Specifies VHDL entity or Verilog module name generated for the block.
GenericList	Default: An empty cell array of string data.  Each element of the cell array is another cell array of the form {'Name', 'Value', 'Type'}, where 'Type' is optional. If you omit 'Type', 'integer' is passed as the data type.	Specifies a list of parameter/value pairs (with optional data type specification) in string format to pass to a subsystem with a BlackBox implementation.
ImplementationLatency	-1   0   positive integer  Default: -1	Specifies the additional latency of the external component in time steps, relative to the Simulink block.  If 0 or greater, this value is used for delay balancing. Your inputs and outputs must operate at the same rate.  If -1, latency is unknown. This disables delay balancing.
InlineConfigurations (VHDL only)	'on'   'off'  Default: If this parameter is unspecified, defaults to the value of the global InlineConfigurations property.	If 'off', suppress generation of a configurations for the block, and require a user-supplied external configuration.

<b>Parameter Name</b>	<b>Values</b>	<b>Description</b>
InputPipeline	Default: '0'	Specifies the number of input pipeline stages (pipeline depth) in the generated code.
OutputPipeline	Default: '0'	Specifies the number of output pipeline stages (pipeline depth) in the generated code.
ResetInputPort	Default: 'reset'	Specifies HDL name for block's reset input.
VHDLArchitectureName (VHDL only)	Default: 'rtl'	Specifies RTL architecture name generated for the block. The architecture name is generated only if InlineConfigurations = 'on'.
VHDLComponentLibrary (VHDL only)	Default: 'work'	Specifies the library from which to load the VHDL component.

## Pass-Through and No-Op Implementations

The coder provides a pass-through or no-op implementation for some blocks. A pass-through implementation generates a wire in the HDL; a no-op implementation omits code generation for the block or subsystem. These implementations are useful in cases where you need a block for simulation, but do not need the block or subsystem in your generated HDL code.

The pass-through and no-op implementations are summarized in the following table.

Implementation	Description
Pass-through implementations	<p>Provides a pass-through implementation in which the block's inputs are passed directly to its outputs. The coder supports the following blocks with a pass-through implementation:</p> <ul style="list-style-type: none"> <li>• Convert 1-D to 2-D</li> <li>• Reshape</li> <li>• Signal Conversion</li> <li>• Signal Specification</li> </ul>
No HDL	<p>This implementation completely removes the block from the generated code. This enables you to use the block in simulation but treat it as a “no-op” in the HDL code. This implementation is used for many blocks (such as Scopes and Assertions) that are significant in simulation but are meaningless in HDL code.</p>

## Limitation on Generated Verilog Interfaces

This section describes a limitation in the current release that applies to generation of Verilog interfaces for the following blocks:

- HDL Verifier HDL Cosimulation blocks
- Model block

When the target language is Verilog, only scalar ports are supported for code generation for these block types. Use of vector ports that are on these blocks are reported as errors in the compatibility checker (`checkhdl`) report, and raise a code generation (`makehdl`) error.

# Stateflow HDL Code Generation Support

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- “Introduction to Stateflow HDL Code Generation” on page 16-2
- “Requirements for Stateflow HDL Code Generation” on page 16-4
- “Map Chart Semantics to HDL” on page 16-9
- “Generate HDL for Mealy and Moore FSMs” on page 16-13
- “Structure a Model for HDL Code Generation” on page 16-24
- “Design Patterns Using Advanced Chart Features” on page 16-25

## Introduction to Stateflow HDL Code Generation

In this section...
“Overview” on page 16-2
“Examples” on page 16-2

### Overview

Stateflow charts provide concise descriptions of complex system behavior using hierarchical finite state machine (FSM) theory, flow diagram notation, and state-transition diagrams.

You use a chart to model a finite state machine or a complex control algorithm intended for realization as an ASIC or FPGA. When the model meets design requirements, you then generate HDL code (VHDL or Verilog) that implements the design embodied in the model. You can simulate and synthesize generated HDL code using industry standard tools, and then map your system designs into FPGAs and ASICs.

In general, generation of VHDL or Verilog code from a model containing a chart does not differ greatly from HDL code generation from other models. The HDL code generator is designed to

- Support the largest possible subset of chart semantics that is consistent with HDL. This broad subset lets you generate HDL code from existing models without significant remodeling effort.
- Generate bit-true, cycle-accurate HDL code that is fully compatible with Stateflow simulation semantics.

### Examples

The following examples, illustrating HDL code generation from subsystems that include Stateflow charts, are available:

- Greatest Common Divisor
- Pipelined Configurable FIR
- 2D FDTD Behavioral Model

- CPU Behavioral Model

To open the example models, open the **Help**, navigate to the HDL Coder documentation, and click **Examples**.

## Requirements for Stateflow HDL Code Generation

### In this section...

“Overview” on page 16-4  
“Location of Charts in the Model” on page 16-4  
“Data Type Usage” on page 16-4  
“Chart Initialization” on page 16-5  
“Registered Output” on page 16-5  
“Restrictions on Imported Code” on page 16-6  
“Using Input and Output Events” on page 16-6  
“Using For Loops” on page 16-6  
“Other Restrictions” on page 16-7

### Overview

This section summarizes the requirements and restrictions you should follow when configuring Stateflow charts that are intended to target HDL code generation. “Map Chart Semantics to HDL” on page 16-9 provides a more detailed rationale for most of these requirements.

### Location of Charts in the Model

A chart intended for HDL code generation must be part of a Simulink subsystem. See “Structure a Model for HDL Code Generation” on page 16-24 for an example.

### Data Type Usage

#### Supported Data Types

The current release supports a subset of MATLAB data types in charts intended for use in HDL code generation. Supported data types are

- Signed and unsigned integer



- Double and single

---

**Note** Results obtained from HDL code generated for models using double or single data types might not be bit-true to results obtained from simulation of the original model.

---

- Fixed point
- Boolean

---

**Note** Multidimensional arrays of these types are supported, with the exception of data types assigned to ports. Port data types must be either scalar or vector.

---

## Chart Initialization

In charts intended for HDL code generation, enable the chart property **Execute (enter) Chart at Initialization**. When this property is enabled, default transitions are tested and actions reachable from the default transition taken are executed. These actions correspond to the reset process in HDL code. “Execution of a Chart at Initialization” describes existing restrictions under this property.

The reset action must not entail the delay of combinatorial logic. Therefore, do not perform arithmetic in initialization actions.

The chart property **Initialize Outputs Every Time Chart Wakes Up** controls whether or not output is persistent.

Selecting **Initialize Outputs Every Time Chart Wakes Up** generates HDL code that is more readable and has better synthesis results.

## Registered Output

If you want to insert an output register that delays the chart output by a simulation cycle, use the OutputPipeline block property.

## Restrictions on Imported Code

A chart intended for HDL code generation must be entirely self-contained. The following restrictions apply:

- Do not call MATLAB functions other than `min` or `max`.
- Do not use MATLAB workspace data.
- Do not call C math functions
- If the **Enable C-like bit operations** property is disabled, do not use the exponentiation operator (^). The exponentiation operator is implemented with the C Math Library function `pow`.
- Do not include custom code. Information entered in the Target Options dialog box is ignored.

## Using Input and Output Events

The coder supports the use of input and output events with Stateflow charts, subject to the following constraints:

- You can define and use one and only one input event per Stateflow chart. (There is no restriction on the number of output events you can use.)
- The coder does not support HDL code generation for charts that have a single input event, and which also have nonzero initial values on the chart's output ports.
- All input and output events must be edge-triggered.

For detailed information on input and output events, see “Using Input Events to Activate a Stateflow Chart” and “Using Output Events to Activate a Simulink Block” in the Stateflow documentation.

## Using For Loops

Do not explicitly use loops other than `for` loops in a chart intended for HDL code generation. Observe the following restrictions on `for` loops:

- The data type of the loop counter variable must be `int32`.
- The coder supports only constant-bounded loops.

The for loop example (sf\_for) illustrates a design pattern for a for loop using a graphical function.

## Other Restrictions

The coder imposes a number of additional restrictions on the use of classic chart features. These limitations exist because HDL does not support some features of general-purpose sequential programming languages.

- Do not define local events in a chart from which HDL code is to be generated.

Do not use the following implicit events:

- enter
- exit
- change

You can use the following implicit events:

- wakeup
- tick

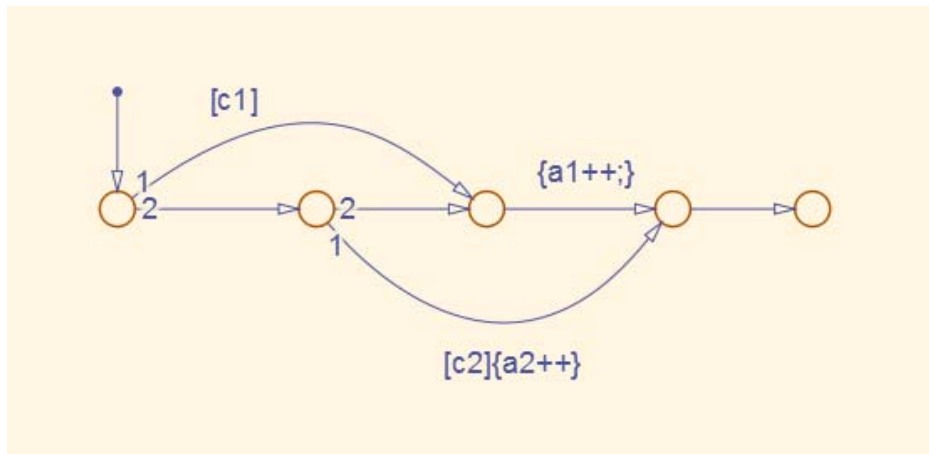
Temporal logic can be used provided the base events are limited to these types of implicit events.

---

**Note** Absolute-time temporal logic is not supported for HDL code generation.

---

- Do not use recursion through graphical functions. The coder does not currently support recursion.
- HDL does not support a goto statement. Therefore, do not use unstructured flow diagrams, such as the flow diagram shown in the following figure.



- Do not read from output ports if you do not have the **Initialize Outputs Every Time Chart Wakes Up** chart option selected.
- Do not use Data Store Memory objects.
- Do not use pointer (&) or indirection (\*) operators. See the discussion of “Pointer and Address Operations”.
- If a chart gets a runtime overflow error during simulation, it is possible to disable data range error checking and generate HDL code for the chart. However, in such cases results obtained from the generated HDL code might not be bit-true to results obtained from the simulation. Recommended practice is to enable overflow checking and eliminate overflow conditions from the model during simulation.

## Map Chart Semantics to HDL

In this section...
“Hardware Realization of Stateflow Semantics” on page 16-9
“Restrictions for HDL Realization” on page 16-11

### Hardware Realization of Stateflow Semantics

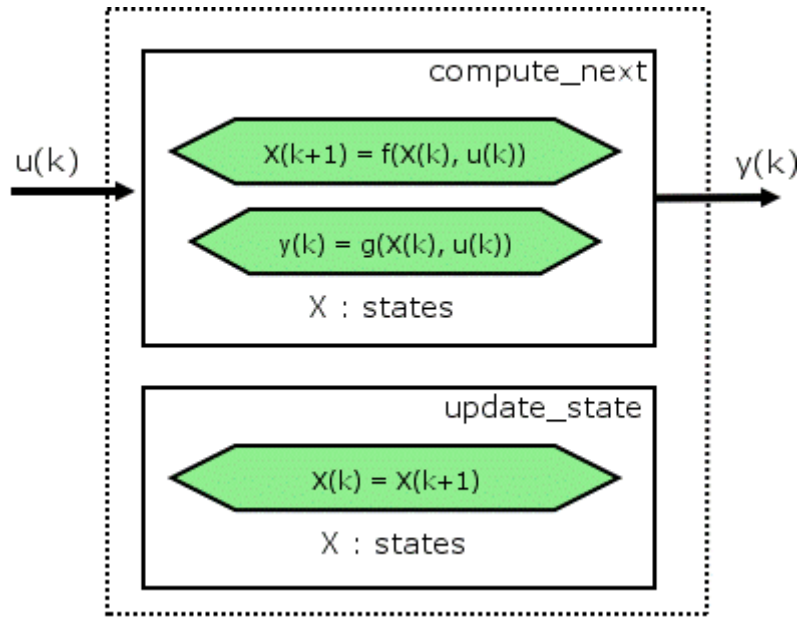
A mapping from Stateflow semantics to an HDL implementation has the following requirements:

- **Requirement 1:** Hardware designs require separability of output and state update functions.
- **Requirement 2:** HDL is a concurrent language. To achieve the goal of bit-true simulation, execution must be in order.

To meet Requirement 1, an FSM is coded in HDL as two concurrent blocks that execute under different conditions. One block evaluates the transition conditions, computes outputs and speculatively computes the next state variables. The other block updates the current state variables from the available next state and performs the actual state transitions. This second block is activated only on the trigger edge of the clock signal, or an asynchronous reset signal.

In practice, output computations usually occur more often than state updates. The presence of inputs drives the computation of outputs. State transitions occur at regular intervals (whenever the chart is activated).

The following diagram shows a concurrent implementation of Stateflow semantics for output and update computations, intended for targeting HDL.



The HDL code generator reuses the original single-function implementation of Stateflow semantics almost without modification. There is one important difference: instead of computing with state variables directly, state computations are performed on local shadow variables. These variables are local to the HDL function `update_chart`. At the beginning of the `update_chart` functions, `current_state` is copied into the shadow variables. At the end of the `update_chart` function, the newly computed state is transferred to registers called collectively `next_state`. The values held in these registers are copied to `current_state` (also registered) when `update_state` is called.

By using local variables, this approach maps Stateflow sequential semantics to HDL sequential statements, avoiding the use of concurrent statements. For instance, local chart variables in function scope map to VHDL variables in process scope. In VHDL, variable assignment is sequential. Therefore, statements in a Stateflow function that uses local variables can map to statements in a VHDL process that uses corresponding variables. The VHDL assignments execute in the same order as the assignments in the Stateflow function.

## Restrictions for HDL Realization

Some restrictions on chart usage are required to achieve a valid mapping from a chart to HDL code. These are summarized briefly in “Requirements for Stateflow HDL Code Generation” on page 16-4. The following sections give a more detailed rationale for most of these restrictions.

### Self-Contained Charts

The Stateflow C target allows generated code to have some dependencies on code or data that is external to the chart. Stateflow charts intended for HDL code generation, however, must be self-contained. Observe the following rules for creating self-contained charts:

- Do not use C math functions such as `sin` and `pow`. There is no HDL counterpart to the C math library.
- Do not use calls to functions coded in a language other than HDL. For example, do not call MATLAB functions for a simulation target, as in the following statement:

```
ml disp( hello )
```

- Do not use custom code. There is no mechanism for embedding external HDL code into generated HDL code. Custom C code (user-written C code intended for linkage with C code generated from a Stateflow chart) is ignored during HDL code generation.

See also “External Component Interfaces”.

- Do not use pointer (`&`) or indirection (`*`) operators. Pointer and indirection operators have no function in a chart in the absence of custom code. Also, pointer and indirection operators do not map directly to synthesizable HDL.
- Do not share data (via Data Store Memory blocks) between charts. The coder does not map such global data to HDL, because HDL does not support global data.

### Charts Must Not Use Features Unsupported by HDL

When creating charts intended for HDL code generation, follow these guidelines to avoid using Stateflow features that cannot be mapped to HDL:

- Avoid recursion. While charts permit recursion (through both event processing and user-written recursive graphical functions), HDL does not allow recursion.
- Do not use Stateflow and local events. These event types do not have equivalents in HDL. Therefore, these event types are not supported for HDL code generation.
- Avoid unstructured code. Although charts allow unstructured code to be written (through transition flow diagrams and graphical functions), this usage results in `goto` statements and multiple function return statements. HDL does not support either `goto` statements or multiple function return statements.
- Select the **Execute (enter) Chart At Initialization** chart property. This option executes the update chart function immediately following chart initialization. The option is required for HDL because outputs must be available at time 0 (hardware reset). You must select this option for bit-true HDL code generation.



## Generate HDL for Mealy and Moore FSMs

In this section...
“Overview” on page 16-13
“Generating HDL for a Mealy Finite State Machine” on page 16-14
“Generating HDL Code for a Moore Finite State Machine” on page 16-18

### Overview

Stateflow charts support modeling of three types of state machines:

- Classic (default)
- Mealy
- Moore

This section discusses issues you should consider when generating HDL code for Mealy and Moore state machines.

Mealy and Moore state machines differ in the following ways:

- The outputs of a Mealy state machine are a function of the current state and inputs.
- The outputs of a Moore state machine are a function of the current state only.

Moore and Mealy state charts can be functionally equivalent; an equivalent Mealy chart can derive from a Moore chart, and vice versa. A Mealy state machine has a richer description and usually requires a smaller number of states.

The principal advantages of using Mealy or Moore charts as an alternative to Classic charts are:

- At compile time, Mealy and Moore charts are validated for conformance to their formal definitions and semantic rules, and violations are reported.

- Moore charts generate more efficient code than Classic charts, for both C and HDL targets.

The execution of a Mealy or Moore chart at time  $t$  is the evaluation of the function represented by that chart at time  $t$ . The initialization property for output defines every output at every time step. Specifically, the output of a Mealy or Moore chart at one time step must not depend on the output of the chart at an earlier time step.

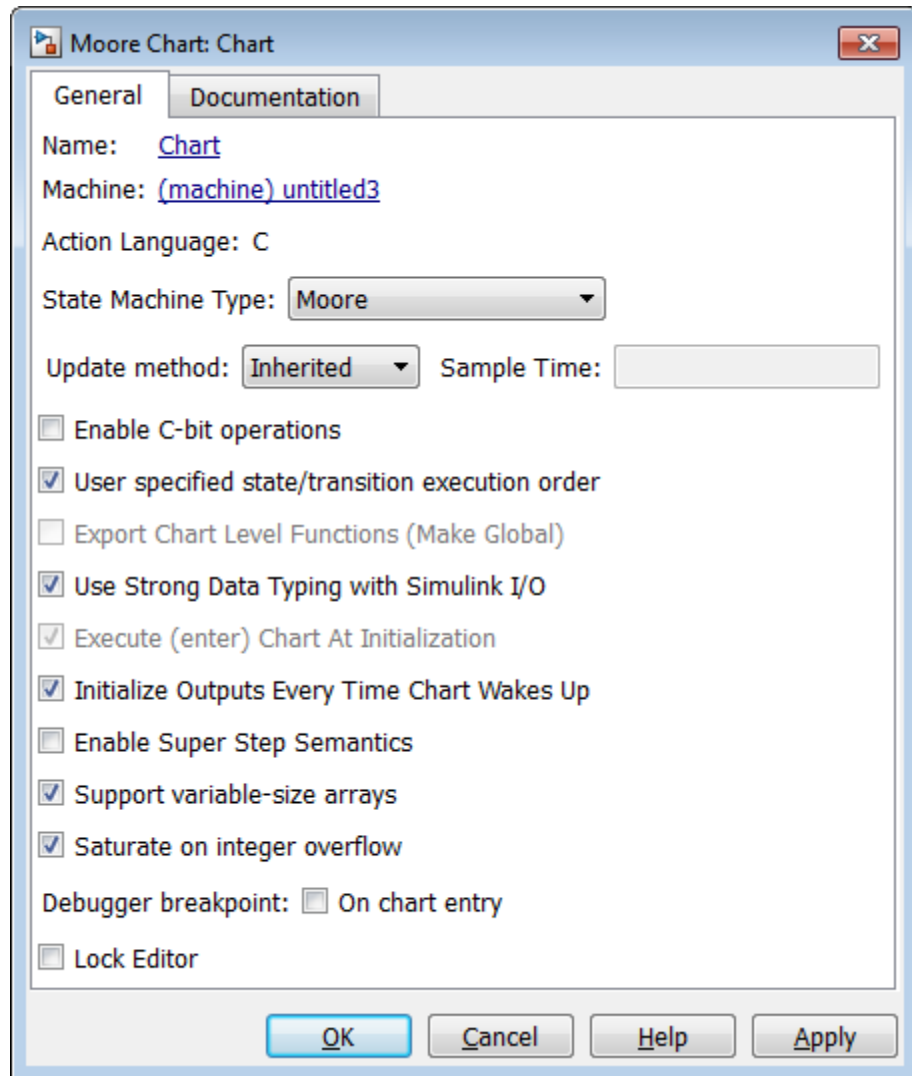
Consider the outputs of a chart. Stateflow charts permit output latching. That is, the value of an output computed at time  $t$  persists until time  $t+d$ , when it is overwritten. The output latching feature corresponds to registered outputs. Therefore, Mealy and Moore charts intended for HDL code generation should not use registered outputs.

### **Generating HDL for a Mealy Finite State Machine**

When generating HDL code for a chart that models a Mealy state machine, make sure that:

- The chart meets the general code generation requirements, as described in “Requirements for Stateflow HDL Code Generation” on page 16-4.
- Actions are associated with inner and outer transitions only.

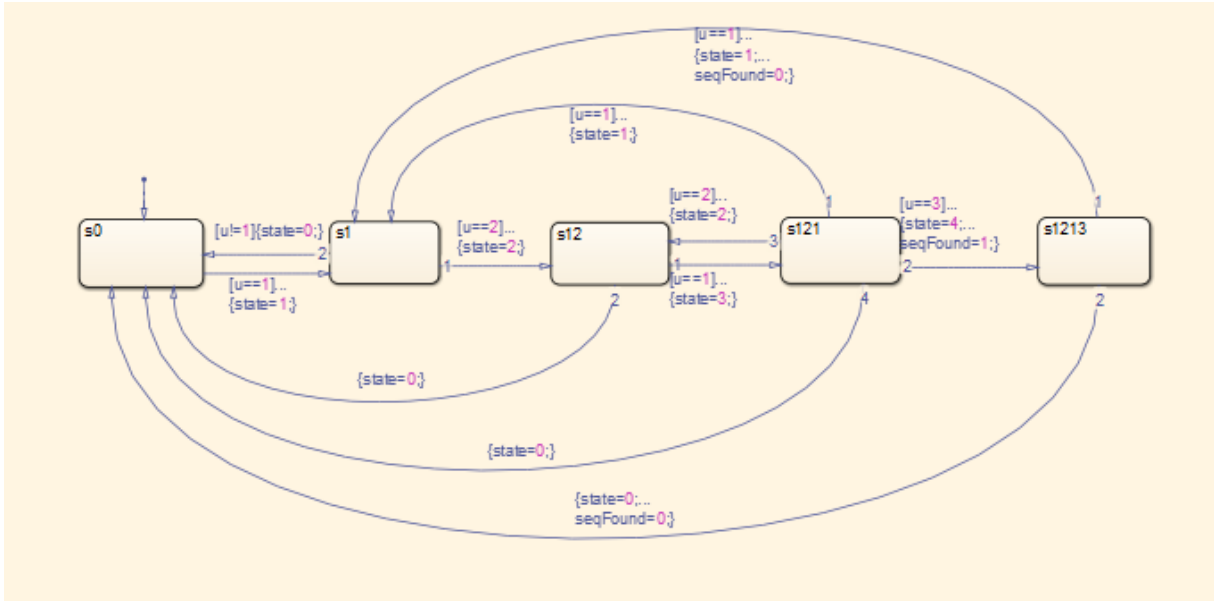
In addition, for better synthesis results and more readable HDL code, we recommend selecting the chart property **Initialize Outputs Every Time Chart Wakes Up**, as shown in the following figure.



Mealy actions are associated with transitions. In Mealy machines, output computation is expected to be driven by the change on inputs. In fact, the dependence of output on input is the fundamental distinguishing factor between the formal definitions of Mealy and Moore machines. The requirement that actions be given on transitions is to some degree stylistic,

rather than required, to enforce Mealy semantics. However, it is natural that output computation follows input conditions on input, because transition conditions are primarily input conditions in any machine type.

The following figure shows an example of a chart that models a Mealy state machine.



The following code example lists the Verilog code generated for the Mealy chart.

```

always @(posedge clk or posedge reset)
begin : MealyChart_1_process
  if (reset == 1'b1) begin
    is_MealyChart <= IN_s0;
  end
  else begin
    if (enb) begin
      is_MealyChart <= is_MealyChart_next;
    end
  end
end

```

```
end

always @* begin
  is_MealyChart_next = is_MealyChart;
  seqFound_1 = 1'b0;
  state_1 = 0.0;

  case ( is_MealyChart)
    IN_s0 :
      begin
        if (u_double == 1.0) begin
          state_1 = 1.0;
          is_MealyChart_next = IN_s1;
        end
      end
    IN_s1 :
      begin
        if (u_double == 2.0) begin
          state_1 = 2.0;
          is_MealyChart_next = IN_s12;
        end
        else if (u_double != 1.0) begin
          state_1 = 0.0;
          is_MealyChart_next = IN_s0;
        end
      end
    IN_s12 :
      begin
        if (u_double == 1.0) begin
          state_1 = 3.0;
          is_MealyChart_next = IN_s121;
        end
        else begin
          state_1 = 0.0;
          is_MealyChart_next = IN_s0;
        end
      end
    IN_s121 :
      begin
        if (u_double == 1.0) begin
```

```
        state_1 = 1.0;
        is_MealyChart_next = IN_s1;
    end
    else if (u_double == 3.0) begin
        state_1 = 4.0;
        seqFound_1 = 1'b1;
        is_MealyChart_next = IN_s1213;
    end
    else if (u_double == 2.0) begin
        state_1 = 2.0;
        is_MealyChart_next = IN_s12;
    end
    else begin
        state_1 = 0.0;
        is_MealyChart_next = IN_s0;
    end
end
default :
begin
    if (u_double == 1.0) begin
        state_1 = 1.0;
        seqFound_1 = 1'b0;
        is_MealyChart_next = IN_s1;
    end
    else begin
        state_1 = 0.0;
        seqFound_1 = 1'b0;
        is_MealyChart_next = IN_s0;
    end
end
endcase

end
```

## Generating HDL Code for a Moore Finite State Machine

When generating HDL code for a chart that models a Moore state machine, make sure that:

- The chart meets the general code generation requirements, as described in “Requirements for Stateflow HDL Code Generation” on page 16-4.
- Actions occur in states only. These actions are unlabeled, and execute when exiting the states or remaining in the states.

Moore actions must be associated with states, because output computation must be dependent only on states, not input. Therefore, the current configuration of active states at time step  $t$  determines output. Thus, the single action in a Moore state serves as both during and exit action. If state  $S$  is active when a chart wakes up at time  $t$ , it contributes to the output whether it remains active into time  $t+1$  or not.

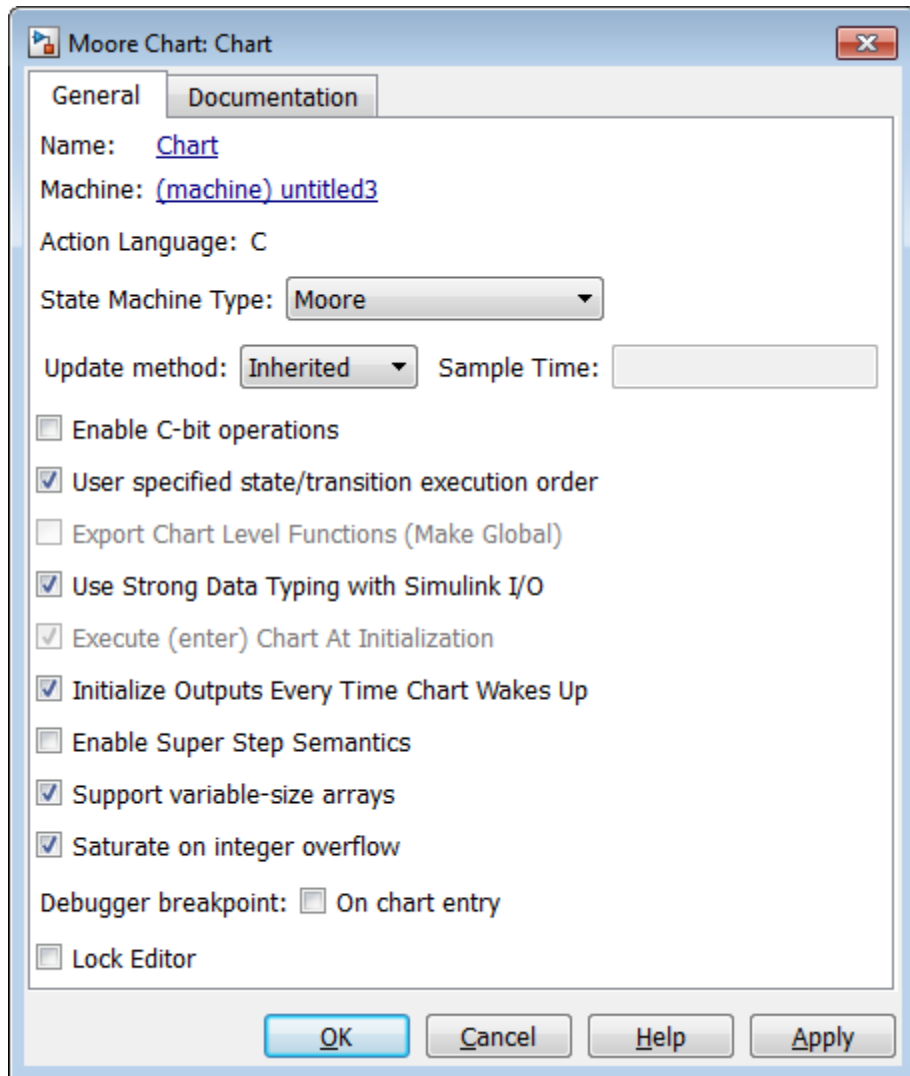
- Local data and graphical functions are not used.

Function calls and local data are not allowed in a Moore chart. This prevents output from depending on input in ways that would be difficult for the HDL code generator to verify. These restrictions strongly encourage coding practices that separate output and input.

- No references to input occur outside of transition conditions.
- Output computation occurs only in leaf states.

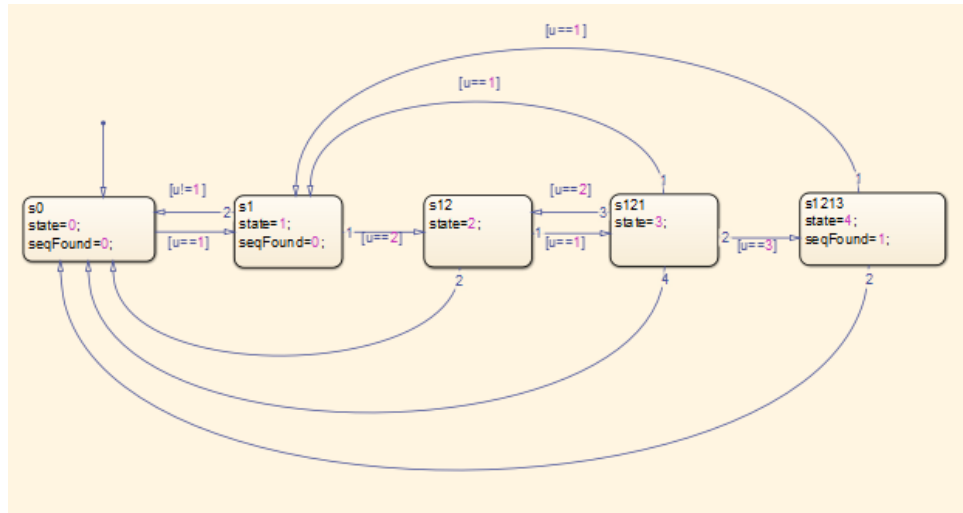
The chart’s top-down semantics compute outputs as if actions were evaluated strictly before inner and outer flow diagrams.

In addition, for better synthesis results and more readable HDL code, we recommend selecting the chart property **Initialize Outputs Every Time Chart Wakes Up**, as shown in the following figure.



The following figure shows a Stateflow chart of a Moore state machine.





The following code example illustrates generated VHDL code for the Moore chart.

```

MooreChart_1_process : PROCESS (clk, reset)
BEGIN
  IF reset = '1' THEN
    is_MooreChart <= IN_s0;
  ELSIF clk'EVENT AND clk = '1' THEN
    IF enb = '1' THEN
      is_MooreChart <= is_MooreChart_next;
    END IF;
  END IF;
END PROCESS MooreChart_1_process;

MooreChart_1_output : PROCESS (is_MooreChart, u)
BEGIN
  is_MooreChart_next <= is_MooreChart;
  seqFound <= '0';
  state <= 0.0;

  CASE is_MooreChart IS
    WHEN IN_s0 =>
      state <= 0.0;
  
```

```

        seqFound <= '0';
    WHEN IN_s1 =>
        state <= 1.0;
        seqFound <= '0';
    WHEN IN_s12 =>
        state <= 2.0;
    WHEN IN_s121 =>
        state <= 3.0;
    WHEN OTHERS =>
        state <= 4.0;
        seqFound <= '1';
END CASE;

CASE is_MooreChart IS
    WHEN IN_s0 =>
        IF u = 1.0 THEN
            is_MooreChart_next <= IN_s1;
        END IF;
    WHEN IN_s1 =>
        IF u = 2.0 THEN
            is_MooreChart_next <= IN_s12;
        ELSIF u /= 1.0 THEN
            is_MooreChart_next <= IN_s0;
        END IF;
    WHEN IN_s12 =>
        IF u = 1.0 THEN
            is_MooreChart_next <= IN_s121;
        ELSE
            is_MooreChart_next <= IN_s0;
        END IF;
    WHEN IN_s121 =>
        IF u = 1.0 THEN
            is_MooreChart_next <= IN_s1;
        ELSIF u = 3.0 THEN
            is_MooreChart_next <= IN_s1213;
        ELSIF u = 2.0 THEN
            is_MooreChart_next <= IN_s12;
        ELSE
            is_MooreChart_next <= IN_s0;
        END IF;
END CASE;

```

```
        END IF;
    WHEN OTHERS =>
        IF u = 1.0 THEN
            is_MooreChart_next <= IN_s1;
        ELSE
            is_MooreChart_next <= IN_s0;
        END IF;
    END CASE;

END PROCESS MooreChart_1_output;
```

## Structure a Model for HDL Code Generation

In general, generation of VHDL or Verilog code from a model containing a Stateflow chart does not differ greatly from HDL code generation from other models.

A chart intended for HDL code generation *must* be part of a subsystem that represents the Device Under Test (DUT). The DUT corresponds to the top level VHDL entity or Verilog module for which code is generated, tested and eventually synthesized. The top level Simulink components that drive the DUT correspond to the behavioral test bench.

You may need to restructure your models to meet this requirement. If the chart for which you want to generate code is at the root level of your model, embed the chart in a subsystem and connect the relevant signals to the subsystem inputs and outputs. In most cases, you can do this by simply clicking on the chart and then selecting **Diagram > Subsystem & Model Reference > Create Subsystem from Selection** in the model window.

## Design Patterns Using Advanced Chart Features

In this section...
“Temporal Logic” on page 16-25
“Graphical Function” on page 16-27
“Hierarchy and Parallelism” on page 16-29
“Stateless Charts” on page 16-30
“Truth Tables” on page 16-31

### Temporal Logic

Stateflow temporal logic operators (such as `after`, `before`, or `every`) are Boolean operators that operate on recurrence counts of Stateflow events. Temporal logic operators can appear only in conditions on transitions that originate from states, and in state actions. Although temporal logic does not introduce new events into a Stateflow model, it is useful to think of the change of value of a temporal logic condition as an event. You can use temporal logic operators in many cases where a counter is required. A common use case would be to use temporal logic to implement a time-out counter.

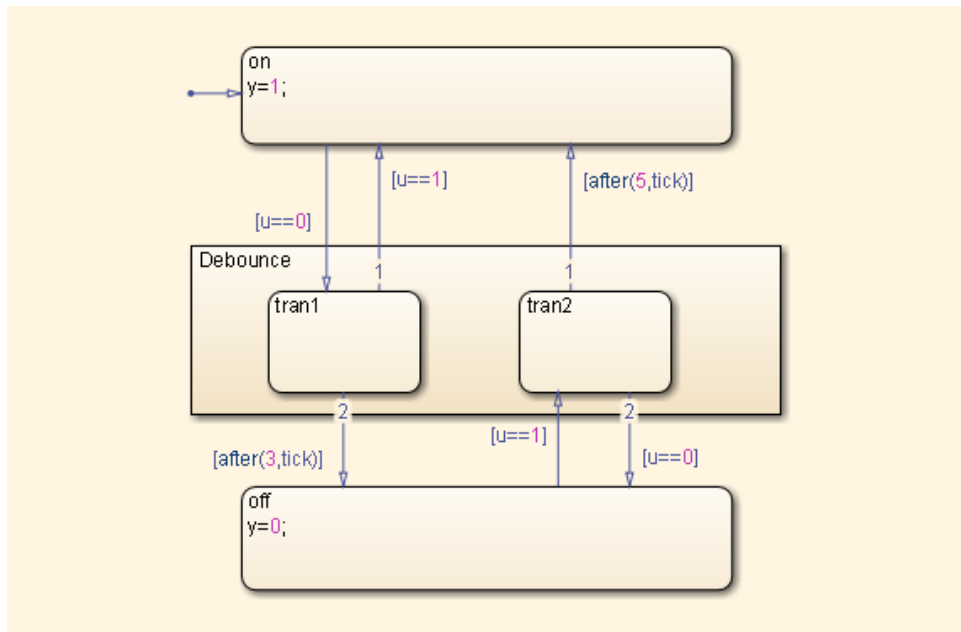
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**Note** Absolute-time temporal logic is not supported for HDL code generation.

---

For detailed information about temporal logic, see “Temporal Logic in State Actions and Transitions”.

The chart shown in the following figure uses temporal logic in a design for a debouncer. Instead of instantaneously switching between `on` and `off` states, the chart uses two intermediate states and temporal logic to ignore transients. The transition is committed based on a time-out.



The following code excerpt shows VHDL code generated from this chart.

```

Chart_1_output : PROCESS (is_Chart, u, temporalCounter_i1, y_reg)
    VARIABLE temporalCounter_i1_temp : unsigned(7 DOWNT0 0);
BEGIN
    temporalCounter_i1_temp := temporalCounter_i1;
    is_Chart_next <= is_Chart;
    y_reg_next <= y_reg;
    IF temporalCounter_i1 < 7 THEN
        temporalCounter_i1_temp := temporalCounter_i1 + 1;
    END IF;

    CASE is_Chart IS
        WHEN IN_tran1 =>
            IF u = 1.0 THEN
                is_Chart_next <= IN_on;
                y_reg_next <= 1.0;
            ELSIF temporalCounter_i1_temp >= 3 THEN
                is_Chart_next <= IN_off;
            END IF;
    END CASE;
END PROCESS;

```

```

        y_reg_next <= 0.0;
    END IF;
    WHEN IN_tran2 =>
        IF temporalCounter_i1_temp >= 5 THEN
            is_Chart_next <= IN_on;
            y_reg_next <= 1.0;
        ELSIF u = 0.0 THEN
            is_Chart_next <= IN_off;
            y_reg_next <= 0.0;
        END IF;
    WHEN IN_off =>
        IF u = 1.0 THEN
            is_Chart_next <= IN_tran2;
            temporalCounter_i1_temp := to_unsigned(0, 8);
        END IF;
    WHEN OTHERS =>
        IF u = 0.0 THEN
            is_Chart_next <= IN_tran1;
            temporalCounter_i1_temp := to_unsigned(0, 8);
        END IF;
    END CASE;

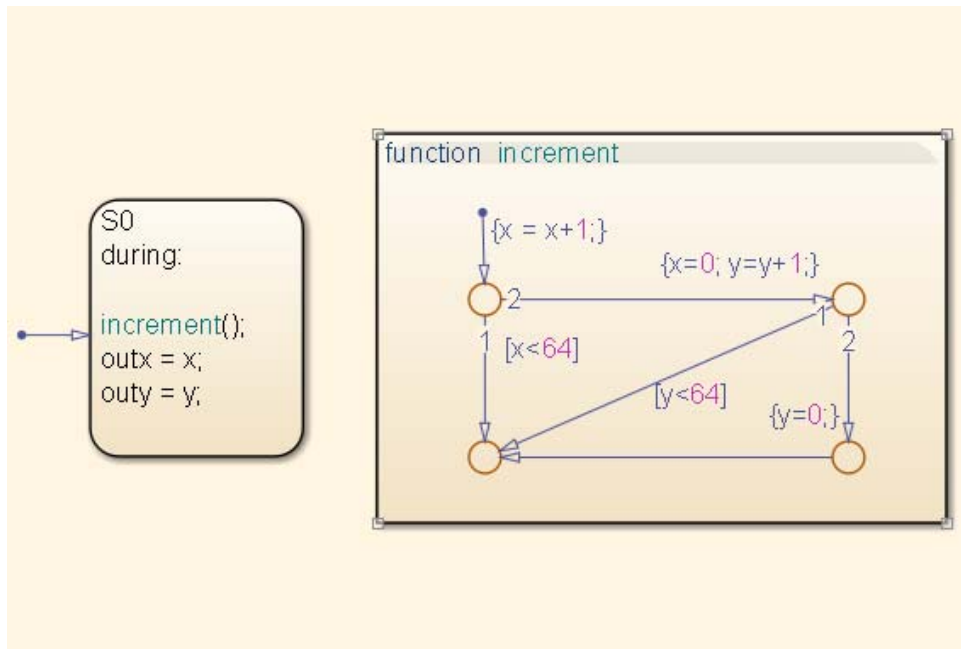
    temporalCounter_i1_next <= temporalCounter_i1_temp;
END PROCESS Chart_1_output;

```

## Graphical Function

A graphical function is a function defined graphically by a flow diagram. Graphical functions reside in a chart along with the diagrams that invoke them. Like MATLAB functions and C functions, graphical functions can accept arguments and return results. Graphical functions can be invoked in transition and state actions.

The following figure shows a graphical function that implements a 64-by-64 counter.



The following code excerpt shows VHDL code generated for this graphical function.

```
x64_counter_sf : PROCESS (x, y, outx_reg, outy_reg)
  -- local variables
  VARIABLE x_temp : unsigned(7 DOWNTO 0);
  VARIABLE y_temp : unsigned(7 DOWNTO 0);
BEGIN
  outx_reg_next <= outx_reg;
  outy_reg_next <= outy_reg;
  x_temp := x;
  y_temp := y;
  x_temp := tmw_to_unsigned(tmw_to_unsigned(tmw_to_unsigned(x_temp, 9), 10)
+ tmw_to_unsigned(to_unsigned(1, 9), 10), 8);

  IF x_temp < to_unsigned(64, 8) THEN
    NULL;
  ELSE

```



```

        x_temp := to_unsigned(0, 8);
        y_temp := tmw_to_unsigned(tmw_to_unsigned(tmw_to_unsigned(y_temp, 9), 10)
+ tmw_to_unsigned(to_unsigned(1, 9), 10), 8);

        IF y_temp < to_unsigned(64, 8) THEN
            NULL;
        ELSE
            y_temp := to_unsigned(0, 8);
        END IF;

    END IF;

    outx_reg_next <= x_temp;
    outy_reg_next <= y_temp;
    x_next <= x_temp;
    y_next <= y_temp;
END PROCESS x64_counter_sf;

```

## Hierarchy and Parallelism

Stateflow charts support both hierarchy (states containing other states) and parallelism (multiple states that can be active simultaneously).

In Stateflow semantics, parallelism is not synonymous with concurrency. Parallel states can be active simultaneously, but they are executed sequentially according to their execution order. (Execution order is displayed on the upper right corner of a parallel state).

For detailed information on hierarchy and parallelism, see “Stateflow Hierarchy of Objects” and “Execution Order for Parallel States”.

For HDL code generation, an entire chart maps to a single output computation process. Within the output computation process:

- The execution of parallel states proceeds sequentially.
- Nested hierarchical states map to nested CASE statements in the generated HDL code.

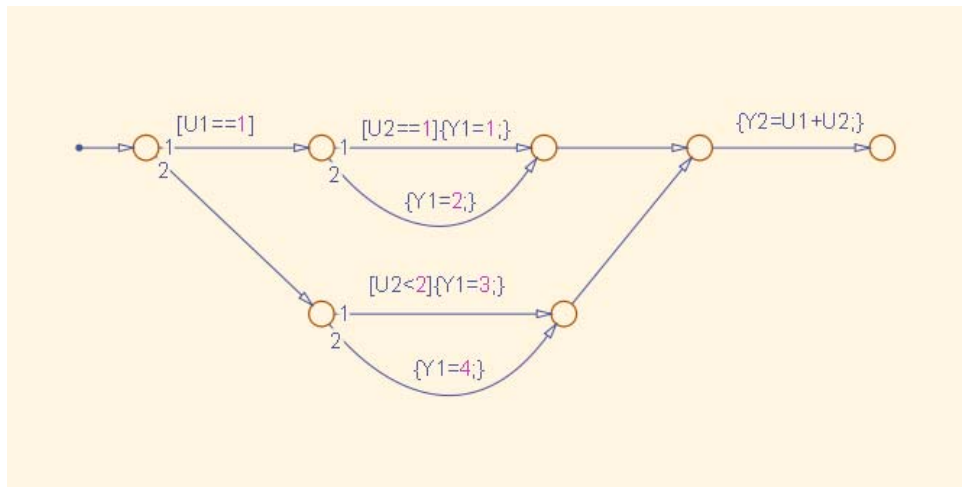
## Stateless Charts

Charts consisting of pure flow diagrams (i.e., charts without states ) are useful in capturing if-then-else constructs used in procedural languages like C.

As an example, consider the following logic, expressed in C-like pseudocode.

```
if(U1==1) {
    if(U2==1) {
        Y = 1;
    }else{
        Y = 2;
    }
}
}else{
    if(U2<2) {
        Y = 3;
    }else{
        Y = 4;
    }
}
```

The following figure shows the flow diagram that implements the if-then-else logic.



The following generated VHDL code excerpt shows the nested IF-ELSE statements obtained from the flow diagram.

```

Chart : PROCESS (Y1_reg, Y2_reg, U1, U2)
  -- local variables
  BEGIN
    Y1_reg_next <= Y1_reg;
    Y2_reg_next <= Y2_reg;

    IF unsigned(U1) = to_unsigned(1, 8) THEN

      IF unsigned(U2) = to_unsigned(1, 8) THEN
        Y1_reg_next <= to_unsigned(1, 8);
      ELSE
        Y1_reg_next <= to_unsigned(2, 8);
      END IF;

    ELSIF unsigned(U2) < to_unsigned(2, 8) THEN
      Y1_reg_next <= to_unsigned(3, 8);
    ELSE
      Y1_reg_next <= to_unsigned(4, 8);
    END IF;

    Y2_reg_next <= tmw_to_unsigned(tmw_to_unsigned(tmw_to_unsigned(unsigned(U1), 9), 10)
      + tmw_to_unsigned(tmw_to_unsigned(unsigned(U2), 9), 10), 8);
  END PROCESS Chart;

```

## Truth Tables

The coder supports HDL code generation for:

- Truth Table functions within a Stateflow chart
- Truth Table blocks in Simulink models

This section examines a Truth Table function in a chart, and the VHDL code generated for the chart.

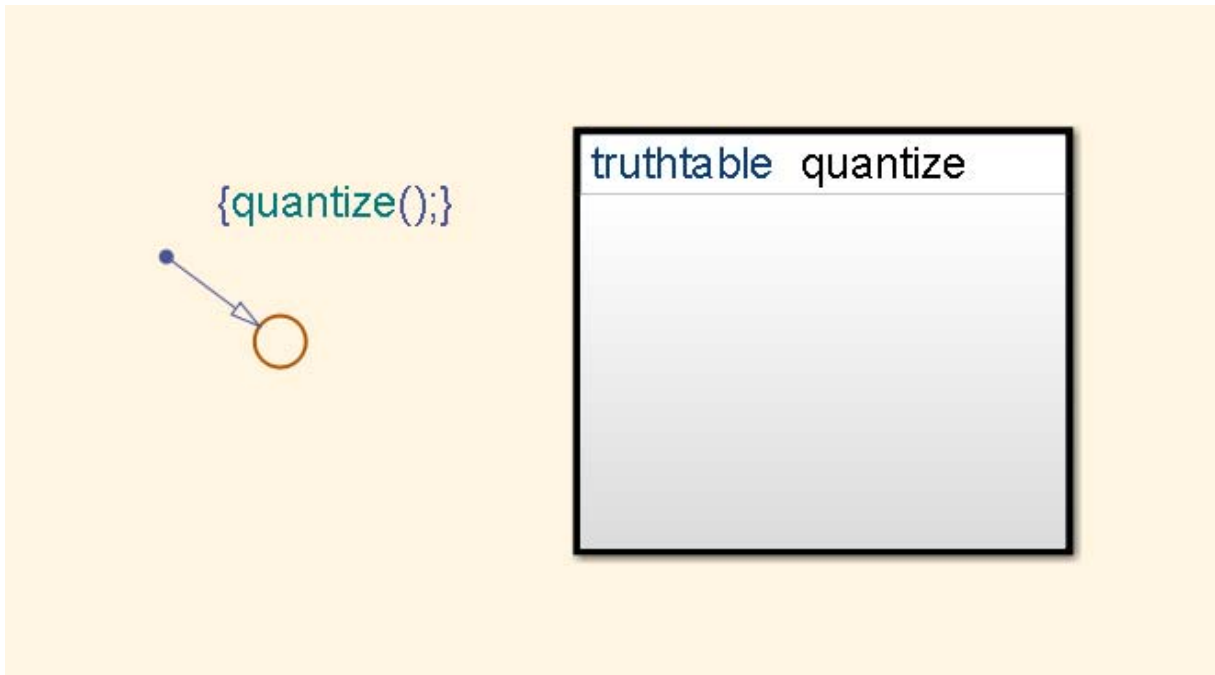
Truth Tables are well-suited for implementing compact combinatorial logic. A typical application for Truth Tables is to implement nonlinear quantization or threshold logic. Consider the following logic:

```

Y = 1 when 0 <= U <= 10
Y = 2 when 10 < U <= 17
Y = 3 when 17 < U <= 45
Y = 4 when 45 < U <= 52
Y = 5 when 52 < U
    
```

A stateless chart with a single call to a Truth Table function can represent this logic succinctly.

The following figure shows the quantizer chart, containing the Truth Table.



The following figure shows the threshold logic, as displayed in the Truth Table Editor.

The screenshot shows a Stateflow window titled "Stateflow (truth table) sf\_truth\_table/quantizer/quantizer.quantize". The window contains two tables: a "Condition Table" and an "Action Table".

**Condition Table**

	Description	Condition	D1	D2	D3	D4	D5
1		$U \leq 10$	T	-	-	-	-
2		$U \leq 17$	-	T	-	-	-
3		$U \leq 45$	-	-	T	-	-
4		$U \leq 52$	-	-	-	T	-
		Actions: Specify a row from the Action Table	1	2	3	4	5

**Action Table**

#	Description	Action
1		$Y = 1$
2		$Y = 2$
3		$Y = 3$
4		$Y = 4$
5		$Y = 5$

The following code excerpt shows VHDL code generated for the quantizer chart.

```
quantizer : PROCESS (Y_reg, U)
```

```
-- local variables
VARIABLE aVarTruthTableCondition_1 : std_logic;
VARIABLE aVarTruthTableCondition_2 : std_logic;
VARIABLE aVarTruthTableCondition_3 : std_logic;
VARIABLE aVarTruthTableCondition_4 : std_logic;
BEGIN
  Y_reg_next <= Y_reg;
  -- Condition #1
  aVarTruthTableCondition_1 := tmw_to_stdlogic(unsigned(U) <= to_unsigned(10, 8));
  -- Condition #2
  aVarTruthTableCondition_2 := tmw_to_stdlogic(unsigned(U) <= to_unsigned(17, 8));
  -- Condition #3
  aVarTruthTableCondition_3 := tmw_to_stdlogic(unsigned(U) <= to_unsigned(45, 8));
  -- Condition #4
  aVarTruthTableCondition_4 := tmw_to_stdlogic(unsigned(U) <= to_unsigned(52, 8));

  IF tmw_to_boolean(aVarTruthTableCondition_1) THEN
    -- D1
    -- Action 1
    Y_reg_next <= to_unsigned(1, 8);
  ELSIF tmw_to_boolean(aVarTruthTableCondition_2) THEN
    -- D2
    -- Action 2
    Y_reg_next <= to_unsigned(2, 8);
  ELSIF tmw_to_boolean(aVarTruthTableCondition_3) THEN
    -- D3
    -- Action 3
    Y_reg_next <= to_unsigned(3, 8);
  ELSIF tmw_to_boolean(aVarTruthTableCondition_4) THEN
    -- D4
    -- Action 4
    Y_reg_next <= to_unsigned(4, 8);
  ELSE
    -- Default
    -- Action 5
    Y_reg_next <= to_unsigned(5, 8);
  END IF;

END PROCESS quantizer;
```

---

**Note** When generating code for a Truth Table block in a Simulink model, the coder writes a separate entity/architecture file for the Truth Table code. The file is named `Truth_Table.vhd` (for VHDL) or `Truth_Table.v` (for Verilog).

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# Generating HDL Code with the MATLAB Function Block

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- “HDL Applications for the MATLAB Function Block” on page 17-2
- “Viterbi Decoder with the MATLAB Function Block” on page 17-3
- “Code Generation from a MATLAB Function Block” on page 17-4
- “MATLAB Function Block Design Patterns for HDL” on page 17-23
- “Design Guidelines for the MATLAB Function Block” on page 17-37
- “Distributed Pipeline Insertion for MATLAB Function Blocks” on page 17-42
- “Limitations for MATLAB Function Block Code Generation” on page 17-49
- “Complex Data Type Support” on page 17-50
- “Operators” on page 17-59
- “Control Flow Statements” on page 17-62
- “Persistent Variables” on page 17-64
- “Persistent Array Variables” on page 17-66
- “Data Types for Variables and Constants” on page 17-67
- “Fixed-Point Bitwise Functions” on page 17-69
- “Fixed-Point Run-Time Library Functions” on page 17-76

## HDL Applications for the MATLAB Function Block

The MATLAB Function block contains a MATLAB function in a model. The function's inputs and outputs are represented by ports on the block, which allow you to interface your model to the function code. When you generate HDL code for a MATLAB Function block, the coder generates two main HDL code files:

- A file containing entity and architecture code that implement the actual algorithm or computations generated for the MATLAB Function block.
- A file containing an entity definition and RTL architecture that provide a black box interface to the algorithmic code generated for the MATLAB Function block.

The structure of these code files is analogous to the structure of the model, in which a subsystem provides an interface between the root model and the function in the MATLAB Function block.

The MATLAB Function block supports a subset of the MATLAB language that is well-suited to HDL implementation of various DSP and telecommunications algorithms, such as:

- Sequence and pattern generators
- Encoders and decoders
- Interleavers and deinterleavers
- Modulators and demodulators
- Multipath channel models; impairment models
- Timing recovery algorithms
- Viterbi algorithm; Maximum Likelihood Sequence Estimation (MLSE)
- Adaptive equalizer algorithms

## Viterbi Decoder with the MATLAB Function Block

`hdlcoderviterbi2` models a Viterbi decoder, incorporating an MATLAB Function block for use in simulation and HDL code generation. To open the model, type the following at the MATLAB command prompt:

```
hdlcoderviterbi2
```

## Code Generation from a MATLAB Function Block

### In this section...

“Counter Model Using the MATLAB Function block” on page 17-4

“Setting Up” on page 17-7

“Creating the Model and Configuring General Model Settings” on page 17-8

“Adding a MATLAB Function Block to the Model” on page 17-8

“Set Fixed-Point Options for the MATLAB Function Block” on page 17-10

“Programming the MATLAB Function Block” on page 17-14

“Constructing and Connecting the DUT\_eML\_Block Subsystem” on page 17-15

“Compiling the Model and Displaying Port Data Types” on page 17-18

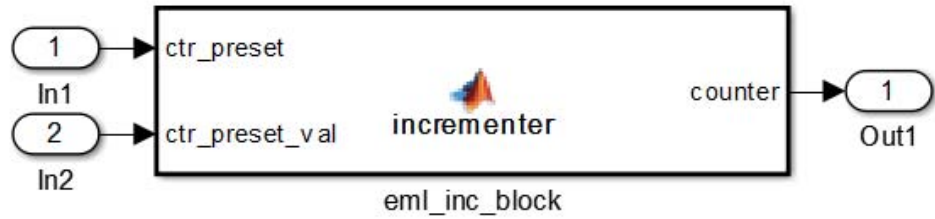
“Simulating the eml\_hdl\_incrementer\_tut Model” on page 17-19

“Generating HDL Code” on page 17-20

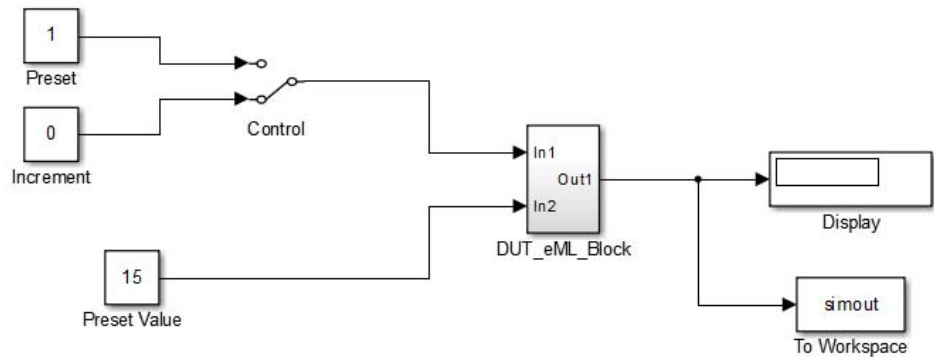
### Counter Model Using the MATLAB Function block

In this tutorial, you construct and configure a simple model, `eml_hdl_incrementer_tut`, and then generate VHDL code from the model. `eml_hdl_incrementer_tut` includes a MATLAB Function block that implements a simple fixed-point counter function, `incrementer`. The `incrementer` function is invoked once during each sample period of the model. The function maintains a persistent variable count, which is either incremented or reinitialized to a preset value (`ctr_preset_val`), depending on the value passed in to the `ctr_preset` input of the MATLAB Function block. The function returns the counter value (`counter`) at the output of the MATLAB Function block.

The MATLAB Function block resides in a subsystem, `DUT_eML_Block`. The subsystem functions as the device under test (DUT) from which you generate HDL code.



The root-level model drives the subsystem and includes Display and To Workspace blocks for use in simulation. (The Display and To Workspace blocks do not generate HDL code.)



---

**Tip** If you do not want to construct the model step by step, or do not have time, you can open the completed model by entering the name at the command prompt:

```
eml_hdl_incrementer
```

After you open the model, save a copy of it to your local folder as `eml_hdl_incrementer_tut`.

---

## The Incrementer Function Code

The following code listing gives the complete incrementer function definition:

```
function counter = incrementer(ctr_preset, ctr_preset_val)
% The function incrementer implements a preset counter that counts
% how many times this block is called.
%
% This example function shows how to model memory with persistent variables,
% using fimath settings suitable for HDL. It also demonstrates MATLAB
% operators and other language features that HDL Coder supports
% for code generation from Embedded MATLAB Function block.
%
% On the first call, the result 'counter' is initialized to zero.
% The result 'counter' saturates if called more than 2^14-1 times.
% If the input ctr_preset receives a nonzero value, the counter is
% set to a preset value passed in to the ctr_preset_val input.

persistent current_count;
if isempty(current_count)
    % zero the counter on first call only
    current_count = uint32(0);
end

counter = getfi(current_count);

if ctr_preset
    % set counter to preset value if input preset signal is nonzero
```

```
        counter = ctr_preset_val;
    else
        % otherwise count up
        inc = counter + getfi(1);
        counter = getfi(inc);
    end

    % store counter value for next iteration
    current_count = uint32(counter);

    function hdl_fi = getfi(val)

    nt = numerictype(0,14,0);
    fm = hdlfimath;
    hdl_fi = fi(val, nt, fm);
```

## Setting Up

Before you begin building the example model, set up a working folder for your model and generated code.

### Setting Up a folder

- 1 Start MATLAB.
- 2 Create a folder named `eml_tut`, for example:

```
mkdir D:\work\eml_tut
```

The `eml_tut` folder stores the model you create, and also contains subfolders and generated code. The location of the folder does not matter, except that it should not be within the MATLAB tree.

- 3 Make the `eml_tut` folder your working folder, for example:

```
cd D:\work\eml_tut
```

## Creating the Model and Configuring General Model Settings

In this section, you create a model and set some parameters to values recommended for HDL code generation `hdlsetup.m` command. The `hdlsetup` command uses the `set_param` function to set up models for HDL code generation quickly and consistently. See “Initializing Model Parameters with `hdlsetup`” for further information about `hdlsetup`.

To set the model parameters:

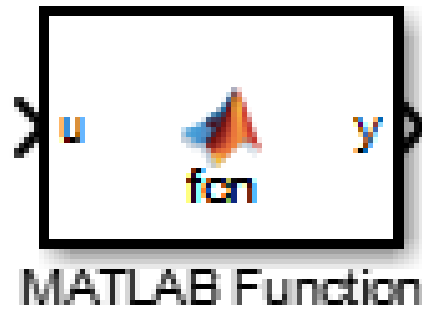
- 1 Create a new model.
- 2 Save the model as `eml_hdl_incrementer_tut`.
- 3 At the MATLAB command prompt, type:

```
hdlsetup('eml_hdl_incrementer_tut');
```
- 4 Open the Configuration Parameters dialog box.
- 5 Set the following **Solver** options, which are useful in simulating this model:
  - **Fixed step size:** 1
  - **Stop time:** 5
- 6 Click **OK** to save your changes and close the Configuration Parameters dialog box.
- 7 Save your model.

## Adding a MATLAB Function Block to the Model

- 1 Open the Simulink Library Browser. Then, select the Simulink/User-Defined Functions library.
- 2 Select the MATLAB Function block from the library window and add it to the model.





- 3 Change the block label from MATLAB Function to em1\_inc\_block.



4 Save the model.

5 Close the Simulink Library Browser.

### **Set Fixed-Point Options for the MATLAB Function Block**

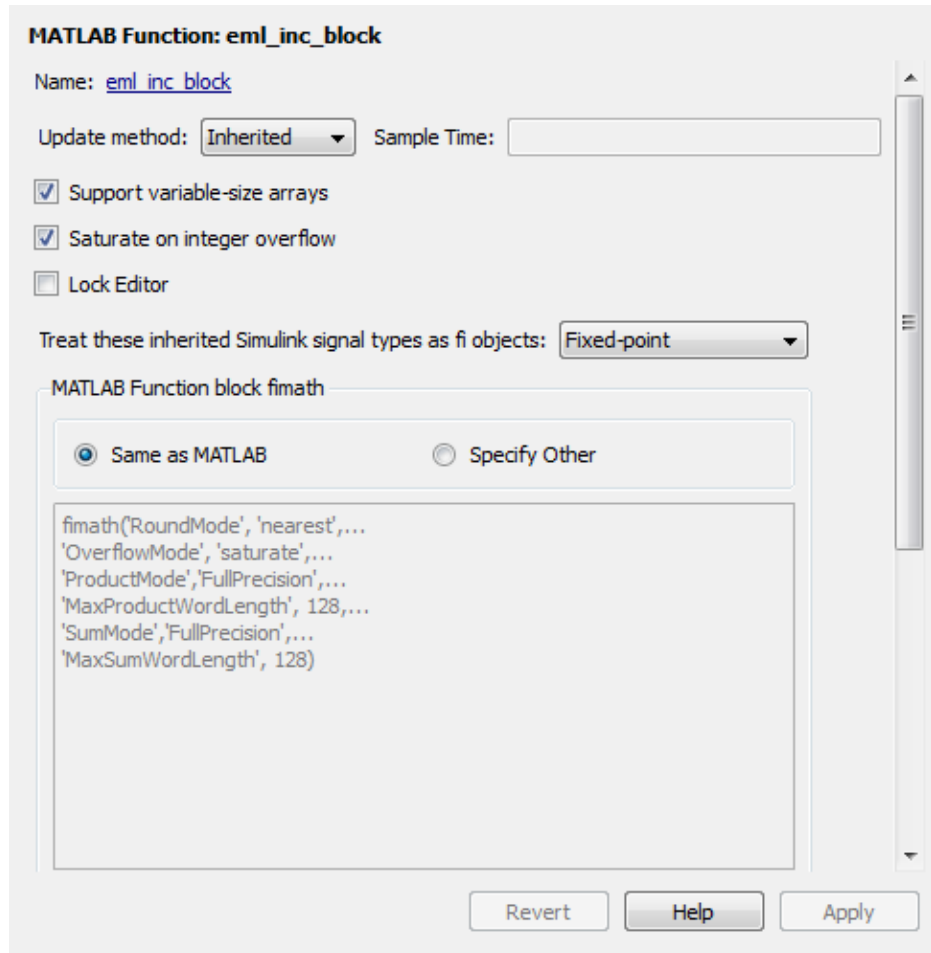
This section describes how to set up the FIMATH specification and other fixed-point options that are recommended for efficient HDL code generation from the MATLAB Function block. The recommended settings are:

- ProductMode property of the FIMATH specification: 'FullPrecision'

- SumMode property of the FIMATH specification: 'FullPrecision'
- **Treat these inherited signal types as fi objects** option: Fixed-point (This is the default setting.)

Configure the options as follows:

- 1** Open the `eml_hdl_incrementer_tut` model that you created in “Adding a MATLAB Function Block to the Model” on page 17-8.
- 2** Double-click the MATLAB Function block to open it for editing. The MATLAB Function Block Editor appears.
- 3** Click **Edit Data**. The Ports and Data Manager dialog box opens, displaying the default FIMATH specification and other properties for the MATLAB Function block.

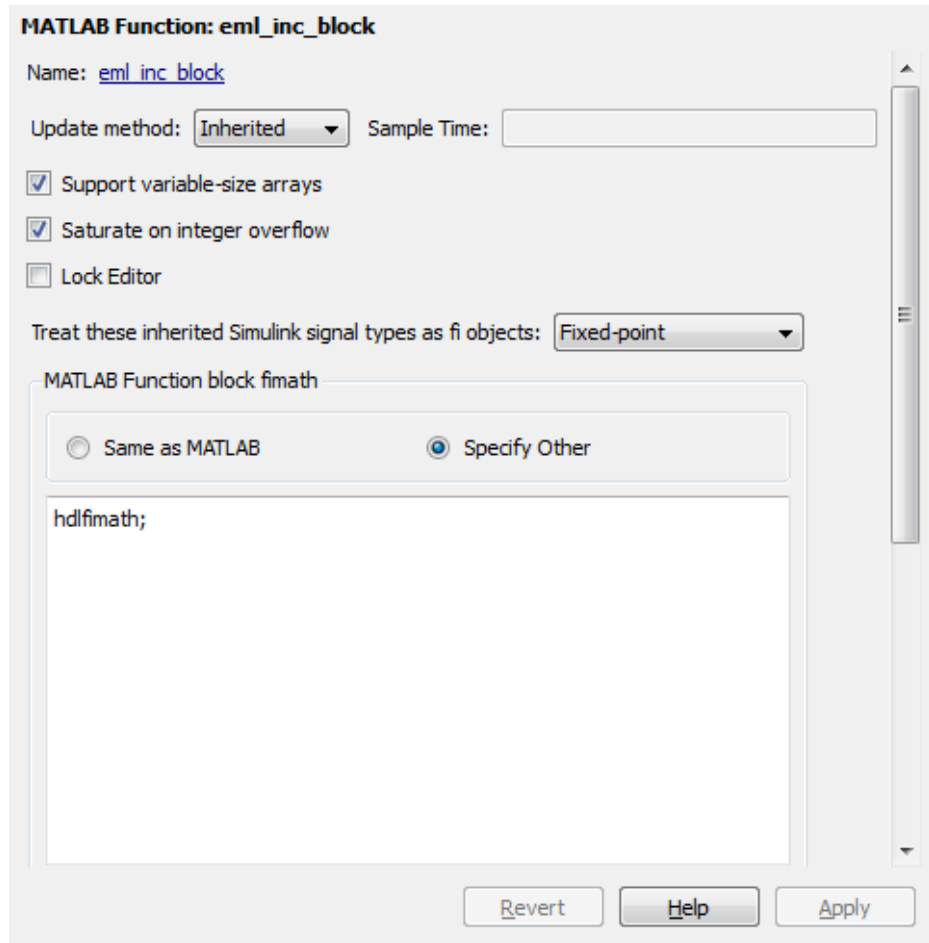


**4** Select **Specify Other**. Selecting this option enables the **MATLAB Function block fimath** text entry field.

**5** The `hdlfimath.m` function is a utility that defines a FIMATH specification that is optimized for HDL code generation. Replace the default **MATLAB Function block fimath** specification with a call to `hdlfimath` as follows:

```
hdlfimath;
```

- 6 Click **Apply**. The MATLAB Function block properties should now appear as shown in the following figure.



- 7 Close the Ports and Data Manager.
- 8 Save the model.

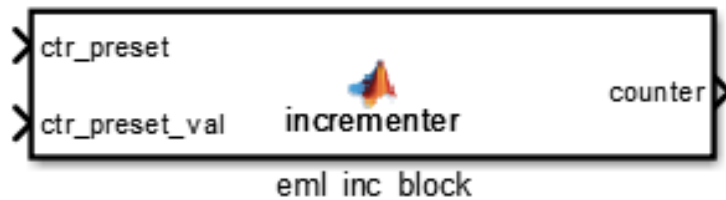
## Programming the MATLAB Function Block

The next step is add code to the MATLAB Function block to define the incrementer function, and then use diagnostics to check for errors.

- 1 Open the `eml_hdl_incrementer_tut` model that you created in “Adding a MATLAB Function Block to the Model” on page 17-8.
- 2 Double-click the MATLAB Function block to open it for editing.
- 3 In the MATLAB Function Block Editor, delete the default code.
- 4 Copy the complete `incrementer` function definition from the listing given in “The Incrementer Function Code” on page 17-6, and paste it into the editor.
- 5 Save the model. Doing so updates the model window, redrawing the MATLAB Function block.

Changing the function header of the MATLAB Function block makes the following changes to the block icon:

- The function name in the middle of the block changes to `incrementer`.
  - The arguments `ctr_preset` and `ctr_preset_val` appear as input ports to the block.
  - The return value `counter` appears as an output port from the block.
- 6 Resize the block to make the port labels more legible.



- 7 Save the model again.

## **Constructing and Connecting the DUT\_eML\_Block Subsystem**

This section assumes that you have completed “Programming the MATLAB Function Block” on page 17-14 without encountering an error. In this section, you construct a subsystem containing the `incrementer` function block, to be used as the device under test (DUT) from which to generate HDL code. You then set the port data types and connect the subsystem ports to the model.

### **Constructing the DUT\_eML\_Block Subsystem**

Construct a subsystem containing the `incrementer` function block as follows:

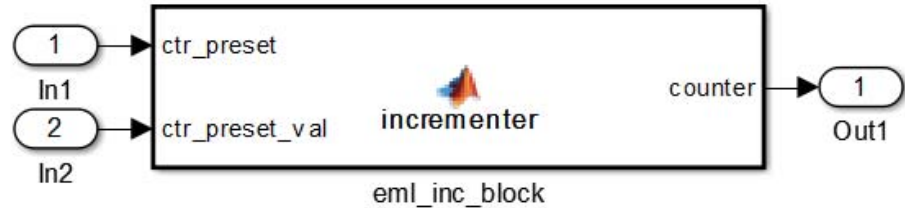
- 1 Click the `incrementer` function block.
- 2 Select **Diagram > Subsystem & Model Reference > Create Subsystem from Selection**.

A subsystem, labeled `Subsystem`, is created in the model window.

- 3 Change the `Subsystem` label to `DUT_eML_Block`.

### **Setting Port Data Types for the MATLAB Function Block**

- 1 Double-click the subsystem to view its interior. As shown in the following figure, the subsystem contains the `incrementer` function block, with input and output ports connected.



- 2 Double-click the incrementer function block to open the MATLAB Function Block Editor.
- 3 In the editor, click **Edit Data** to open the Ports and Data Manager.
- 4 Select the ctr\_preset entry in the port list on the left. Click the button labeled >> to display the Data Type Assistant. Set **Mode** for this port to Built in. Set **Data type** to boolean. Click the button labeled << to close the Data Type Assistant. Click **Apply**.
- 5 Select the ctr\_preset\_val entry in the port list on the left. Click the button labeled >> to display the Data Type Assistant. Set **Mode** for this port to Fixed point. Set **Signedness** to Unsigned. Set **Word length** to 14. Click the button labeled << to close the Data Type Assistant. Click **Apply**.
- 6 Select the counter entry in the port list on the left. Click the button labeled >> to display the Data Type Assistant. Verify that **Mode** for this port is set to Inherit: Same as Simulink. Click the button labeled << to close the Data Type Assistant. Click **Apply**.
- 7 Close the Ports and Data Manager dialog box and the MATLAB Function Block Editor.
- 8 Save the model and close the DUT\_eML\_Block subsystem.



## Connecting Subsystem Ports to the Model

Next, connect the ports of the DUT\_eML\_Block subsystem to the model as follows:

- 1 From the Sources library, add a Constant block to the model. Set the value of the Constant to 1, and the **Output data type** to **boolean**. Change the block label to **Preset**.
- 2 Make a copy of the **Preset** Constant block. Set its value to 0, and change its block label to **Increment**.
- 3 From the Signal Routing library, add a Manual Switch block to the model. Change its label to **Control**. Connect its output to the In1 port of the DUT\_eML\_Block subsystem.
- 4 Connect the **Preset** Constant block to the upper input of the **Control** switch block. Connect the **Increment** Constant block to the lower input of the **Control** switch block.
- 5 Add a third Constant block to the model. Set the value of the Constant to 15, and the **Output data type** to **Inherit via back propagation**. Change the block label to **Preset Value**.
- 6 Connect the **Preset Value** Constant block to the In2 port of the DUT\_eML\_Block subsystem.
- 7 From the Sinks library, add a Display block to the model. Connect it to the Out1 port of the DUT\_eML\_Block subsystem.
- 8 From the Sinks library, add a To Workspace block to the model. Route the output signal from the DUT\_eML\_Block subsystem to the To Workspace block.
- 9 Save the model.

## Checking the Function for Errors

Use the built-in diagnostics of MATLAB Function blocks to test for syntax errors:

- 1 Open the `eml_hdl_incrementer_tut` model.

- 2 Double-click the MATLAB Function block incrementer to open it for editing.
- 3 In the MATLAB Function Block Editor, select **Build Model > Build** to compile and build the MATLAB Function block code.

The build process displays some progress messages. These messages include some warnings, because the ports of the MATLAB Function block are not yet connected to signals. You can ignore these warnings.

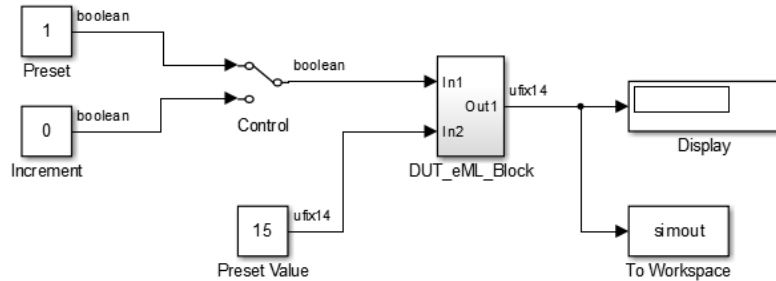
The build process builds an S-function for use in simulation. The build process includes generation of C code for the S-function. The code generation messages you see during the build process refer to generation of C code, not HDL code generation.

When the build concludes without encountering an error, a message window appears indicating that parsing was successful. If errors are found, the Diagnostics Manager lists them. See the MATLAB Function block documentation for information on debugging MATLAB Function block build errors.

### Compiling the Model and Displaying Port Data Types

In this section you enable the display of port data types and then compile the model. Model compilation verifies the model structure and settings, and updates the model display.

- 1 Select **Display > Signals & Ports > Port Data Types**.
- 2 Select **Simulation > Update Diagram** (or press **Ctrl+D**) to compile the model. This triggers a rebuild of the code. After the model compiles, the block diagram updates to show the port data types.

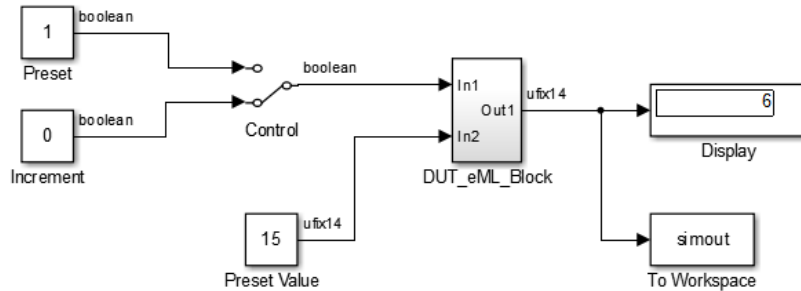


3 Save the model.

## Simulating the `eml_hdl_incrementer_tut` Model

Start simulation. If required, the code rebuilds before the simulation starts.

After the simulation completes, the Display block shows the final output value returned by the `incrementer` function block. For example, given a **Start time** of 0, a **Stop time** of 5, and a zero value at the `ctr_preset` port, the simulation returns a value of 6:



You might want to experiment with the results of toggling the `Control` switch, changing the `Preset Value` constant, and changing the total simulation time. You might also want to examine the workspace variable `simout`, which is bound to the `To Workspace` block.

## Generating HDL Code

In this section, you select the `DUT_eML_Block` subsystem for HDL code generation, set basic code generation options, and then generate VHDL code for the subsystem.

### Selecting the Subsystem for Code Generation

Select the `DUT_eML_Block` subsystem for code generation:

- 1 Open the Model Configuration Parameters dialog box and click the **HDL Code** pane.
- 2 Select `eml_hdl_incrementer_tut/DUT_eML_Block` from the **Generate HDL for** list.
- 3 Click **OK**.

## Generating VHDL Code

The top-level **HDL Code** options should now be set as follows:

- The **Generate HDL for** field specifies the `eml_hdl_incrementer_tut/DUT_eML_Block` subsystem for code generation.
- The **Language** field specifies (by default) generation of VHDL code.
- The **Folder** field specifies (by default) that the code generation target folder is a subfolder of your working folder, named `hdlsrc`.

Before generating code, select **Current Folder** from the **Layout** menu in the MATLAB Command Window. This displays the Current Folder browser, which lets you easily access your working folder and the files that are generated within it.

To generate code:

- 1 Click the **Generate** button.

The coder compiles the model before generating code. Depending on model display options (such as port data types), the appearance of the model might change after code generation.

- 2 As code generation proceeds, the coder displays progress messages. The process should complete with a message like the following:

```
### HDL Code Generation Complete.
```

The names of generated VHDL files in the progress messages are hyperlinked. After code generation completes, you can click these hyperlinks to view the files in the MATLAB Editor.

- 3 A folder icon for the `hdlsrc` folder is now visible in the Current Folder browser. To view generated code and script files, double-click the `hdlsrc` folder icon.
- 4 Observe that two VHDL files were generated. The structure of HDL code generated for MATLAB Function blocks is similar to the structure of code generated for Stateflow charts and Digital Filter blocks. The VHDL files that were generated in the `hdlsrc` folder are:

- `eml_inc_blk.vhd`: VHDL code. This file contains entity and architecture code implementing the actual computations generated for the MATLAB Function block.
- `DUT_eML_Block.vhd`: VHDL code. This file contains an entity definition and RTL architecture that provide a black box interface to the code generated in `eml_inc_blk.vhd`.

The structure of these code files is analogous to the structure of the model, in which the `DUT_eML_Block` subsystem provides an interface between the root model and the incrementer function in the MATLAB Function block.

The other files generated in the `hdlsrc` folder are:

- `DUT_eML_Block_compile.do`: Mentor Graphics ModelSim compilation script (`vcom` command) to compile the VHDL code in the two `.vhd` files.
  - `DUT_eML_Block_synplify.tcl`: Synplify® synthesis script.
  - `DUT_eML_Block_map.txt`: Mapping file. This report file maps generated entities (or modules) to the subsystems that generated them (see “Trace Code Using the Mapping File” on page 14-36).
- 5** To view the generated VHDL code in the MATLAB Editor, double-click the `DUT_eML_Block.vhd` or `eml_inc_blk.vhd` file icons in the Current Folder browser.

## MATLAB Function Block Design Patterns for HDL

### In this section...

“The eml\_hdl\_design\_patterns Library” on page 17-23

“Efficient Fixed-Point Algorithms” on page 17-25

“Model State Using Persistent Variables” on page 17-29

“Creating Intellectual Property with the MATLAB Function Block” on page 17-30

“Nontunable Parameter Arguments” on page 17-31

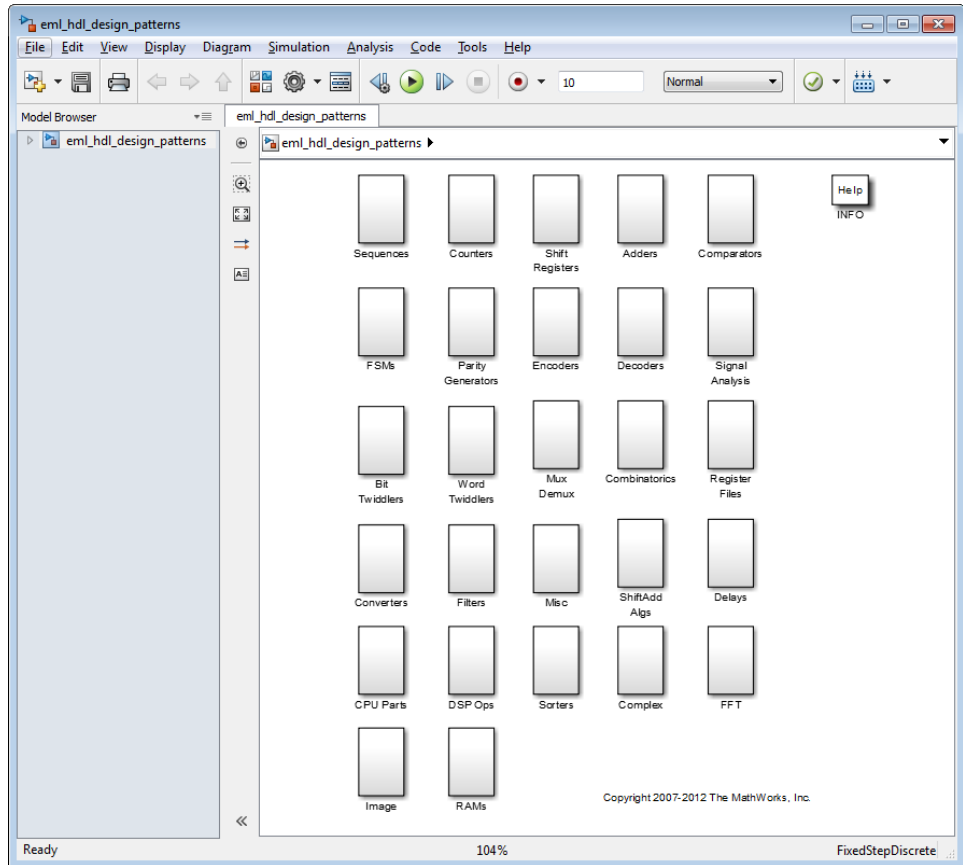
“Modeling Control Logic and Simple Finite State Machines” on page 17-31

“Modeling Counters” on page 17-33

“Modeling Hardware Elements” on page 17-35

### The eml\_hdl\_design\_patterns Library

The eml\_hdl\_design\_patterns library is an extensive collection of examples demonstrating useful applications of the MATLAB Function block in HDL code generation.



To open the library, type the following command at the MATLAB prompt:

```
em1_hdl_design_patterns
```

You can use many blocks in the library as cookbook examples of various hardware elements, as follows:

- Copy a block from the library to your model and use it as a computational unit.
- Copy the code from the block and use it as a local function in an existing MATLAB Function block.



When you create custom blocks, you can control whether to inline or instantiate the HDL code generated from MATLAB Function blocks. Use the **Inline MATLAB Function block code** check box in the **HDL Code > Global Settings > Coding style** section of the Model Configuration Parameters dialog box. For more information, see “Inline MATLAB Function block code” on page 7-69.

## Efficient Fixed-Point Algorithms

The MATLAB Function block supports fixed point arithmetic using the Fixed-Point Toolbox `fi` function. This function supports rounding and saturation modes that are useful for coding algorithms that manipulate arbitrary word and fraction lengths. The coder supports all `fi` rounding and overflow modes.

HDL code generated from the MATLAB Function block is bit-true to MATLAB semantics. Generated code uses bit manipulation and bit access operators (for example, `Slice`, `Extend`, `Reduce`, `Concat`, etc.) that are native to VHDL and Verilog.

The following discussion shows how HDL code generated from the MATLAB Function block follows cast-before-sum semantics, in which addition and subtraction operands are cast to the result type before the addition or subtraction is performed.

Open the `eml_hdl_design_patterns` library and select the `Combinatorics/eml_expr` block. `eml_expr` implements a simple expression containing addition, subtraction, and multiplication operators with differing fixed point data types. The generated HDL code shows the conversion of this expression with fixed point operands. The MATLAB Function block uses the following code:

```
% fixpt arithmetic expression
expr = (a*b) - (a+b);

% cast the result to (sfix7_En4) output type
y = fi(expr, 1, 7, 4);
```

The default `fimath` specification for the block determines the behavior of arithmetic expressions using fixed point operands inside the MATLAB Function block:

```
fimath(...  
    'RoundMode', 'ceil',...  
    'OverflowMode', 'saturate',...  
    'ProductMode', 'FullPrecision', 'ProductWordLength', 32,...  
    'SumMode', 'FullPrecision', 'SumWordLength', 32,...  
    'CastBeforeSum', true)
```

The data types of operands and output are as follows:

- a: (`sfix5_En2`)
- b: (`sfix5_En3`)
- y: (`sfix7_En4`).

Before HDL code generation, the operation

```
expr = (a*b) - (a+b);
```

is broken down internally into the following substeps:

```
1 tmul = a * b;  
2 tadd = a + b;  
3 tsub = tmul - tadd;  
4 y = tsub;
```

Based on the `fimath` settings (see “Design Guidelines for the MATLAB Function Block” on page 17-37) this expression is further broken down internally as follows:

- Based on the specified `ProductMode`, 'FullPrecision', the output type of `tmul` is computed as (`sfix10_En5`).
- Since the `CastBeforeSum` property is set to 'true', substep 2 is broken down as follows:

```
t1 = (sfix7_En3) a;
t2 = (sfix7_En3) b;
tadd = t1 + t2;
```

`sfix7_En3` is the result sum type after aligning binary points and accounting for an extra bit to account for possible overflow.

- Based on intermediate types of `tmul` (`sfix10_En5`) and `tadd` (`sfix7_En3`) the result type of the subtraction in substep 3 is computed as `sfix11_En5`. Accordingly, substep 3 is broken down as follows:

```
t3 = (sfix11_En5) tmul;
t4 = (sfix11_En5) tadd;
tsub = t3 - t4;
```

- Finally, the result is cast to a smaller type (`sfix7_En4`) leading to the following final expression statements:

```
tmul = a * b;
t1 = (sfix7_En3) a;
t2 = (sfix7_En3) b;
tadd = t1 + t2;
t3 = (sfix11_En5) tmul;
t4 = (sfix11_En5) tadd;
tsub = t3 - t4;
y = (sfix7_En4) tsub;
```

The following listings show the generated VHDL and Verilog code from the `eml_expr` block.

VHDL code excerpt:

```
BEGIN
  --MATLAB Function 'Subsystem/eml_expr': '<S2>:1'
  -- fixpt arithmetic expression
  -- '<S2>:1:4'
  mul_temp <= signed(a) * signed(b);
  sub_cast <= resize(mul_temp, 11);
  add_cast <= resize(signed(a & '0'), 7);
  add_cast_0 <= resize(signed(b), 7);
  add_temp <= add_cast + add_cast_0;
  sub_cast_0 <= resize(add_temp & '0' & '0', 11);
```

```

expr <= sub_cast - sub_cast_0;
-- cast the result to correct output type
-- '<S2>:1:7'

y <= "0111111" WHEN ((expr(10) = '0') AND (expr(9 DOWNT0 7) /= "000"))
    OR ((expr(10) = '0') AND (expr(7 DOWNT0 1) = "0111111"))
    ELSE
    "1000000" WHEN (expr(10) = '1') AND (expr(9 DOWNT0 7) /= "111")
    ELSE
    std_logic_vector(expr(7 DOWNT0 1) + ("0" & expr(0)));

END fsm_SFHDH;

```

Verilog code excerpt:

```

//MATLAB Function 'Subsystem/em1_expr': '<S2>:1'
// fixpt arithmetic expression
// '<S2>:1:4'
assign mul_temp = a * b;
assign sub_cast = mul_temp;
assign add_cast = {a[4], {a, 1'b0}};
assign add_cast_0 = b;
assign add_temp = add_cast + add_cast_0;
assign sub_cast_0 = {{2{add_temp[6]}}, {add_temp, 2'b00}};
assign expr = sub_cast - sub_cast_0;
// cast the result to correct output type
// '<S2>:1:7'
assign y = (((expr[10] == 0) && (expr[9:7] != 0))
    || ((expr[10] == 0) && (expr[7:1] == 63)) ? 7'sb0111111 :
    ((expr[10] == 1) && (expr[9:7] != 7) ? 7'sb1000000 :
    expr[7:1] + $signed({1'b0, expr[0]}));

```

These code excerpts show that the generated HDL code from the MATLAB Function block represents the bit-true behavior of fixed point arithmetic expressions using high level HDL operators. The HDL code is generated using HDL coding rules like high level `bitselect` and `partselect` replication operators and explicit sign extension and resize operators.

## Model State Using Persistent Variables

In the MATLAB Function block programming model, state-holding elements are represented as persistent variables. A variable that is declared `persistent` retains its value across function calls in software, and across sample time steps during simulation.

Please note that your MATLAB code *must* read the persistent variable before it is written if you want the coder to infer a register in the HDL code. The coder displays a warning message if your code does not follow this rule.

The following example shows the `unit_delay` block, which delays the input sample, `u`, by one simulation time step. `u` is a fixed-point operand of type `sfix6`. `u_d` is a persistent variable that holds the input sample.

```
function y = fcn(u)

persistent u_d;
if isempty(u_d)
    u_d = fi(-1, numerictype(u), fimath(u));
end

% return delayed input from last sample time hit
y = u_d;

% store the current input to be used later
u_d = u;
```

Because this code intends for `u_d` to infer a register during HDL code generation, `u_d` is read in the assignment statement, `y = u_d`, before it is written in `u_d = u`.

The coder generates the following HDL code for the `unit_delay` block.

```
ENTITY Unit_Delay IS
    PORT (
        clk : IN std_logic;
        clk_enable : IN std_logic;
        reset : IN std_logic;
        u : IN std_logic_vector(15 DOWNTO 0);
        y : OUT std_logic_vector(15 DOWNTO 0));
```

```
END Unit_Delay;

ARCHITECTURE fsm_SFHDL OF Unit_Delay IS

BEGIN
    initialize_Unit_Delay : PROCESS (clk, reset)
    BEGIN
        IF reset = '1' THEN
            y <= std_logic_vector(to_signed(0, 16));
        ELSIF clk'EVENT AND clk = '1' THEN
            IF clk_enable = '1' THEN
                y <= u;
            END IF;
        END IF;
    END PROCESS initialize_Unit_Delay;
```

Initialization of persistent variables is moved into the master reset region in the initialization process.

Refer to the `Delays` subsystem in the `eml_hdl_design_patterns` library to see how vectors of persistent variables can be used to model integer delay, tap delay, and tap delay vector blocks. These design patterns are useful in implementing sequential algorithms that carry state between executions of the MATLAB Function block in a model.

## Creating Intellectual Property with the MATLAB Function Block

The MATLAB Function block helps you author intellectual property and create alternate implementations of part of an algorithm. By using MATLAB Function blocks in this way, you can guide the detailed operation of the HDL code generator even while writing high-level algorithms.

For example, the subsystem `Comparators` in the `eml_hdl_design_patterns` library includes several alternate algorithms for finding the minimum value of a vector. The `Comparators/eml_linear_min` block finds the minimum of the vector in a linear mode serially. The `Comparators/eml_tree_min` block

compares the elements in a tree structure. The tree implementation can achieve a higher clock frequency by adding pipeline registers between the  $\log_2(N)$  stages. (See `eml_hdl_design_patterns/Filters` for an example.)

Now consider replacing the simple comparison operation in the Comparators blocks with an arithmetic operation (for example, addition, subtraction, or multiplication) where intermediate results must be quantized. Using `fimath` rounding settings, you can fine tune intermediate value computations before intermediate values feed into the next stage. You can use this technique for tuning the generated hardware or customizing your algorithm.

## Nontunable Parameter Arguments

You can declare a nontunable parameter for a MATLAB Function block by setting its **Scope** to Parameter in the Ports and Data Manager GUI, and clearing the **Tunable** option.

A nontunable parameter does not appear as a signal port on the block. Parameter arguments for MATLAB Function blocks take their values from parameters defined in a parent Simulink masked subsystem or from variables defined in the MATLAB base workspace, not from signals in the Simulink model.

Only *nontunable* parameters are supported for HDL code generation. If you declare parameter arguments in MATLAB Function block code that is intended for HDL code generation, be sure to clear the **Tunable** option for each such parameter argument.

## Modeling Control Logic and Simple Finite State Machines

MATLAB Function block control constructs such as `switch/case` and `if-elseif-else`, coupled with fixed point arithmetic operations let you model control logic quickly.

The `FSMs/mealy_fsm_blk` and `FSMs/moore_fsm_blk` blocks in the `eml_hdl_design_patterns` library provide example implementations of Mealy and Moore finite state machines in the MATLAB Function block.

The following listing implements a Moore state machine.

```
function Z = moore_fsm(A)

persistent moore_state_reg;
if isempty(moore_state_reg)
    moore_state_reg = fi(0, 0, 2, 0);
end

S1 = 0;
S2 = 1;
S3 = 2;
S4 = 3;

switch uint8(moore_state_reg)

    case S1,
        Z = true;
        if (~A)
            moore_state_reg(1) = S1;
        else
            moore_state_reg(1) = S2;
        end
    case S2,
        Z = false;
        if (~A)
            moore_state_reg(1) = S1;
        else
            moore_state_reg(1) = S2;
        end
    case S3,
        Z = false;
        if (~A)
            moore_state_reg(1) = S2;
        else
            moore_state_reg(1) = S3;
        end
    case S4,
        Z = true;
        if (~A)
            moore_state_reg(1) = S1;
        else
```



```

        moore_state_reg(1) = S3;
    end
    otherwise,
        Z = false;
end

```

In this example, a persistent variable (`moore_state_reg`) models state variables. The output depends only on the state variables, thus modeling a Moore machine.

The FSMs/`mealy_fsm_blk` block in the `eml_hdl_design_patterns` library implements a Mealy state machine. A Mealy state machine differs from a Moore state machine in that the outputs depend on inputs as well as state variables.

The MATLAB Function block can quickly model simple state machines and other control-based hardware algorithms (such as pattern matchers or synchronization-related controllers) using control statements and persistent variables.

For modeling more complex and hierarchical state machines with complicated temporal logic, use a Stateflow chart to model the state machine.

## Modeling Counters

To implement arithmetic and control logic algorithms in MATLAB Function blocks intended for HDL code generation, there are some simple HDL related coding requirements:

- The top level MATLAB Function block must be called once per time step.
- It must be possible to fully unroll program loops.
- Persistent variables with reset values and update logic must be used to hold values across simulation time steps.
- Quantized data variables must be used inside loops.

The following script shows how to model a synchronous up/down counter with preset values and control inputs. The example provides both master reset control of persistent state variables and local reset control using block

inputs (e.g. `presetClear`). The `isempty` condition enters the initialization process under the control of a synchronous reset. The `presetClear` section is implemented in the output section in the generated HDL code.

Both the up and down case statements implementing the count loop require that the values of the counter are quantized after addition or subtraction. By default, the MATLAB Function block automatically propagates fixed-point settings specified for the block. In this script, however, fixed-point settings for intermediate quantities and constants are explicitly specified.

```
function [Q, QN] = up_down_ctr(upDown, presetClear, loadData, presetData)

% up down result
% 'result' synthesizes into sequential element

result_nt = numerictype(0,4,0);
result_fm = fimath('OverflowMode', 'saturate', 'RoundMode', 'floor');

initVal = fi(0, result_nt, result_fm);

persistent count;
if isempty(count)
    count = initVal;
end

if presetClear
    count = initVal;
elseif loadData
    count = presetData;
elseif upDown
    inc = count + fi(1, result_nt, result_fm);
    -- quantization of output
    count = fi(inc, result_nt, result_fm);
else
    dec = count - fi(1, result_nt, result_fm);
    -- quantization of output
    count = fi(dec, result_nt, result_fm);
end

Q = count;
```

```
QN = bitcmp(count);
```

## Modeling Hardware Elements

The following code example shows how to model shift registers in MATLAB Function block code by using the `bitsliceget` and `bitconcat` function. This function implements a serial input and output shifters with a 32-bit fixed-point operand input. See the `Shift Registers/shift_reg_1by32` block in the `eml_hdl_design_patterns` library for more details.

```
function sr_out = fcn(shift, sr_in)
%shift register 1 by 32

persistent sr;
if isempty(sr)
    sr = fi(0, 0, 32, 0, 'fimath', fimath(sr_in));
end

% return sr[31]
sr_out = getmsb(sr);

if (shift)
    % sr_new[32:1] = sr[31:1] & sr_in
    sr = bitconcat(bitsliceget(sr, 31, 1), sr_in);
end
```

The following code example shows VHDL process code generated for the `shift_reg_1by32` block.

```
shift_reg_1by32 : PROCESS (shift, sr_in, sr)
    BEGIN
        sr_next <= sr;
        -- MATLAB Function Function 'Subsystem/shift_reg_1by32': '<S2>:1'
        --shift register 1 by 32
        --'<S2>:1:1
        -- return sr[31]
        --'<S2>:1:10'
        sr_out <= sr(31);

        IF shift /= '0' THEN
```

```
--'<S2>:1:12'  
-- sr_new[32:1] = sr[31:1] & sr_in  
--'<S2>:1:14'  
sr_next <= sr(30 DOWNT0 0) & sr_in;  
END IF;  
  
END PROCESS shift_reg_1by32;
```

The Shift Registers/shift\_reg\_1by64 block shows a 64 bit shifter. In this case, the shifter uses two fixed point words, to represent the operand, overcoming the 32-bit word length limitation for fixed-point integers.

Browse the `eml_hdl_design_patterns` model for other useful hardware elements that can be easily implemented using the MATLAB Function block.

## Design Guidelines for the MATLAB Function Block

### In this section...

“Introduction” on page 17-37

“Use Compiled External Functions With MATLAB Function Blocks” on page 17-37

“Build the MATLAB Function Block Code First” on page 17-38

“Use the hdlfimath Utility for Optimized FIMATH Settings” on page 17-38

“Use Optimal Fixed-Point Option Settings” on page 17-40

“Set the Output Data Type of MATLAB Function Blocks Explicitly” on page 17-41

### Introduction

This section describes recommended practices when using the MATLAB Function block for HDL code generation.

By setting MATLAB Function block options as described in this section, you can significantly increase the efficiency of generated HDL code. See “Set Fixed-Point Options for the MATLAB Function Block” on page 17-10 for an example.

### Use Compiled External Functions With MATLAB Function Blocks

The coder supports HDL code generation from MATLAB Function blocks that include compiled external functions. This feature enables you to write reusable MATLAB code and call it from multiple MATLAB Function blocks.

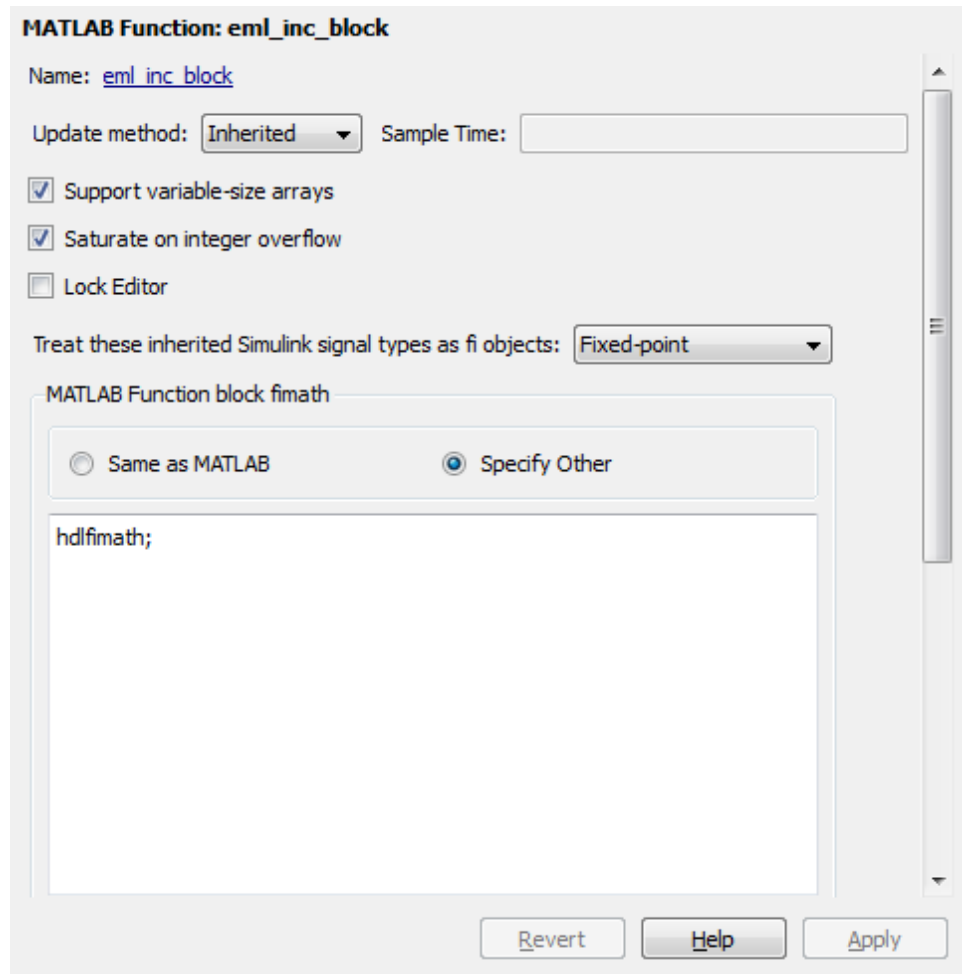
Such functions must be defined in files that are on the MATLAB Function block path. Use the `%#codegen` compilation directive to indicate that the MATLAB code is suitable for code generation. See “Function Definition” for information on how to create, compile, and invoke external functions.

### **Build the MATLAB Function Block Code First**

Before generating HDL code for a subsystem containing a MATLAB Function block, build the MATLAB Function block code to check for errors. To build the code, select **Build** from the **Tools** menu in the MATLAB Function Block Editor (or press **CTRL+B**).

### **Use the `hdlfimath` Utility for Optimized FIMATH Settings**

The `hdlfimath.m` function is a utility that defines a FIMATH specification that is optimized for HDL code generation. Replace the default **MATLAB Function block `fimath`** specification with a call to the `hdlfimath` function, as shown in the following figure.



The following listing shows the FIMATH setting defined by `hdlfimath`.

```
hdlfm = fimath(...  
    'RoundMode', 'floor',...  
    'OverflowMode', 'wrap',...  
    'ProductMode', 'FullPrecision', 'ProductWordLength', 32,...  
    'SumMode', 'FullPrecision', 'SumWordLength', 32,...  
    'CastBeforeSum', true);
```

---

**Note** Use of 'floor' rounding mode for signed integer division will cause an error at code generation time. The HDL division operator does not support 'floor' rounding mode. Use 'round' mode, or else change the signed integer division operations to unsigned integer division.

---

---

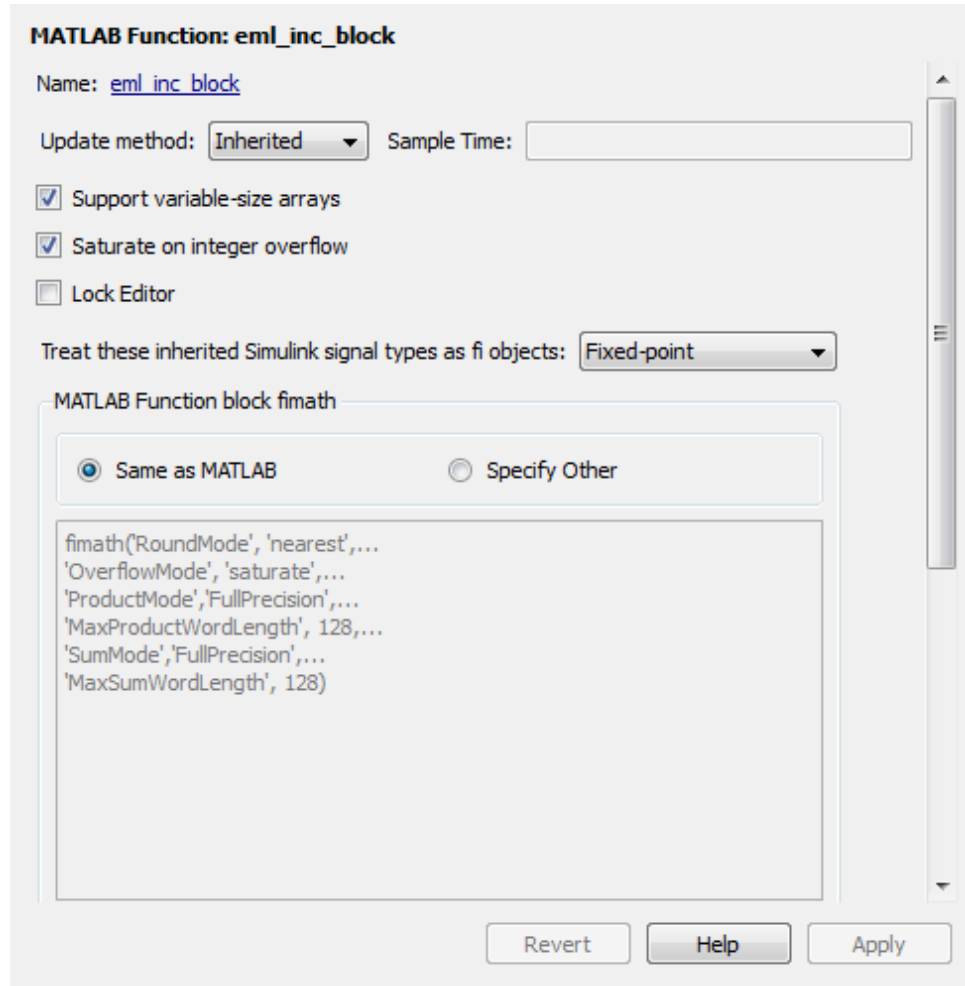
**Note** When the FIMATH OverflowMode property of the FIMATH specification is set to 'Saturate', HDL code generation is disallowed for the following cases:

- SumMode is set to 'SpecifyPrecision'
  - ProductMode is set to 'SpecifyPrecision'
- 

### **Use Optimal Fixed-Point Option Settings**

Use the default (Fixed-point) setting for the **Treat these inherited signal types as fi objects** option, as shown in the following figure.





## Set the Output Data Type of MATLAB Function Blocks Explicitly

By setting the output data type of a MATLAB Function block explicitly, you enable optimizations for RAM mapping and pipelining. Avoid inheriting the output data type for a MATLAB Function block for which you want to enable optimizations.

## Distributed Pipeline Insertion for MATLAB Function Blocks

### In this section...

“Overview” on page 17-42

“Distributed Pipelining in a Multiplier Chain” on page 17-42

### Overview

*Distributed pipeline insertion* is a special optimization for HDL code generated from MATLAB Function blocks or Stateflow charts. Distributed pipeline insertion lets you achieve higher clock rates in your HDL applications, at the cost of some amount of latency caused by the introduction of pipeline registers.

For general information on distributed pipeline insertion, including limitations, see “DistributedPipelining” on page 9-66.

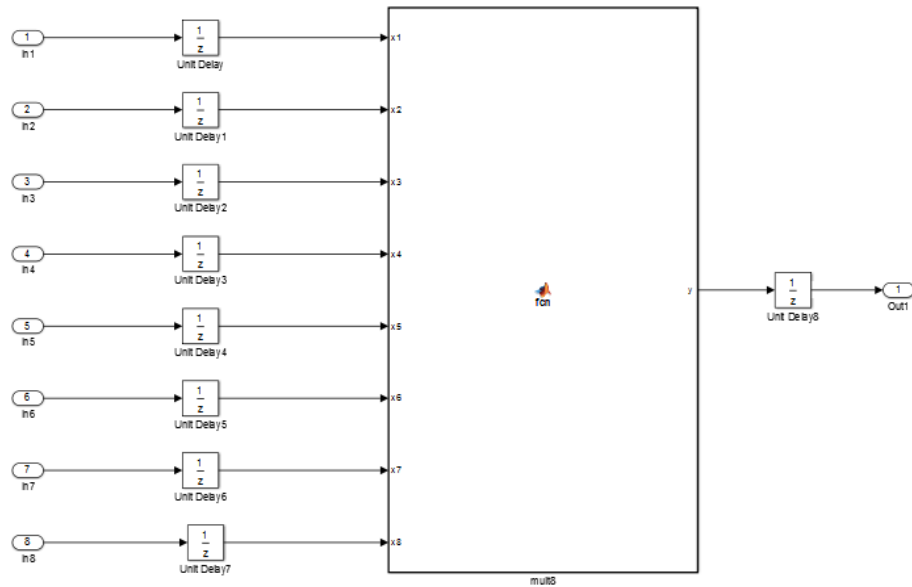
### Distributed Pipelining in a Multiplier Chain

This example shows distributed pipeline insertion in a simple model that implements a chain of 5 multiplications.

To open the model, enter the following:

```
mpipe_multichain
```

The root level model contains a subsystem `multi_chain`. The `multi_chain` subsystem functions as the device under test (DUT) from which to generate HDL code. The subsystem drives a MATLAB Function block, `mult8`. The following figure shows the subsystem.



The following shows a chain of multiplications as coded in the `mul8` MATLAB Function block:

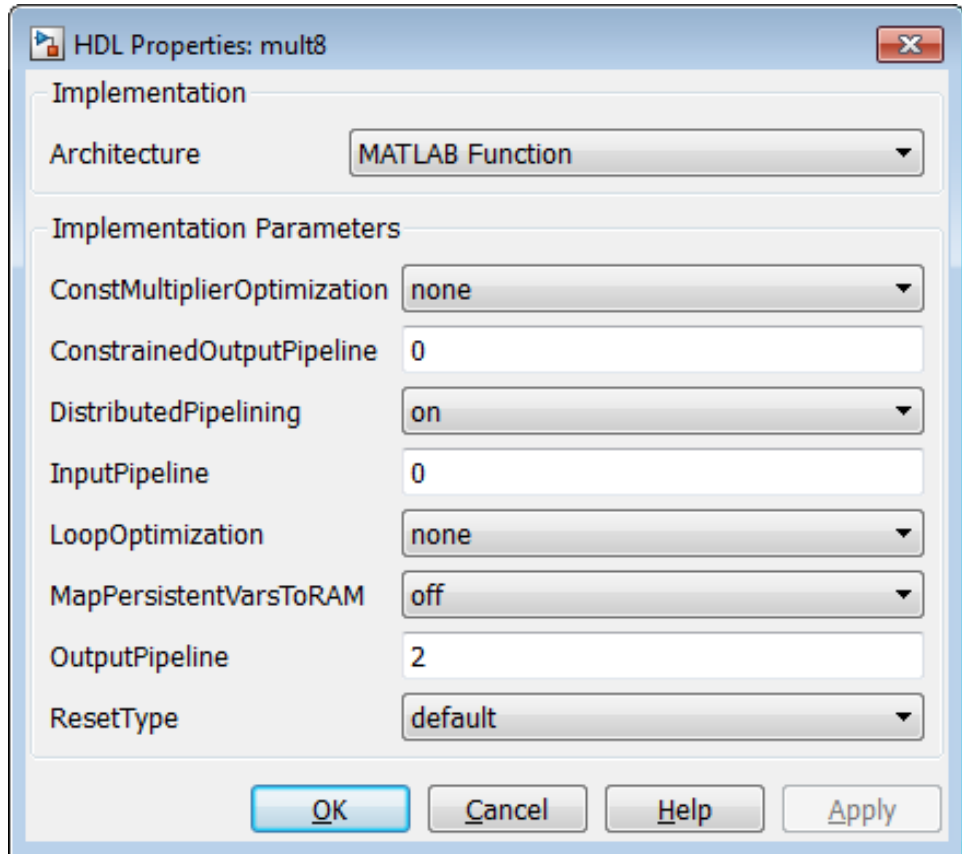
```
function y = fcn(x1,x2,x3,x4,x5,x6,x7,x8)
% A chained multiplication:
% y = (x1*x2)*(x3*x4)*(x5*x6)*(x7*x8)

y1 = x1 * x2;
y2 = x3 * x4;
y3 = x5 * x6;
y4 = x7 * x8;

y5 = y1 * y2;
y6 = y3 * y4;

y = y5 * y6;
```

To apply distributed pipeline insertion to this block, use the HDL Properties dialog box for the `mul8` block. Specify generation of two pipeline stages for the MATLAB Function block, and enable the distributed pipeline optimization:



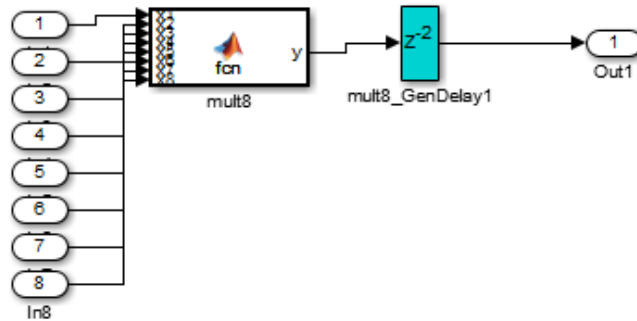
In the Model Configuration Parameters dialog box, the top-level **HDL Code Generation** options specify that:

- VHDL code is generated from the subsystem `mpipe_multchain/mult_chain`.
- The coder will generate code and display the generated model.

The insertion of two pipeline stages into the generated HDL code results in a latency of two clock cycles. In the generated model, a delay of two clock cycles is inserted before the output of the `mpipe_multchain/mult_chain/mult8`

subsystem so that simulations of the model reflect the behavior of the generated HDL code. The following figure shows the inserted Delay block.

gm\_mpipeline\_multichain\_vnl ▶ mult\_chain ▶ mult8 ▶ mult8



The following listing shows the complete architecture section of the generated code. Comments generated by the coder indicate the pipeline register definitions.

```
ARCHITECTURE fsm_SFHDL OF mult8 IS
```

```

SIGNAL pipe_var_0_1 : signed(7 DOWNTO 0); -- Pipeline reg from stage 0 to stage 1
SIGNAL b_pipe_var_0_1 : signed(7 DOWNTO 0); -- Pipeline reg from stage 0 to stage 1
SIGNAL c_pipe_var_0_1 : signed(7 DOWNTO 0); -- Pipeline reg from stage 0 to stage 1
SIGNAL d_pipe_var_0_1 : signed(7 DOWNTO 0); -- Pipeline reg from stage 0 to stage 1
SIGNAL pipe_var_1_2 : signed(7 DOWNTO 0); -- Pipeline reg from stage 1 to stage 2
SIGNAL b_pipe_var_1_2 : signed(7 DOWNTO 0); -- Pipeline reg from stage 1 to stage 2
SIGNAL pipe_var_0_1_next : signed(7 DOWNTO 0);
SIGNAL b_pipe_var_0_1_next : signed(7 DOWNTO 0);
SIGNAL c_pipe_var_0_1_next : signed(7 DOWNTO 0);
SIGNAL d_pipe_var_0_1_next : signed(7 DOWNTO 0);
SIGNAL pipe_var_1_2_next : signed(7 DOWNTO 0);

```

```

SIGNAL b_pipe_var_1_2_next : signed(7 DOWNTO 0);
SIGNAL y1 : signed(7 DOWNTO 0);
SIGNAL y2 : signed(7 DOWNTO 0);
SIGNAL y3 : signed(7 DOWNTO 0);
SIGNAL y4 : signed(7 DOWNTO 0);
SIGNAL y5 : signed(7 DOWNTO 0);
SIGNAL y6 : signed(7 DOWNTO 0);
SIGNAL mul_temp : signed(15 DOWNTO 0);
SIGNAL mul_temp_0 : signed(15 DOWNTO 0);
SIGNAL mul_temp_1 : signed(15 DOWNTO 0);
SIGNAL mul_temp_2 : signed(15 DOWNTO 0);
SIGNAL mul_temp_3 : signed(15 DOWNTO 0);
SIGNAL mul_temp_4 : signed(15 DOWNTO 0);
SIGNAL mul_temp_5 : signed(15 DOWNTO 0);

BEGIN

initialize_mult8 : PROCESS (clk, reset)
BEGIN
    IF reset = '1' THEN
        pipe_var_0_1 <= to_signed(0, 8);
        b_pipe_var_0_1 <= to_signed(0, 8);
        c_pipe_var_0_1 <= to_signed(0, 8);
        d_pipe_var_0_1 <= to_signed(0, 8);
        pipe_var_1_2 <= to_signed(0, 8);
        b_pipe_var_1_2 <= to_signed(0, 8);
    ELSIF clk'EVENT AND clk= '1' THEN
        IF clk_enable= '1' THEN
            pipe_var_0_1 <= pipe_var_0_1_next;
            b_pipe_var_0_1 <= b_pipe_var_0_1_next;
            c_pipe_var_0_1 <= c_pipe_var_0_1_next;
            d_pipe_var_0_1 <= d_pipe_var_0_1_next;
            pipe_var_1_2 <= pipe_var_1_2_next;
            b_pipe_var_1_2 <= b_pipe_var_1_2_next;
        END IF;
    END IF;
END PROCESS initialize_mult8;

-- This block supports an embeddable subset of the MATLAB language.
-- See the help menu for details.
--y = (x1+x2)+(x3+x4)+(x5+x6)+(x7+x8);

```

```
mul_temp <= signed(x1) * signed(x2);

y1 <= "01111111" WHEN (mul_temp(15) = '0') AND (mul_temp(14 DOWNT0 7) /= "00000000")
      ELSE "10000000" WHEN (mul_temp(15) = '1') AND (mul_temp(14 DOWNT0 7) /= "11111111")
      ELSE mul_temp(7 DOWNT0 0);

mul_temp_0 <= signed(x3) * signed(x4);

y2 <= "01111111" WHEN (mul_temp_0(15) = '0') AND (mul_temp_0(14 DOWNT0 7) /= "00000000")
      ELSE "10000000" WHEN (mul_temp_0(15) = '1') AND (mul_temp_0(14 DOWNT0 7) /= "11111111")
      ELSE mul_temp_0(7 DOWNT0 0);

mul_temp_1 <= signed(x5) * signed(x6);

y3 <= "01111111" WHEN (mul_temp_1(15) = '0') AND (mul_temp_1(14 DOWNT0 7) /= "00000000")
      ELSE "10000000" WHEN (mul_temp_1(15) = '1') AND (mul_temp_1(14 DOWNT0 7) /= "11111111")
      ELSE mul_temp_1(7 DOWNT0 0);

mul_temp_2 <= signed(x7) * signed(x8);

y4 <= "01111111" WHEN (mul_temp_2(15) = '0') AND (mul_temp_2(14 DOWNT0 7) /= "00000000")
      ELSE "10000000" WHEN (mul_temp_2(15) = '1') AND (mul_temp_2(14 DOWNT0 7) /= "11111111")
      ELSE mul_temp_2(7 DOWNT0 0);

mul_temp_3 <= pipe_var_0_1 * b_pipe_var_0_1;

y5 <= "01111111" WHEN (mul_temp_3(15) = '0') AND (mul_temp_3(14 DOWNT0 7) /= "00000000")
      ELSE "10000000" WHEN (mul_temp_3(15) = '1') AND (mul_temp_3(14 DOWNT0 7) /= "11111111")
      ELSE mul_temp_3(7 DOWNT0 0);

mul_temp_4 <= c_pipe_var_0_1 * d_pipe_var_0_1;

y6 <= "01111111" WHEN (mul_temp_4(15) = '0') AND (mul_temp_4(14 DOWNT0 7) /= "00000000")
      ELSE "10000000" WHEN (mul_temp_4(15) = '1') AND (mul_temp_4(14 DOWNT0 7) /= "11111111")
      ELSE mul_temp_4(7 DOWNT0 0);

mul_temp_5 <= pipe_var_1_2 * b_pipe_var_1_2;

y <= "01111111" WHEN (mul_temp_5(15) = '0') AND (mul_temp_5(14 DOWNT0 7) /= "00000000")
      ELSE "10000000" WHEN (mul_temp_5(15) = '1') AND (mul_temp_5(14 DOWNT0 7) /= "11111111")
```

```
ELSE std_logic_vector(mul_temp_5(7 DOWNTO 0));

b_pipe_var_1_2_next <= y6;
pipe_var_1_2_next <= y5;
d_pipe_var_0_1_next <= y4;
c_pipe_var_0_1_next <= y3;
b_pipe_var_0_1_next <= y2;
pipe_var_0_1_next <= y1;
END fsm_SFHDL;
```



## Limitations for MATLAB Function Block Code Generation

This section lists other limitations that apply when generating HDL code with the MATLAB Function block.

- The HDL compatibility checker (`checkhdl`) performs only a basic compatibility check on the MATLAB Function block. HDL related warnings or errors may arise during code generation from a MATLAB Function block that is otherwise valid for simulation. Such errors are reported in a separate message window.
- The MATLAB Function block does not support nested functions. Local functions are supported, however. For an example, see “Code Generation from a MATLAB Function Block” on page 17-4.
- Use of multiple values on the left side of an expression is not supported. For example, an error results from the following assignment statement:

```
[t1, t2, t3] = [1, 2, 3];
```

## Complex Data Type Support

### In this section...

“Declaring Complex Signals” on page 17-50

“Conversion Between Complex and Real Signals” on page 17-51

“Arithmetic Operations on Complex Numbers” on page 17-52

“Support for Vectors of Complex Numbers” on page 17-56

“Other Operations on Complex Numbers” on page 17-57

### Declaring Complex Signals

The following MATLAB code declares several local complex variables.  $x$  and  $y$  are declared by complex constant assignment;  $z$  is created using the using the `complex()` function.

```
function [x,y,z] = fcn

% create 8 bit complex constants
x = uint8(1 + 2i);
y = uint8(3 + 4j);
z = uint8(complex(5, 6));
```

The following code example shows VHDL code generated from the previous MATLAB code.

```
ENTITY complex_decl IS
    PORT (
        clk : IN std_logic;
        clk_enable : IN std_logic;
        reset : IN std_logic;
        x_re : OUT std_logic_vector(7 DOWNTO 0);
        x_im : OUT std_logic_vector(7 DOWNTO 0);
        y_re : OUT std_logic_vector(7 DOWNTO 0);
        y_im : OUT std_logic_vector(7 DOWNTO 0);
        z_re : OUT std_logic_vector(7 DOWNTO 0);
        z_im : OUT std_logic_vector(7 DOWNTO 0));
END complex_decl;
```

```

ARCHITECTURE fsm_SFHDH OF complex_decl IS

BEGIN
    x_re <= std_logic_vector(to_unsigned(1, 8));
    x_im <= std_logic_vector(to_unsigned(2, 8));
    y_re <= std_logic_vector(to_unsigned(3, 8));
    y_im <= std_logic_vector(to_unsigned(4, 8));
    z_re <= std_logic_vector(to_unsigned(5, 8));
    z_im <= std_logic_vector(to_unsigned(6, 8));
END fsm_SFHDH;

```

As shown in the example, complex inputs, outputs and local variables declared in MATLAB code expand into real and imaginary signals. The naming conventions for these derived signals are:

- Real components have the same name as the original complex signal, suffixed with the default string `'_re'` (for example, `x_re`). To specify a different suffix, set the **Complex real part postfix** option (or the corresponding `ComplexRealPostfix` CLI property).
- Imaginary components have the same name as the original complex signal, suffixed with the string `'_im'` (for example, `x_im`). To specify a different suffix, set the **Complex imaginary part postfix** option (or the corresponding `ComplexImagPostfix` CLI property).

A complex variable declared in MATLAB code remains complex during the entire length of the program.

## Conversion Between Complex and Real Signals

The MATLAB code provides access to the fields of a complex signal via the `real()` and `imag()` functions, as shown in the following code.

```

function [Re_part, Im_part]= fcn(c)
% Output real and imaginary parts of complex input signal

Re_part = real(c);
Im_part = imag(c);

```

The coder supports these constructs, accessing the corresponding real and imaginary signal components in generated HDL code. In the following Verilog code example, the MATLAB complex signal variable `c` is flattened into the signals `c_re` and `c_im`. Each of these signals is assigned to the output variables `Re_part` and `Im_part`, respectively.

```
module Complex_To_Real_Imag (clk, clk_enable, reset, c_re, c_im, Re_part, Im_part );

    input clk;
    input clk_enable;
    input reset;
    input [3:0] c_re;
    input [3:0] c_im;
    output [3:0] Re_part;
    output [3:0] Im_part;

    // Output real and imaginary parts of complex input signal
    assign Re_part = c_re;
    assign Im_part = c_im;
```

## Arithmetic Operations on Complex Numbers

When generating HDL code, the coder supports the following arithmetic operators for complex numbers composed of base types (integer, fixed-point, double):

- Addition (+)
- Subtraction (-)
- Multiplication (\*)

The coder supports division only for the Fixed-Point Toolbox `divide` function (see `divide`). The `divide` function is supported only if the base type of both complex operands is fixed-point.

As shown in the following example, the default sum and product mode for fixed-point objects is `FullPrecision`, and the `CastBeforeSum` property defaults to `true`.

```
fm = hdlfmath
```

```

fm =

        RoundMode: floor
      OverflowMode: wrap
        ProductMode: FullPrecision
MaxProductWordLength: 128
        SumMode: FullPrecision
MaxSumWordLength: 128
      CastBeforeSum: true

```

Given fixed-point operands, the coder follows full-precision cast before sum semantics. Each addition or subtraction increases the result width by one bit. Further casting is required to bring the results back to a smaller bit width.

In the following example function, two complex operands (with real and imaginary `ufix4` components) are summed, with a complex result having real and imaginary `ufix5` components. The result is then cast back to the original bit width.

```

function z = fcn(x, y)
% addition of two complex numbers x,y of type 'ufix4'

% x+y will have 'ufix5' type
z = x+y;

% to cast the result back to 'ufix4'
% z = fi(x + y, numerictype(x), fimath(x));

```

The following example shows VHDL code generated from this function.

```

ENTITY complex_add_entity IS
  PORT (
    clk : IN std_logic;
    clk_enable : IN std_logic;
    reset : IN std_logic;
    x_re : IN std_logic_vector(3 DOWNTO 0);
    x_im : IN std_logic_vector(3 DOWNTO 0);
    y_re : IN std_logic_vector(3 DOWNTO 0);
    y_im : IN std_logic_vector(3 DOWNTO 0);

```

```
        z_re : OUT std_logic_vector(4 DOWNTO 0);
        z_im : OUT std_logic_vector(4 DOWNTO 0));
END complex_add_entity;

ARCHITECTURE fsm_SFHDL OF complex_add_entity IS

BEGIN
    -- addition of two complex numbers x,y of type 'ufix4'
    -- x+y will have 'ufix5' type
    z_re <= std_logic_vector(resize(unsigned(x_re), 5) +
                            resize(unsigned(y_re), 5));

    z_im <= std_logic_vector(resize(unsigned(x_im), 5) +
                            resize(unsigned(y_im), 5));

    -- to cast the result back to 'ufix4' use
    -- z = fi(x + y, numericity(x), fimath(x));

END fsm_SFHDL;
```

Similarly, for the product operation in FullPrecision mode, the result bit width increases to the sum of the lengths of the individual operands. Further casting is required to bring the results back to a smaller bit width.

The following example function shows how the product of two complex operands (with real and imaginary ufix4 components) can be cast back to the original bit width.

```
function z = fcn(x, y)
% Multiplication of two complex numbers x,y of type 'ufix4'

% x*y will have 'ufix8' type
z = x * y;

% to cast the result back to 'ufix4'
% z = fi(x * y, numericity(x), fimath(x));
```

The following example shows VHDL code generated from this function.

```
ENTITY complex_mul IS
```

```

PORT (
    clk : IN std_logic;
    clk_enable : IN std_logic;
    reset : IN std_logic;
    x_re : IN std_logic_vector(3 DOWNTO 0);
    x_im : IN std_logic_vector(3 DOWNTO 0);
    y_re : IN std_logic_vector(3 DOWNTO 0);
    y_im : IN std_logic_vector(3 DOWNTO 0);
    z_re : OUT std_logic_vector(8 DOWNTO 0);
    z_im : OUT std_logic_vector(8 DOWNTO 0));
END complex_mul;

ARCHITECTURE fsm_SFHDL OF complex_mul IS

    SIGNAL pr1 : unsigned(7 DOWNTO 0);
    SIGNAL pr2 : unsigned(7 DOWNTO 0);
    SIGNAL pr1in : unsigned(8 DOWNTO 0);
    SIGNAL pr2in : unsigned(8 DOWNTO 0);
    SIGNAL pre : unsigned(8 DOWNTO 0);
    SIGNAL pi1 : unsigned(7 DOWNTO 0);
    SIGNAL pi2 : unsigned(7 DOWNTO 0);
    SIGNAL pi1in : unsigned(8 DOWNTO 0);
    SIGNAL pi2in : unsigned(8 DOWNTO 0);
    SIGNAL pim : unsigned(8 DOWNTO 0);

BEGIN
    -- addition of two complex numbers x,y of type 'ufix4'
    -- x*y will have 'ufix8' type
    pr1 <= unsigned(x_re) * unsigned(y_re);
    pr2 <= unsigned(x_im) * unsigned(y_im);
    pr1in <= resize(pr1, 9);
    pr2in <= resize(pr2, 9);
    pre <= pr1in - pr2in;
    pi1 <= unsigned(x_re) * unsigned(y_im);
    pi2 <= unsigned(x_im) * unsigned(y_re);
    pi1in <= resize(pi1, 9);
    pi2in <= resize(pi2, 9);
    pim <= pi1in + pi2in;
    z_re <= std_logic_vector(pre);

```

```
z_im <= std_logic_vector(pim);  
-- to cast the result back to 'ufix4'  
-- z = fi(x * y, numerictype(x), fimath(x));  
END fsm_SFHDL;
```

## Support for Vectors of Complex Numbers

You can generate HDL code for vectors of complex numbers. Like scalar complex numbers, vectors of complex numbers are flattened down to vectors of real and imaginary parts in generated HDL code.

For example in the following script `t` is a complex vector variable of base type `ufix4` and size `[1,2]`.

```
function y = fcn(u1, u2)  
  
t = [u1 u2];  
y = t+1;
```

In the generated HDL code the variable `t` is broken down into real and imaginary parts with the same two-element array. .

```
VARIABLE t_re : vector_of_unsigned4(0 TO 3);  
VARIABLE t_im : vector_of_unsigned4(0 TO 3);
```

The real and imaginary parts of the complex number have the same vector of type `ufix4`, as shown in the following code.

```
TYPE vector_of_unsigned4 IS ARRAY (NATURAL RANGE <>) OF unsigned(3 DOWNT0 0);
```

Complex vector-based operations (+, -, \* etc.) are similarly broken down to vectors of real and imaginary parts. Operations are performed independently on the elements of such vectors, following MATLAB semantics for vectors of complex numbers.

In both VHDL and Verilog code generated from MATLAB code, complex vector ports are always flattened. If complex vector variables appear on inputs and outputs, real and imaginary vector components are further flattened to scalars.



In the following code, `u1` and `u2` are scalar complex numbers and `y` is a vector of complex numbers.

```
function y = fcn(u1, u2)

t = [u1 u2];
y = t+1;
```

This generates the following port declarations in a VHDL entity definition.

```
ENTITY _MATLAB_Function IS
  PORT (
    clk : IN std_logic;
    clk_enable : IN std_logic;
    reset : IN std_logic;
    u1_re : IN vector_of_std_logic_vector4(0 TO 1);
    u1_im : IN vector_of_std_logic_vector4(0 TO 1);
    u2_re : IN vector_of_std_logic_vector4(0 TO 1);
    u2_im : IN vector_of_std_logic_vector4(0 TO 1);
    y_re : OUT vector_of_std_logic_vector32(0 TO 3);
    y_im : OUT vector_of_std_logic_vector32(0 TO 3));
END _MATLAB_Function;
```

## Other Operations on Complex Numbers

The coder supports the following functions with complex operands:

- `complex`
- `real`
- `imag`
- `conj`
- `transpose`
- `ctranspose`
- `isnumeric`
- `isreal`
- `isscalar`

The `isreal` function, which returns 0 for complex numbers, is particularly useful for writing functions that behave differently based on whether the input is a complex or real signal.

```
function y = fcn(u)

% output is same as input if 'u' is real
% output is conjugate of input if 'u' is complex

if isreal(u)
    y = u;
else
    y = conj(u);
end
```

For detailed information on these functions, see “Functions Supported for Code Acceleration or Generation”.

# Operators

## Arithmetic Operators

HDL Coder supports the arithmetic operators (and equivalent MATLAB functions) listed in the following table.

Operation	Operator Syntax	Equivalent Function	Restrictions
Binary addition	A+B	plus(A,B)	Neither A nor B can be data type logical.
Matrix multiplication	A*B	mtimes(A,B)	
Arraywise multiplication	A.*B	times(A,B)	Neither A nor B can be data type logical.
Matrix power	A^B	mpower(A,B)	A and B must be scalar, and B must be an integer.
Arraywise power	A.^B	power(A,B)	A and B must be scalar, and B must be an integer.
Complex transpose	A'	ctranspose(A)	
Matrix transpose	A. '	transpose(A)	
Matrix concat	[A B]	None	
Matrix index	A(r c)	None	Before you use a variable, you must fully define it.

## Relational Operators

HDL Coder supports the relational operators (and equivalent MATLAB functions) listed in the following table.

Relation	Operator Syntax	Equivalent Function
Less than	$A < B$	<code>lt(A,B)</code>
Less than or equal to	$A \leq B$	<code>le(A,B)</code>
Greater than or equal to	$A \geq B$	<code>ge(A,B)</code>
Greater than	$A > B$	<code>gt(A,B)</code>
Equal	$A == B$	<code>eq(A,B)</code>
Not equal	$A \neq B$	<code>ne(A,B)</code>

## Logical Operators

HDL Coder supports the logical operators (and equivalent MATLAB functions) listed in the following table.

Relation	Operator Syntax	M Function Equivalent	Notes
Logical And	$A \& B$	<code>and(A,B)</code>	
Logical Or	$A   B$	<code>or(A,B)</code>	
Logical Xor	$A \text{ xor } B$	<code>xor(A,B)</code>	
Logical And (short circuiting)	$A \&\& B$	N/A	Use short circuiting logical operators within conditionals. See also “Control Flow Statements” on page 17-62.

<b>Relation</b>	<b>Operator Syntax</b>	<b>M Function Equivalent</b>	<b>Notes</b>
Logical Or (short circuiting)	$A \mid B$	N/A	Use short circuiting logical operators within conditionals. See also “Control Flow Statements” on page 17-62.
Element complement	$\sim A$	not(A)	

## Control Flow Statements

HDL Coder supports the following control flow statements and constructs with restrictions.

Control Flow Statement	Restrictions
for	<p>Do not use for loops without static bounds.</p> <p>Do not use the &amp; and   operators within conditions of a for statement. Instead, use the &amp;&amp; and    operators.</p> <p>HDL Coder does not support nonscalar expressions in the conditions of for statements. Instead, use the all or any functions to collapse logical vectors into scalars.</p>
if	<p>Do not use the &amp; and   operators within conditions of an if statement. Instead, use the &amp;&amp; and    operators.</p> <p>HDL Coder does not support nonscalar expressions in the conditions of if statements. Instead, use the all or any functions to collapse logical vectors into scalars.</p>
switch	<p>The conditional expression in a switch or case statement must use only:</p> <ul style="list-style-type: none"> <li>• uint8, uint16, uint32, int8, int16, or int32 data types</li> <li>• Scalar data</li> </ul> <p>If multiple case statements make assignments to the same variable, the numeric type and fimath specification for that variable must be the same in every case statement.</p>

The following control flow statements are not supported:

- while
- break
- continue

- `return`

## **Vector Function Limitations Related to Control Statements**

Avoid using the following vector functions, as they may generate loops containing `break` statements:

- `isequal`
- `bitrevorder`

## Persistent Variables

Persistent variables enable you to model registers. If you need to preserve state between invocations of your MATLAB algorithm, use persistent variables.

Before you use a persistent variable, you must initialize it with a statement specifying its size and type. You can initialize a persistent variable with either a constant value or a variable, as in the following examples:

```
% Initialize with a constant
persistent p;
if isempty(p)
    p = fi(0,0,8,0);
end
```

```
% Initialize with a variable
initval = fi(0,0,8,0);
```

```
persistent p;
if isempty(p)
    p = initval;
end
```

Use a logical expression that evaluates to a constant to test whether a persistent variable has been initialized, as in the preceding examples. Using a logical expression that evaluates to a constant ensures that the generated HDL code for the test is executed only once, as part of the reset process.

You can initialize multiple variables within a single logical expression, as in the following example:

```
% Initialize with variables
initval1 = fi(0,0,8,0);
initval2 = fi(0,0,7,0);
```

```
persistent p;
if isempty(p)
    x = initval1;
    y = initval2;
```



end

---

**Note** If persistent variables are not initialized as described above, extra sentinel variables can appear in the generated code. These sentinel variables can translate to inefficient hardware.

---

### Persistent Array Variables

Persistent array variables enable you to model RAM.

By default, the coder optimizes the area of your design by mapping persistent array variables to RAM. If persistent array variables are not mapped to RAM, they map to registers. RAM mapping can therefore reduce the area of your design in the target hardware.

To learn how persistent array variables map to RAM, see “Map Persistent Arrays and `dsp.Delay` to RAM” on page 4-3.

## Data Types for Variables and Constants

### Supported Data Types

HDL Coder supports the following subset of MATLAB data types.

Types	Supported Data Types	Restrictions
Integer	<ul style="list-style-type: none"> <li>• uint8, uint16, uint32,</li> <li>• int8, int16, int32</li> </ul>	
Real	<ul style="list-style-type: none"> <li>• double</li> <li>• single</li> </ul>	HDL code generated with double or single data types can be used for simulation, but is not synthesizable.
Character	char	
Logical	logical	
Fixed point	<ul style="list-style-type: none"> <li>• Scaled (binary point only) fixed-point numbers</li> <li>• Custom integers (zero binary point)</li> </ul>	<p>Fixed-point numbers with slope (not equal to 1.0) and bias (not equal to 0.0) are not supported.</p> <p>Maximum word size for fixed-point numbers is 128 bits.</p>
Vectors	<ul style="list-style-type: none"> <li>• unordered {N}</li> <li>• row {1, N}</li> <li>• column {N, 1}</li> </ul>	<p>The maximum number of vector elements allowed is <math>2^{32}</math>.</p> <p>Before a variable is subscripted, it must be fully defined.</p>

<b>Types</b>	<b>Supported Data Types</b>	<b>Restrictions</b>
Matrices	{N, M}	Matrices are supported in the body of the design algorithm, but are not supported as inputs to the top-level design function.  Do not use matrices in the testbench.
Structures	struct	Structures are supported in the body of the design algorithm, but are not supported as inputs to the top-level design function.  Do not use structures in the testbench.

## Unsupported Data Types

In the current release, the following data types are not supported:

- Cell array
- Enumeration

## Fixed-Point Bitwise Functions

### In this section...

“Overview” on page 17-69

“Bitwise Functions Supported for HDL Code Generation” on page 17-69

### Overview

HDL Coder supports many bitwise functions that operate on fixed-point integers of arbitrary length. For more information about these bitwise functions, see “Bitwise Operations” in the Fixed-Point Toolbox documentation.

This section describes HDL code generation support for these functions. “Bitwise Functions Supported for HDL Code Generation” on page 17-69 summarizes the supported functions, with notes that describe considerations specific to HDL code generation. “Bit Slicing and Bit Concatenation” on page 1-46 and “Shift and Rotate Without Saturation Or Rounding Logic” on page 1-43 provide usage examples, with corresponding MATLAB and generated HDL code.

### Bitwise Functions Supported for HDL Code Generation

The following table summarizes MATLAB bitwise functions that are supported for HDL code generation. The Description column notes considerations that are specific to HDL. The following conventions are used in the table:

- *a, b*: Denote fixed-point integer operands.
- *idx*: Denotes an index to a bit within an operand. Indexes can be scalar or vector, depending on the function.

MATLAB code uses 1-based indexing conventions. In generated HDL code, such indexes are converted to zero-based indexing conventions.

- *lidx*, *ridx*: denote indexes to the left and right boundaries delimiting bit fields. Indexes can be scalar or vector, depending on the function.
- *val*: Denotes a Boolean value.

**Note** Indexes, operands, and values passed as arguments bitwise functions can be scalar or vector, depending on the function. For information on the individual functions, see “Bitwise Operations” in the Fixed-Point Toolbox documentation.

<b>MATLAB Syntax</b>	<b>Description</b>	<b>See Also</b>
<code>bitand(a, b)</code>	Bitwise AND	<code>bitand</code>
<code>bitandreduce(a, lidx, ridx)</code>	<p>Bitwise AND of a field of consecutive bits within <code>a</code>. The field is delimited by <code>lidx</code>, <code>ridx</code>.</p> <p>Output data type: <code>ufix1</code></p> <p>For VHDL, generates the bitwise AND operator operating on a set of individual slices</p> <p>For Verilog, generates the reduce operator:</p> <p><code>&amp;a[lidx:ridx]</code></p>	<code>bitandreduce</code>
<code>bitcmp(a)</code>	Bitwise complement	<code>bitcmp</code>
<code>bitconcat(a, b)</code> <code>bitconcat([a_vector])</code> <code>bitconcat(a, b, c, d, ...)</code>	<p>Concatenate fixed-point operands. Operands can be of different signs.</p> <p>Output data type: <code>ufixN</code>, where <code>N</code> is the sum of the word lengths of <code>a</code> and <code>b</code>.</p> <p>For VHDL, generates the concatenation operator: <code>(a &amp; b)</code></p> <p>For Verilog, generates the concatenation operator: <code>{a , b}</code></p>	<code>bitconcat</code>

<b>MATLAB Syntax</b>	<b>Description</b>	<b>See Also</b>
<code>bitget(a,idx)</code>	Access a bit at position <code>idx</code> . For VHDL, generates the slice operator: <code>a(idx)</code> For Verilog, generates the slice operator: <code>a[idx]</code>	<code>bitget</code>
<code>bitor(a, b)</code>	Bitwise OR	<code>bitor</code>
<code>bitorreduce(a, lidx, ridx)</code>	Bitwise OR of a field of consecutive bits within <code>a</code> . The field is delimited by <code>lidx</code> and <code>ridx</code> . Output data type: <code>ufix1</code> For VHDL, generates the bitwise OR operator operating on a set of individual slices. For Verilog, generates the reduce operator: <code> a[lidx:ridx]</code>	<code>bitorreduce</code>
<code>bitset(a, idx, val)</code>	Set or clear bit(s) at position <code>idx</code> . If <code>val = 0</code> , clears the indicated bit(s). Otherwise, sets the indicated bits.	<code>bitset</code>
<code>bitreplicate(a, n)</code>	Concatenate bits of <code>fi</code> object <code>a</code> <code>n</code> times	<code>bitreplicate</code>

<b>MATLAB Syntax</b>	<b>Description</b>	<b>See Also</b>
<code>bitrol(a, idx)</code>	<p>Rotate left.</p> <p><code>idx</code> must be a positive integer. The value of <code>idx</code> can be greater than the word length of <code>a</code>. <code>idx</code> is normalized to <code>mod(idx, wlen)</code>. <code>wlen</code> is the word length of <code>a</code>.</p> <p>For VHDL, generates the <code>rol</code> operator.</p> <p>For Verilog, generates the following expression (where <code>wl</code> is the word length of <code>a</code>):</p> $a \ll idx \    \ a \gg wl - idx$	<code>bitrol</code>
<code>bitror(a, idx)</code>	<p>Rotate right.</p> <p><code>idx</code> must be a positive integer. The value of <code>idx</code> can be greater than the word length of <code>a</code>. <code>idx</code> is normalized to <code>mod(idx, wlen)</code>. <code>wlen</code> is the word length of <code>a</code>.</p> <p>For VHDL, generates the <code>ror</code> operator.</p> <p>For Verilog, generates the following expression (where <code>wl</code> is the word length of <code>a</code>):</p> $a \gg idx \    \ a \ll wl - idx$	<code>bitror</code>
<code>bitset(a, idx, val)</code>	<p>Set or clear bit(s) at position <code>idx</code>.</p> <p>If <code>val = 0</code>, clears the indicated bit(s). Otherwise, sets the indicated bits.</p>	<code>bitset</code>



MATLAB Syntax	Description	See Also
bitshift(a, idx)	<p><b>Note:</b> For efficient HDL code generation, use bitsll, bitsrl, or bitsra <i>instead</i> of bitshift.</p> <p>Shift left or right, based on the positive or negative integer value of <code>idx</code>.</p> <p><code>idx</code> must be an integer.</p> <p>For positive values of <code>idx</code>, shift left <code>idx</code> bits.</p> <p>For negative values of <code>idx</code>, shift right <code>idx</code> bits.</p> <p>If <code>idx</code> is a variable, generated code contains logic for both left shift and right shift.</p> <p>Result values saturate if the <code>overflowMode</code> of <code>a</code> is set to saturate.</p>	bitshift
bitsliceget(a, lidx, ridx)	<p>Access consecutive set of bits from <code>lidx</code> to <code>ridx</code>.</p> <p>Output data type: <code>ufixN</code>, where <math>N = \text{ridx} - \text{lidx} + 1</math>.</p>	bitsliceget
bitsll(a, idx)	<p>Shift left logical.</p> <p><code>idx</code> must be a scalar within the range</p> $0 \leq \text{idx} < \text{wl}$ <p><code>wl</code> is the word length of <code>a</code>.</p> <p>Overflow and rounding modes of input operand <code>a</code> are ignored.</p> <p>Generates <code>sll</code> operator in VHDL.</p> <p>Generates <code>&lt;&lt;</code> operator in Verilog.</p>	bitsll

<b>MATLAB Syntax</b>	<b>Description</b>	<b>See Also</b>
<code>bitsra(a, idx)</code>	<p>Shift right arithmetic.</p> <p><code>idx</code> must be a scalar within the range</p> $0 \leq \text{idx} < w1$ <p><code>w1</code> is the word length of <code>a</code>,</p> <p>Overflow and rounding modes of input operand <code>a</code> are ignored.</p> <p>Generates <code>sra</code> operator in VHDL.</p> <p>Generates <code>&gt;&gt;&gt;</code> operator in Verilog.</p>	<code>bitsra</code>
<code>bitsrl(a, idx)</code>	<p>Shift right logical.</p> <p><code>idx</code> must be a scalar within the range</p> $0 \leq \text{idx} < w1$ <p><code>w1</code> is the word length of <code>a</code>.</p> <p>Overflow and rounding modes of input operand <code>a</code> are ignored.</p> <p>Generates <code>srl</code> operator in VHDL.</p> <p>Generates <code>&gt;&gt;</code> operator in Verilog.</p>	<code>bitsrl</code>
<code>bitxor(a, b)</code>	Bitwise XOR	<code>bitxor</code>

<b>MATLAB Syntax</b>	<b>Description</b>	<b>See Also</b>
<code>bitxorreduce(a, lidx, ridx)</code>	<p>Bitwise XOR reduction.</p> <p>Bitwise XOR of a field of consecutive bits within <code>a</code>. The field is delimited by <code>lidx</code> and <code>ridx</code>.</p> <p>Output data type: <code>ufix1</code></p> <p>For VHDL, generates a set of individual slices.</p> <p>For Verilog, generates the reduce operator:</p> <p><code>^a[lidx:ridx]</code></p>	<code>bitxorreduce</code>
<code>getlsb(a)</code>	Return value of LSB.	<code>getlsb</code>
<code>getmsb(a)</code>	Return value of MSB.	<code>getmsb</code>

## Fixed-Point Run-Time Library Functions

HDL code generation support for fixed-point run-time library functions from the Fixed-Point Toolbox is summarized in the following table. See “Fixed-Point Function Limitations” on page 17-85 for general limitations of fixed-point run-time library functions for code generation.

Function	Restrictions
abs	N/A
add	N/A
all	N/A
any	N/A
bitand	Not supported for slope-bias scaled <code>fi</code> objects.
bitandreduce	N/A
bitcmp	N/A
bitconcat	N/A
bitget	N/A
bitor	Not supported for slope-bias scaled <code>fi</code> objects.
bitorreduce	N/A
bitreplicate	N/A
bitrol	N/A
bitror	N/A
bitset	N/A
bitshift	N/A
bitsliceget	N/A
bitsll	N/A
bitsra	N/A
bitsrl	N/A
bitxor	Not supported for slope-bias scaled <code>fi</code> objects.

<b>Function</b>	<b>Restrictions</b>
bitxorreduce	N/A
ceil	N/A
complex	N/A
conj	N/A
conv	<ul style="list-style-type: none"> <li>• Variable-sized inputs are only supported when the <code>SumMode</code> property of the governing <code>fimath</code> is set to <code>Specify precision</code> or <code>Keep LSB</code>.</li> <li>• For variable-sized signals, you may see different results between generated code and MATLAB. <ul style="list-style-type: none"> <li>▪ In the generated code, the output for variable-sized signals is always computed using the <code>SumMode</code> property of the governing <code>fimath</code>.</li> <li>▪ In MATLAB, the output for variable-sized signals is computed using the <code>SumMode</code> property of the governing <code>fimath</code> when both inputs are nonscalar. However, if either input is a scalar, MATLAB computes the output using the <code>ProductMode</code> of the governing <code>fimath</code>.</li> </ul> </li> </ul>
convergent	N/A
cordicabs	Variable-size signals are not supported.
cordicangle	Variable-size signals are not supported.
cordicatan2	Variable-size signals are not supported.
cordiccart2pol	Variable-size signals are not supported.
cordiccxp	Variable-size signals are not supported.
cordiccos	Variable-size signals are not supported.
cordicpol2cart	Variable-size signals are not supported.
cordicrotate	Variable-size signals are not supported.
cordicsin	Variable-size signals are not supported.

<b>Function</b>	<b>Restrictions</b>
cordicsincos	Variable-size signals are not supported.
ctranspose	N/A
diag	If supplied, the index, $k$ , must be a real and scalar integer value that is not a <code>fi</code> object.
disp	Not supported for HDL code generation.
divide	<ul style="list-style-type: none"> <li>• For HDL Code generation, the divisor must be a constant and a power of two.</li> <li>• Any non-<code>fi</code> input must be constant; that is, its value must be known at compile time so that it can be cast to a <code>fi</code> object.</li> <li>• Complex and imaginary divisors are not supported.</li> <li>• Code generation in MATLAB does not support the syntax <code>T.divide(a,b)</code>.</li> </ul>
double	N/A
end	N/A
eps	<ul style="list-style-type: none"> <li>• Supported for scalar fixed-point signals only.</li> <li>• Supported for scalar, vector, and matrix, <code>fi</code> single and <code>fi</code> double signals.</li> </ul>
eq	Not supported for fixed-point signals with different biases.

Function	Restrictions
fi	<ul style="list-style-type: none"> <li>• Use to create a fixed-point constant or variable in the generated code.</li> <li>• The default constructor syntax without any input arguments is not supported.</li> <li>• The syntax <code>fi('PropertyName',PropertyValue...)</code> is not supported. To use property name/property value pairs, you must first specify the value <code>v</code> of the <code>fi</code> object as in <code>fi(v,'PropertyName',PropertyValue...)</code>.</li> <li>• Works for all input values when complete <code>numericType</code> information of the <code>fi</code> object is provided.</li> <li>• Works only for constant input values (value of input must be known at compile time) when complete <code>numericType</code> information of the <code>fi</code> object is not specified.</li> <li>• <code>numericType</code> object information must be available for nonfixed-point Simulink inputs.</li> </ul>
fimath	<ul style="list-style-type: none"> <li>• Fixed-point signals coming in to a MATLAB Function block from Simulink are assigned a <code>fimath</code> object. You define this object in the MATLAB Function block dialog in the Model Explorer.</li> <li>• Use to create <code>fimath</code> objects in the generated code.</li> </ul>
fix	N/A
floor	N/A
ge	Not supported for fixed-point signals with different biases.
get	Not supported for HDL code generation.
getlsb	N/A

<b>Function</b>	<b>Restrictions</b>
getmsb	N/A
gt	Not supported for fixed-point signals with different biases.
horzcat	N/A
imag	N/A
int8, int16, int32	N/A
iscolumn	N/A
isempty	N/A
isequal	N/A
isfi	N/A
isfimath	N/A
isfimathlocal	N/A
isfinite	N/A
isinf	N/A
isnan	N/A
isnumeric	N/A
isnumericitype	N/A
isreal	N/A
isrow	N/A
isscalar	N/A
assigned	N/A
isvector	N/A
le	Not supported for fixed-point signals with different biases.
length	N/A
logical	N/A
lowerbound	N/A



Function	Restrictions
lsb	<ul style="list-style-type: none"> <li>• Supported for scalar fixed-point signals only.</li> <li>• Supported for scalar, vector, and matrix, <code>fi</code> single and double signals.</li> </ul>
lt	Not supported for fixed-point signals with different biases.
max	N/A
mean	N/A
median	N/A
min	N/A
minus	Any non- <code>fi</code> input must be constant; that is, its value must be known at compile time so that it can be cast to a <code>fi</code> object.
mpower	<ul style="list-style-type: none"> <li>• The exponent input, <code>k</code>, must be constant; that is, its value must be known at compile time.</li> <li>• Variable-sized inputs are only supported when the <code>SumMode</code> property of the governing <code>fimath</code> is set to <code>Specify precision</code> or <code>Keep LSB</code>.</li> <li>• For variable-sized signals, you may see different results between the generated code and MATLAB. <ul style="list-style-type: none"> <li>▪ In the generated code, the output for variable-sized signals is always computed using the <code>SumMode</code> property of the governing <code>fimath</code>.</li> <li>▪ In MATLAB, the output for variable-sized signals is computed using the <code>SumMode</code> property of the governing <code>fimath</code> when the first input, <code>a</code>, is nonscalar. However, when <code>a</code> is a scalar, MATLAB computes the output using the <code>ProductMode</code> of the governing <code>fimath</code>.</li> </ul> </li> </ul>

Function	Restrictions
mpy	<p>When you provide complex inputs to the mpy function inside of a MATLAB Function block, you must declare the input as complex before running the simulation. To do so, go to the <b>Ports and data manager</b> and set the <b>Complexity</b> parameter for all known complex inputs to On.</p>
mrdivide	N/A
mtimes	<ul style="list-style-type: none"> <li>• Any non-fi input must be constant; that is, its value must be known at compile time so that it can be cast to a fi object.</li> <li>• Variable-sized inputs are only supported when the SumMode property of the governing fimath is set to Specify precision or Keep LSB.</li> <li>• For variable-sized signals, you may see different results between the generated code and MATLAB. <ul style="list-style-type: none"> <li>▪ In the generated code, the output for variable-sized signals is always computed using the SumMode property of the governing fimath.</li> <li>▪ In MATLAB, the output for variable-sized signals is computed using the SumMode property of the governing fimath when both inputs are nonscalar. However, if either input is a scalar, MATLAB computes the output using the ProductMode of the governing fimath.</li> </ul> </li> </ul>
ndims	N/A
ne	Not supported for fixed-point signals with different biases.
nearest	N/A

<b>Function</b>	<b>Restrictions</b>
<code>numberofelements</code>	<code>numberofelements</code> and <code>numel</code> both work the same as MATLAB <code>numel</code> for <code>fi</code> objects in the generated code.
<code>numerictype</code>	<ul style="list-style-type: none"> <li>Fixed-point signals coming in to a MATLAB Function block from Simulink are assigned a <code>numerictype</code> object that is populated with the signal's data type and scaling information.</li> <li>Returns the data type when the input is a nonfixed-point signal.</li> <li>Use to create <code>numerictype</code> objects in generated code.</li> </ul>
<code>permute</code>	N/A
<code>plus</code>	Any non- <code>fi</code> input must be constant; that is, its value must be known at compile time so that it can be cast to a <code>fi</code> object.
<code>pow2</code>	Not supported for HDL code generation.
<code>power</code>	The exponent input, $k$ , must be constant; that is, its value must be known at compile time.
<code>range</code>	N/A
<code>rdivide</code>	N/A
<code>real</code>	Not supported for HDL code generation.
<code>realmax</code>	N/A
<code>realmin</code>	N/A
<code>reinterpretcast</code>	N/A
<code>repmat</code>	N/A
<code>rescale</code>	N/A
<code>reshape</code>	N/A
<code>round</code>	N/A
<code>sfi</code>	N/A

<b>Function</b>	<b>Restrictions</b>
sign	N/A
single	N/A
size	N/A
sort	N/A
sqrt	<ul style="list-style-type: none"> <li>• Complex and [Slope Bias] inputs error out.</li> <li>• Negative inputs yield a 0 result.</li> </ul>
storedInteger	N/A
storedIntegerToDouble	N/A
sub	N/A
subasgn	Supported data types for HDL code generation are listed in “Supported Data Types” on page 17-67
subref	Supported data types for HDL code generation are listed in “Supported Data Types” on page 17-67
sum	Variable-sized inputs are only supported when the SumMode property of the governing fimath is set to Specify precision or Keep LSB.
times	<ul style="list-style-type: none"> <li>• Any non-fi input must be constant; that is, its value must be known at compile time so that it can be cast to a fi object.</li> <li>• When you provide complex inputs to the times function inside of a MATLAB Function block, you must declare the input as complex before running the simulation. To do so, go to the <b>Ports and data manager</b> and set the <b>Complexity</b> parameter for all known complex inputs to 0n.</li> </ul>
transpose	N/A
tril	If supplied, the index, $k$ , must be a real and scalar integer value that is not a fi object.
triu	If supplied, the index, $k$ , must be a real and scalar integer value that is not a fi object.

Function	Restrictions
<code>ufi</code>	N/A
<code>uint8, uint16, uint32</code>	N/A
<code>uminus</code>	N/A
<code>uplus</code>	N/A
<code>upperbound</code>	N/A
<code>vertcat</code>	N/A

## Fixed-Point Function Limitations

In addition to any function-specific limitations listed in the table, the following general limitations always apply to the use of Fixed-Point Toolbox functions in generated code or with `fiaccel`:

- `fipref` and quantizer objects are not supported.
- Dot notation is only supported for getting the values of `fimath` and `numericType` properties. Dot notation is not supported for `fi` objects, and it is not supported for setting properties.
- Word lengths greater than 128 bits are not supported.
- You cannot change the `fimath` or `numericType` of a given variable after that variable has been created.
- The `boolean` and `ScaledDouble` values of the `DataTypeMode` and `DataType` properties are not supported.
- For all `SumMode` property settings other than `FullPrecision`, the `CastBeforeSum` property must be set to `true`.
- The `numel` function returns the number of elements of `fi` objects in the generated code.
- When you compile code containing `fi` objects with nontrivial slope and bias scaling, you may see different results in generated code than you achieve by running the same code in MATLAB.

- All general limitations of C/C++ code generated from MATLAB apply. See “MATLAB Language Features Not Supported for C/C++ Code Generation” for more information.

# Generating Scripts for HDL Simulators and Synthesis Tools

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- “Script Generation for EDA Tools” on page 18-2
- “Script Generation Defaults” on page 18-3
- “Generate Scripts for Compilation, Simulation, and Synthesis” on page 18-4

### **Script Generation for EDA Tools**

The coder supports generation of script files for third-party electronic design automation (EDA) tools. These scripts let you compile and simulate generated HDL code or synthesize generated HDL code.

Using the defaults, you can automatically generate scripts for the Mentor Graphics ModelSim simulator.

Optionally, you can also generate scripts for a variety of synthesis tools.



## Script Generation Defaults

By default, script generation takes place automatically, as part of the code and test bench generation process.

The coder generates script files in the target folder.

When you generate HDL code for a model or subsystem *system*, the coder writes the following script files:

- `system_compile.do`: Mentor Graphics ModelSim compilation script. This script contains commands to compile the generated code, but not to simulate it.

When you generate test bench code for a model or subsystem *system*, the coder writes the following script files:

- `system_tb_compile.do`: Mentor Graphics ModelSim compilation script. This script contains commands to compile the generated code and test bench.
- `system_tb_sim.do`: Mentor Graphics ModelSim simulation script. This script contains commands to run a simulation of the generated code and test bench.

By default, the coder does not generate a synthesis script. To enable synthesis script generation, select a synthesis tool from the **Choose synthesis tool** pulldown menu, as described in “Synthesis Script Options” on page 18-14.

## Generate Scripts for Compilation, Simulation, and Synthesis

### In this section...

“Overview” on page 18-4

“Structure of Generated Script Files” on page 18-4

“Properties for Controlling Script Generation” on page 18-5

“Controlling Script Generation with the EDA Tool Scripts Pane” on page 18-9

### Overview

You can enable or disable script generation and customize the names and content of generated script files using either of the following methods:

- Use the `makehdl` or `makehdltb` functions, and pass in property name/property value arguments, as described in “Properties for Controlling Script Generation” on page 18-5.
- Set script generation options in the **HDL Code > EDA Tool Scripts** pane of the Model Configuration Parameters dialog box, as described in “Controlling Script Generation with the EDA Tool Scripts Pane” on page 18-9.

### Structure of Generated Script Files

A generated EDA script consists of three sections, generated and executed in the following order:

- 1** An initialization (`Init`) phase. The `Init` phase performs the required setup actions, such as creating a design library or a project file. Some arguments to the `Init` phase are implicit, for example, the top-level entity or module name.
- 2** A command-per-file phase (`Cmd`). This phase of the script is called iteratively, once per generated HDL file or once per signal. On each call, a different file or signal name is passed in.

- 3 A termination phase (`Term`). This is the final execution phase of the script. One application of this phase is to execute a simulation of HDL code that was compiled in the `Cmd` phase. The `Term` phase does not take arguments.

The coder generates scripts by passing format strings to the `fprintf` function. Using the GUI options (or `makehdl` and `makehdltb` properties) summarized in the following sections, you can pass in customized format strings to the script generator. Some of these format strings take arguments, such as the top-level entity or module name, or the names of the VHDL or Verilog files in the design.

You can use valid `fprintf` formatting characters. For example, `'\n'` inserts a newline into the script file.

## Properties for Controlling Script Generation

This section describes how to set properties in the `makehdl` or `makehdltb` functions to enable or disable script generation and customize the names and content of generated script files.

### Enabling and Disabling Script Generation

The `EDAScriptGeneration` property controls the generation of script files. By default, `EDAScriptGeneration` is set `'on'`. To disable script generation, set `EDAScriptGeneration` to `'off'`, as in the following example.

```
makehdl('sfir_fixed/symmetric_fir','EDAScriptGeneration','off')
```

### Customizing Script Names

When you generate HDL code, script names are generated by appending a postfix string to the model or subsystem name *system*.

When you generate test bench code, script names are generated by appending a postfix string to the test bench name *testbench\_tb*.

The postfix string depends on the type of script (compilation, simulation, or synthesis) being generated. The default postfix strings are shown in the following table. For each type of script, you can define your own postfix using the associated property.

Script Type	Property	Default Value
Compilation	'HDLCompileFilePostfix'	'_compile.do'
Simulation	'HDLSimFilePostfix'	'_sim.do'
Synthesis	'HDLSynthFilePostfix'	Depends on the selected synthesis tool. See HDLSynthTool.

The following command generates VHDL code for the subsystem `system`, specifying a custom postfix string for the compilation script. The name of the generated compilation script will be `system_test_compilation.do`.

```
makehdl('mymodel/system', 'HDLCompileFilePostfix', '_test_compilation.do')
```

### Customizing Script Code

Using the property name/property value pairs summarized in the following table, you can pass in customized format strings to `makehdl` or `makehdltb`. The properties are named according to the following conventions:

- Properties that apply to the initialization (`Init`) phase are identified by the substring `Init` in the property name.
- Properties that apply to the command-per-file phase (`Cmd`) are identified by the substring `Cmd` in the property name.
- Properties that apply to the termination (`Term`) phase are identified by the substring `Term` in the property name.

Property Name and Default	Description
Name: 'HDLCompileInit' Default: 'vlib %s\n'	Format string passed to <code>fprintf</code> to write the <code>Init</code> section of the compilation script. The argument is the contents of the 'VHDLLibraryName' property, which defaults to 'work'. You can override the default <code>Init</code> string ('vlib work\n' by changing the value of 'VHDLLibraryName'.
Name: 'HDLCompileVHDLCmd'	Format string passed to <code>fprintf</code> to write the <code>Cmd</code> section of the compilation script for VHDL files. The two arguments are the contents of the

Property Name and Default	Description
Default: 'vcom %s %s\n'	'SimulatorFlags' property and the file name of the current entity or module. To omit the flags, set 'SimulatorFlags' to '' (the default).
Name: 'HDLCompileVerilogCmd' Default: 'vlog %s %s\n'	Format string passed to fprintf to write the Cmd section of the compilation script for Verilog files. The two arguments are the contents of the 'SimulatorFlags' property and the file name of the current entity or module. To omit the flags, set 'SimulatorFlags' to '' (the default).
Name: 'HDLCompileTerm' Default: ''	Format string passed to fprintf to write the termination portion of the compilation script.
Name: 'HDLSimInit' Default:  ['onbreak resume\n',... 'onerror resume\n']	Format string passed to fprintf to write the initialization section of the simulation script.
Name: 'HDLSimCmd' Default: 'vsim -novopt work.%s\n'	Format string passed to fprintf to write the simulation command. The implicit argument is the top-level module or entity name.
Name: 'HDLSimViewWaveCmd' Default: 'add wave sim:%s\n'	Format string passed to fprintf to write the simulation script waveform viewing command. The implicit argument is the top-level module or entity name.
Name: 'HDLSimTerm' Default: 'run -all\n'	Format string passed to fprintf to write the Term portion of the simulation script. The string is a synthesis project creation command. The implicit argument is the top-level module or entity name.
	The content of the string is specific to the selected synthesis tool. See HDLSynthTool.

Property Name and Default	Description
Name: 'HDLSynthInit'	Format string passed to <code>fprintf</code> to write the <code>Init</code> section of the synthesis script. The content of the string is specific to the selected synthesis tool. See <code>HDLSynthTool</code> .
Name: 'HDLSynthCmd'	Format string passed to <code>fprintf</code> to write the <code>Cmd</code> section of the synthesis script. The argument is the file name of the entity or module. The content of the string is specific to the selected synthesis tool. See <code>HDLSynthTool</code> .
Name: 'HDLSynthTerm'	Format string passed to <code>fprintf</code> to write the <code>Term</code> section of the synthesis script. The content of the string is specific to the selected synthesis tool. See <code>HDLSynthTool</code> .

### Examples

The following example specifies a Mentor Graphics ModelSim command for the `Init` phase of a compilation script for VHDL code generated from the subsystem `system`.

```
makehdl(system, 'HDLCompileInit', 'vlib mydesignlib\n')
```

The following example lists the resultant script, `system_compile.do`.

```
vlib mydesignlib
vcom system.vhd
```

The following example specifies that the coder generate a Xilinx ISE synthesis file for the subsystem `sfir_fixed/symmetric_fir`.

```
makehdl('sfir_fixed/symmetric_fir', 'HDLSynthTool', 'ISE')
```

The following listing shows the resultant script, `symmetric_fir_ise.tcl`.

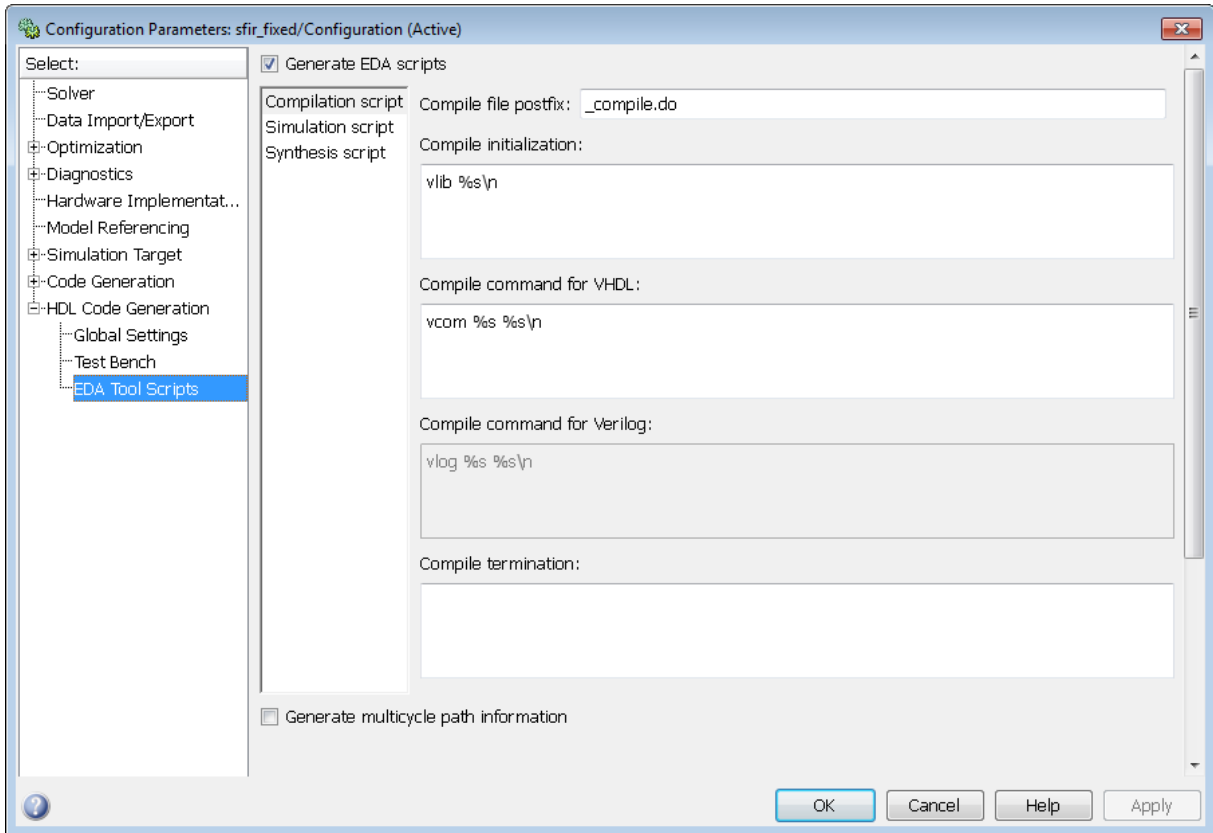
```
set src_dir "./hdlsrc"
set prj_dir "synprj"
file mkdir ../$prj_dir
cd ../$prj_dir
project new symmetric_fir_ise
xfile add ../$src_dir/symmetric_fir.vhd
project set family Virtex4
project set device xc4vsx35
project set package ff668
project set speed -10
process run "Synthesize - XST"
```

## Controlling Script Generation with the EDA Tool Scripts Pane

You set options that control generation of script files on the **EDA Tool Scripts** pane. These options correspond to the properties described in “Properties for Controlling Script Generation” on page 18-5.

To view and set **EDA Tool Scripts** options:

- 1 Open the Model Configuration Parameters dialog box.
- 2 Select the **HDL Code > EDA Tool Scripts** pane.



**3** The **Generate EDA scripts** option controls the generation of script files. By default, this option is selected.

If you want to disable script generation, clear this check box and click **Apply**.

**4** The list on the left of the **EDA Tool Scripts** pane lets you select from several categories of options. Select a category and set the options as desired. The categories are:

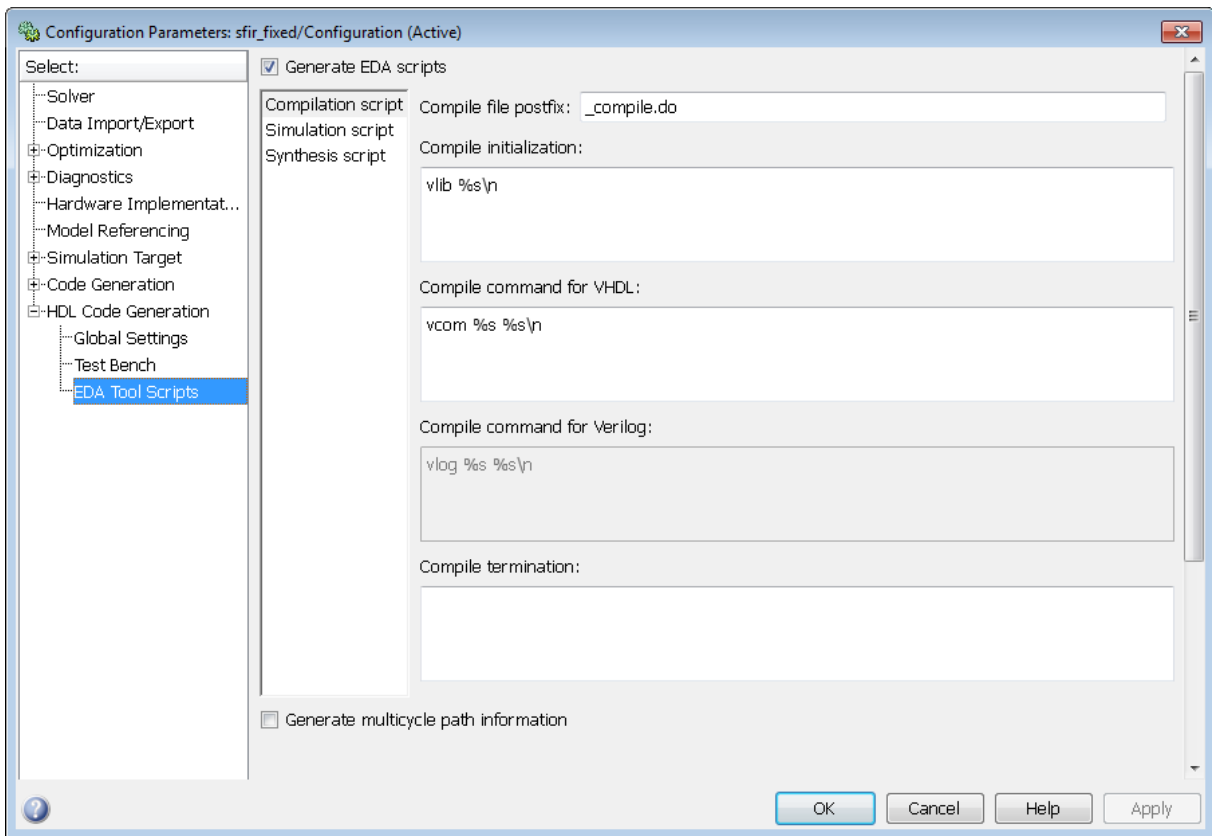
- **Compilation script:** Options related to customizing scripts for compilation of generated VHDL or Verilog code. See “Compilation Script Options” on page 18-11 for further information.



- **Simulation script:** Options related to customizing scripts for HDL simulators. See “Simulation Script Options” on page 18-12 for further information.
- **Synthesis script:** Options related to customizing scripts for synthesis tools. See “Synthesis Script Options” on page 18-14 for further information.

## Compilation Script Options

The following figure shows the **Compilation script** pane, with options set to their default values.

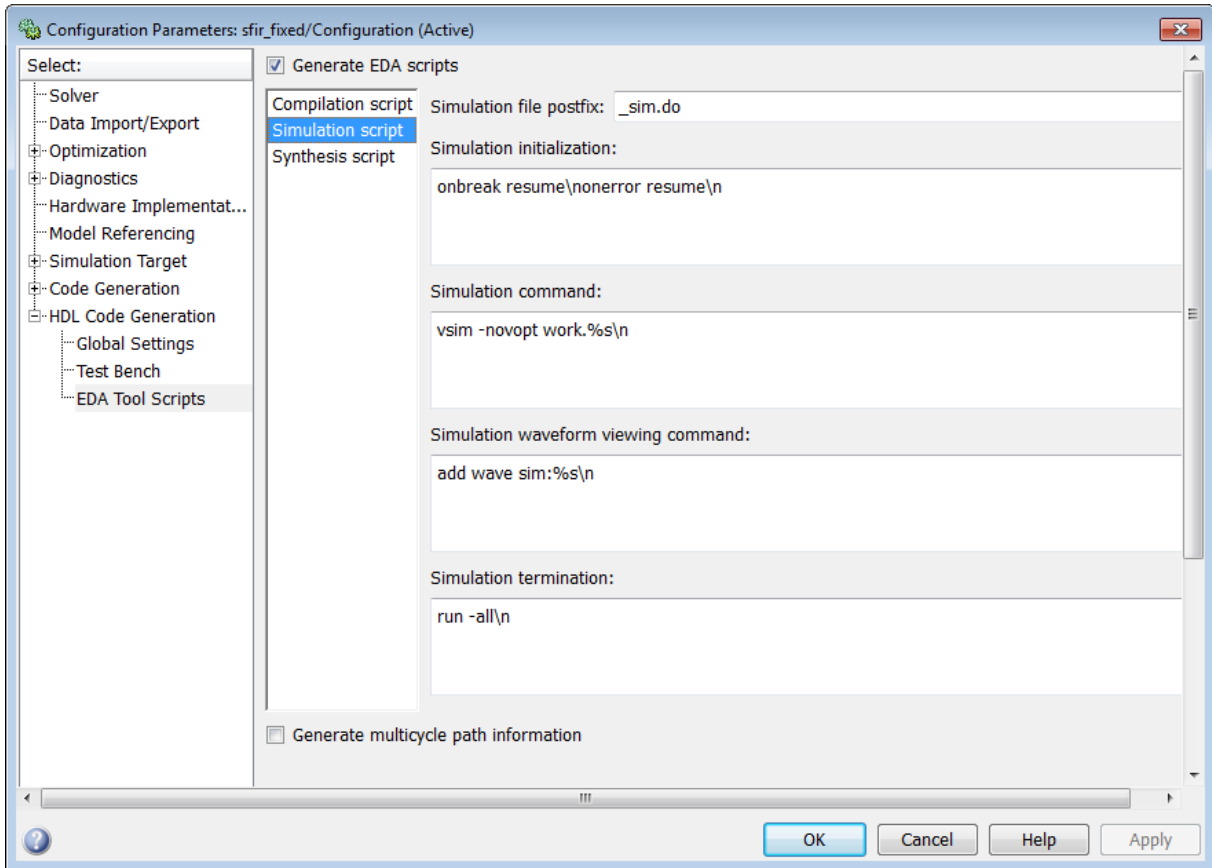


The following table summarizes the **Compilation script** options.

Option and Default	Description
<b>Compile file postfix'</b> '_compile.do'	Postfix string appended to the DUT name or test bench name to form the script file name.
Name: <b>Compile initialization</b> Default: 'vlib %s\n'	Format string passed to fprintf to write the Init section of the compilation script. The argument is the contents of the 'VHDLLibraryName' property, which defaults to 'work'. You can override the default <i>Init string ('vlib work\n')</i> by changing the value of
Name: <b>Compile command for VHDL</b> Default: 'vcom %s %s\n'	Format string passed to fprintf to write the Cmd section of the compilation script for VHDL files. The two arguments are the contents of the 'SimulatorFlags' property option and the filename of the current entity or module. To omit the flags, set 'SimulatorFlags' to '' (the default).
Name: <b>Compile command for Verilog</b> Default: 'vlog %s %s\n'	Format string passed to fprintf to write the Cmd section of the compilation script for Verilog files. The two arguments are the contents of the 'SimulatorFlags' property and the filename of the current entity or module. To omit the flags, set 'SimulatorFlags' to '' (the default).
Name: <b>Compile termination</b> Default: ''	Format string passed to fprintf to write the termination portion of the compilation script.

### Simulation Script Options

The following figure shows the **Simulation script** pane, with options set to their default values.



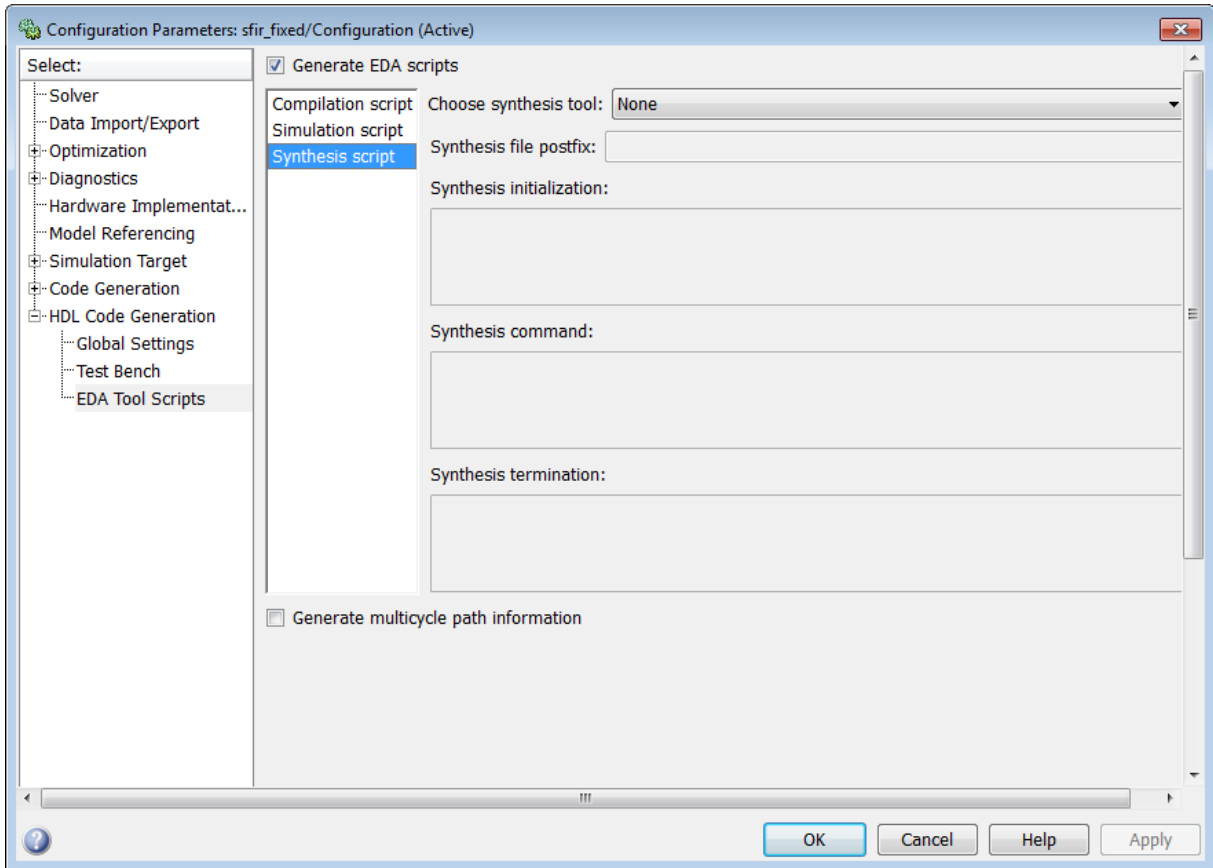
The following table summarizes the **Simulation script** options.

Option and Default	Description
<b>Simulation file postfix</b> Default: <code>'_sim.do'</code>	Postfix string appended to the model name or test bench name to form the simulation script file name.
<b>Simulation initialization</b> Default: <code>['onbreak resume\nonerror resume\n']</code>	Format string passed to <code>fprintf</code> to write the initialization section of the simulation script.

<b>Option and Default</b>	<b>Description</b>
<b>Simulation command</b> Default: 'vsim -novopt work.%s\n'	Format string passed to fprintf to write the simulation command. The implicit argument is the top-level module or entity name.
<b>Simulation waveform viewing command</b> Default: 'add wave sim:%s\n'	Format string passed to fprintf to write the simulation script waveform viewing command. The top-level module or entity signal names are implicit arguments.
<b>Simulation termination</b> Default: 'run -all\n'	Format string passed to fprintf to write the Term portion of the simulation script.

### Synthesis Script Options

The following figure shows the **Synthesis script** pane, with options set to their default values. The **Choose synthesis tool** property defaults to **None**, which disables generation of a synthesis script.

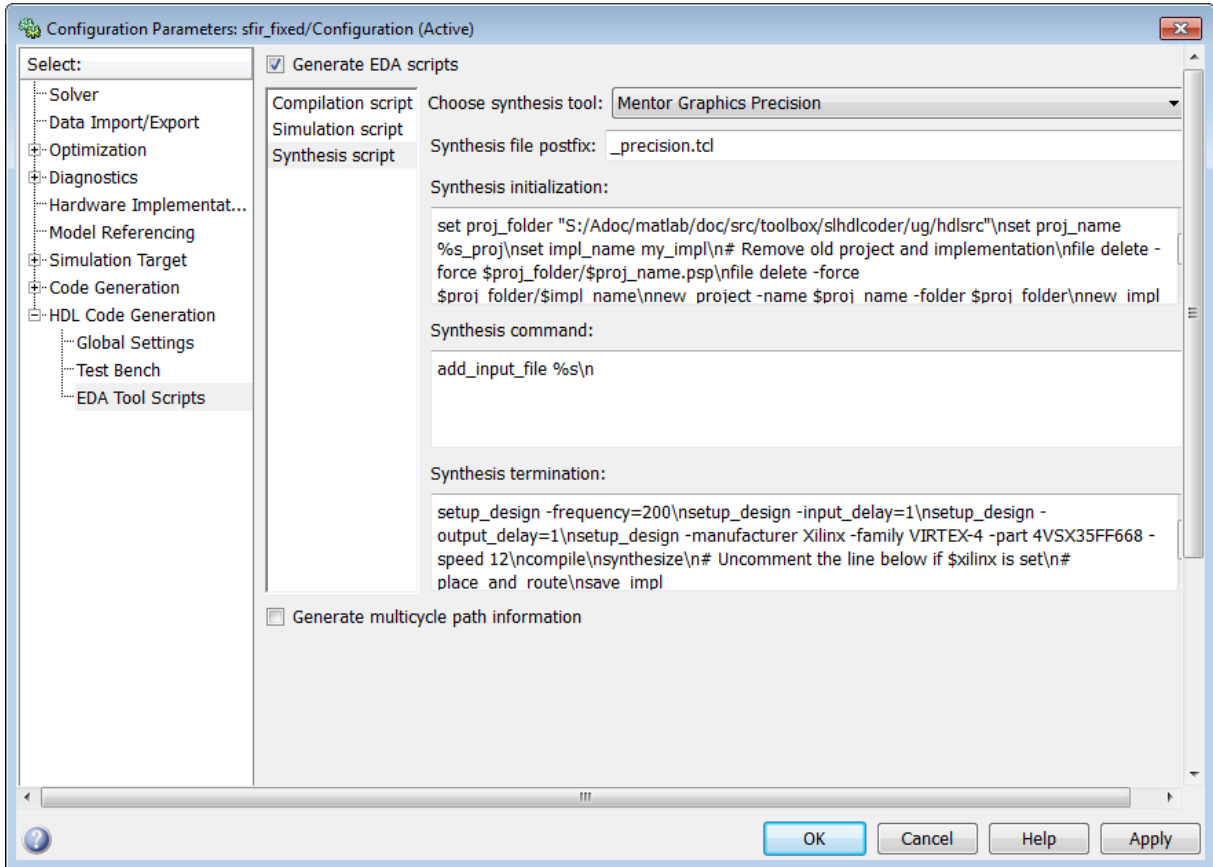


To enable synthesis script generation, select a synthesis tool from the **Choose synthesis tool** menu.

When you select a synthesis tool, the coder:

- Enables synthesis script generation.
- Enters a file name postfix (specific to the chosen synthesis tool) into the **Synthesis file postfix** field.
- Enters strings (specific to the chosen synthesis tool) into the initialization, command, and termination fields.

The following figure shows the default option values entered for the Mentor Graphics Precision tool.



The following table summarizes the **Synthesis script** options.

Option Name	Description
<b>Choose synthesis tool</b>	<p>None (default): do not generate a synthesis script</p> <p>ISE: generate a synthesis script for Xilinx ISE</p> <p>Precision: generate a synthesis script for Mentor Graphics Precision</p> <p>Quartus: generate a synthesis script for Altera Quartus II</p> <p>Synplify: generate a synthesis script for Synopsys Synplify Pro</p>
<b>Synthesis file postfix</b>	<p>Your choice of synthesis tool sets the postfix for generated synthesis file names to one of the following:</p> <p><code>_ise.tcl</code></p> <p><code>_precision.tcl</code></p> <p><code>_quartus.tcl</code></p> <p><code>_synplify.tcl</code></p>
<b>Synthesis initialization</b>	<p>Format string passed to <code>fprintf</code> to write the <code>Init</code> section of the synthesis script. The default string is a synthesis project creation command. The implicit argument is the top-level module or entity name. The content of the string is specific to the selected synthesis tool.</p>
<b>Synthesis command</b>	<p>Format string passed to <code>fprintf</code> to write the <code>Cmd</code> section of the synthesis script. The argument is the filename of the entity or module. The content of the string is specific to the selected synthesis tool.</p>
<b>Synthesis termination</b>	<p>Format string passed to <code>fprintf</code> to write the <code>Term</code> section of the synthesis script. The content of the string is specific to the selected synthesis tool.</p>





# Using the HDL Workflow Advisor

---

- “What Is the HDL Workflow Advisor?” on page 19-2
- “Open the HDL Workflow Advisor” on page 19-3
- “Using the HDL Workflow Advisor Window” on page 19-6
- “Selecting and Running HDL Workflow Advisor Tasks” on page 19-9
- “Save and Restore HDL Workflow Advisor State” on page 19-21
- “Fix a Workflow Advisor Warning or Failure” on page 19-25
- “View and Save HDL Workflow Advisor Reports” on page 19-28
- “Set Target Device and Synthesis Tool” on page 19-33
- “FPGA Target-Specific Floating-Point Library Mapping” on page 19-34
- “FPGA Synthesis and Analysis” on page 19-40
- “FPGA-in-the-Loop” on page 19-53
- “Automated Workflows for Specific Target Devices and Synthesis Tools” on page 19-60
- “xPC Target Interface Generation for Speedgoat Boards” on page 19-62
- “Target Xilinx FPGA Development Boards” on page 19-72

## What Is the HDL Workflow Advisor?

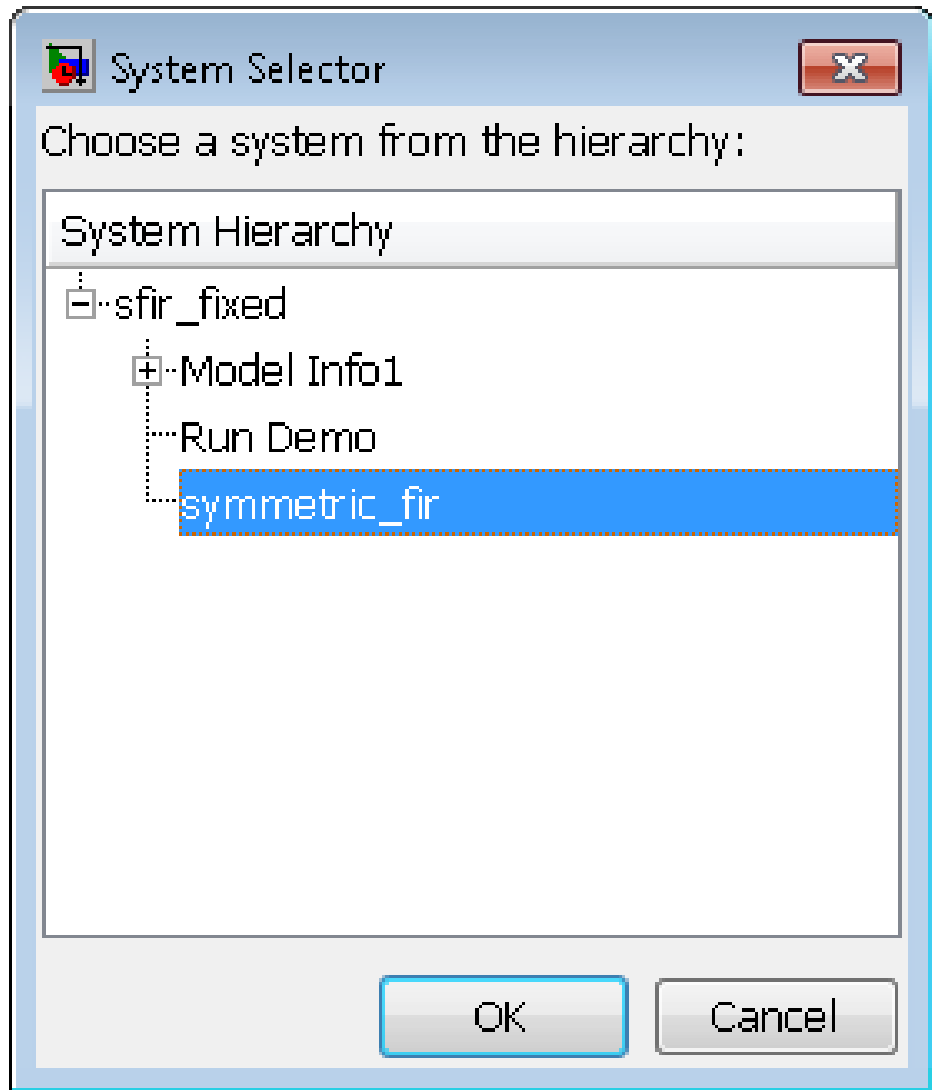
The HDL Workflow Advisor is a tool that supports and integrates the stages of the FPGA design process, such as:

- Checking the Simulink model for HDL code generation compatibility
- Automatically fixing model settings that are incompatible with HDL code generation
- Generation of RTL code, RTL test bench, a cosimulation model, or a combination of these
- Synthesis and timing analysis through integration with third-party synthesis tools
- Back annotation of the Simulink model with critical path and other information obtained during synthesis
- Complete automated workflows for selected FPGA development target devices and xPC Target™, including FPGA-in-the-Loop simulation

## Open the HDL Workflow Advisor

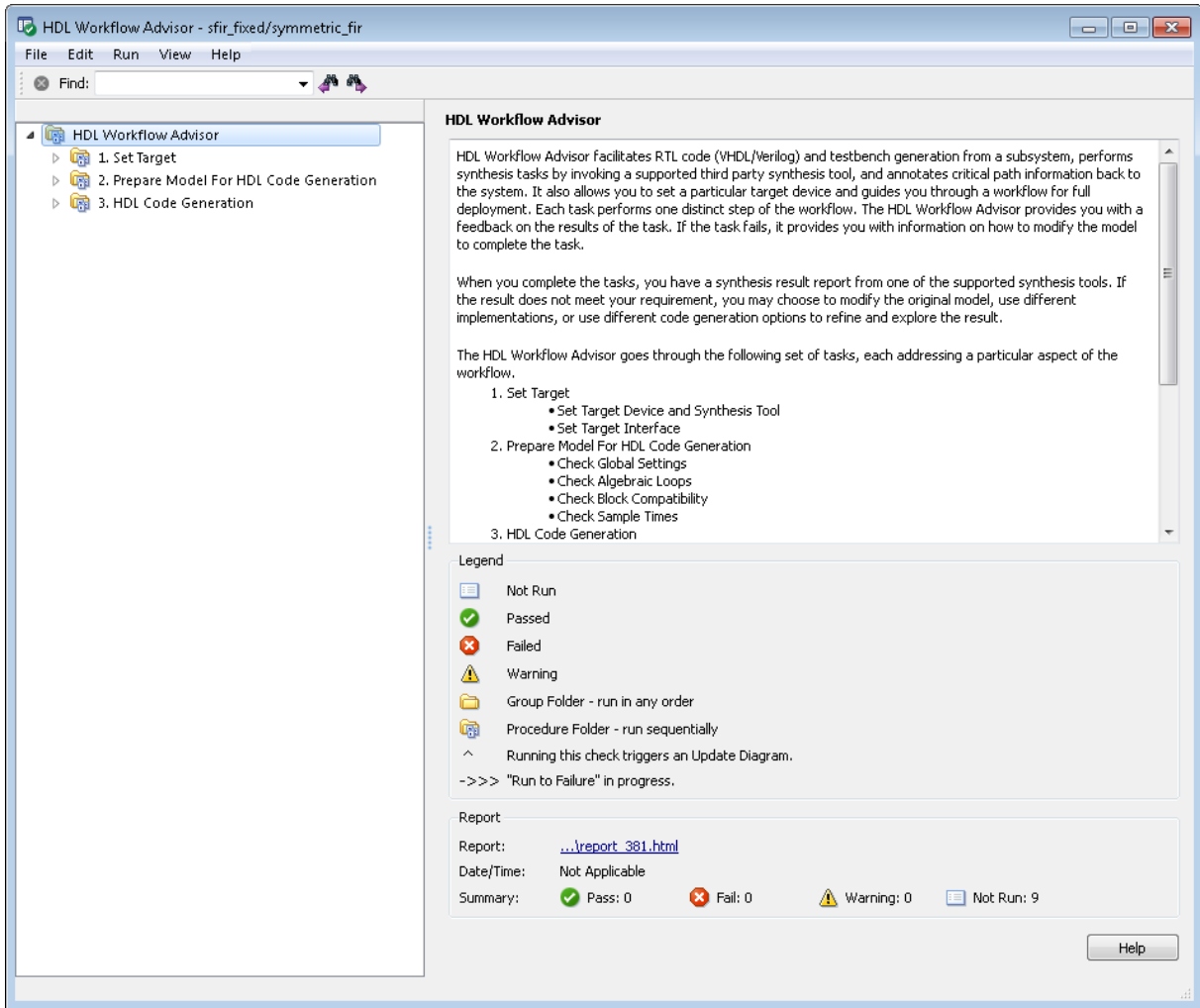
To start the HDL Workflow Advisor from a model:

- 1** Open your model.
- 2** Select **Code > HDL Code > HDL Workflow Advisor**.
- 3** In the System Selector window, select the DUT that you want to review. In the following figure, the `symmetric_fir` subsystem is the selected DUT.



4 Click **OK**.

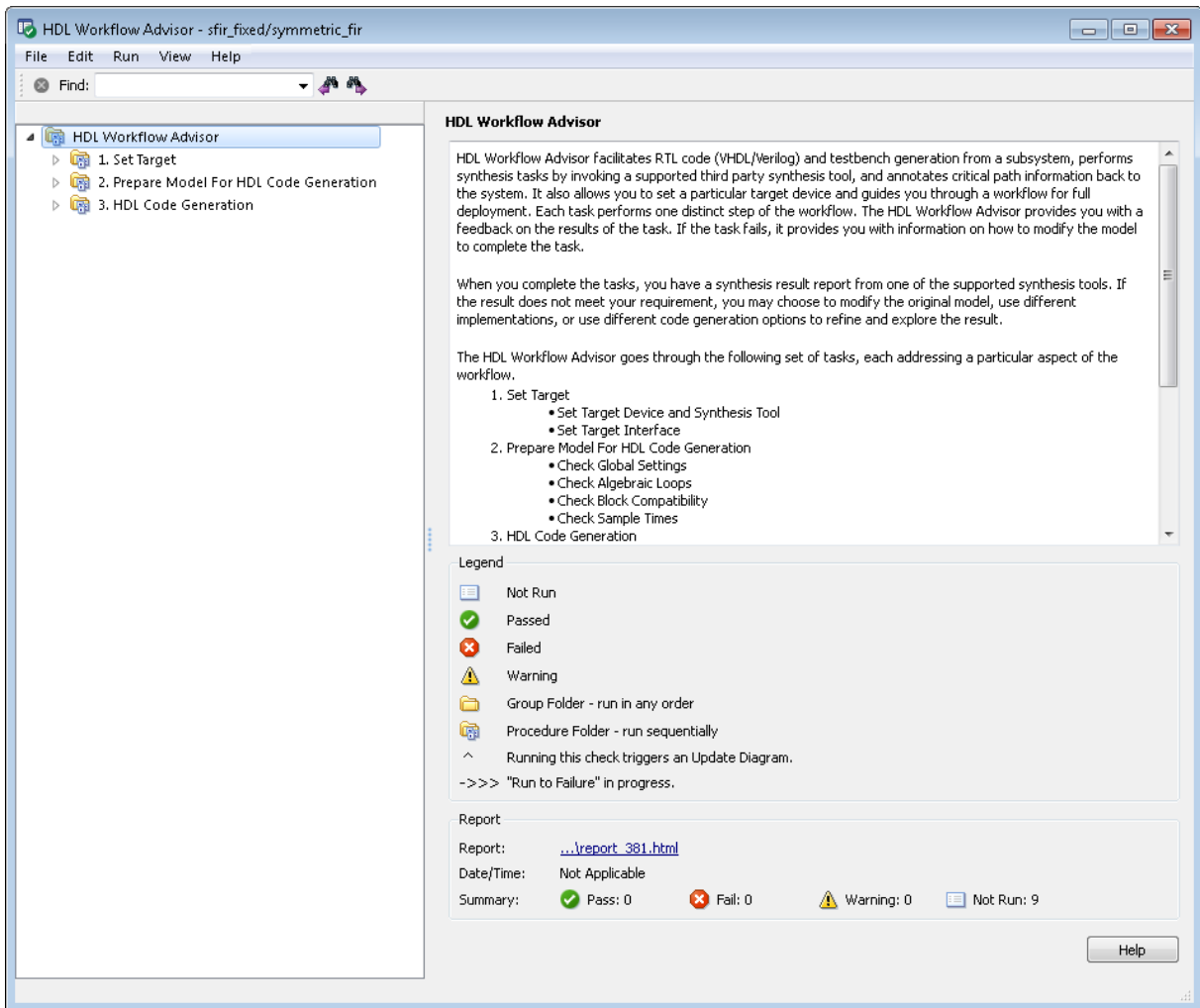
The HDL Workflow Advisor initializes and appears.



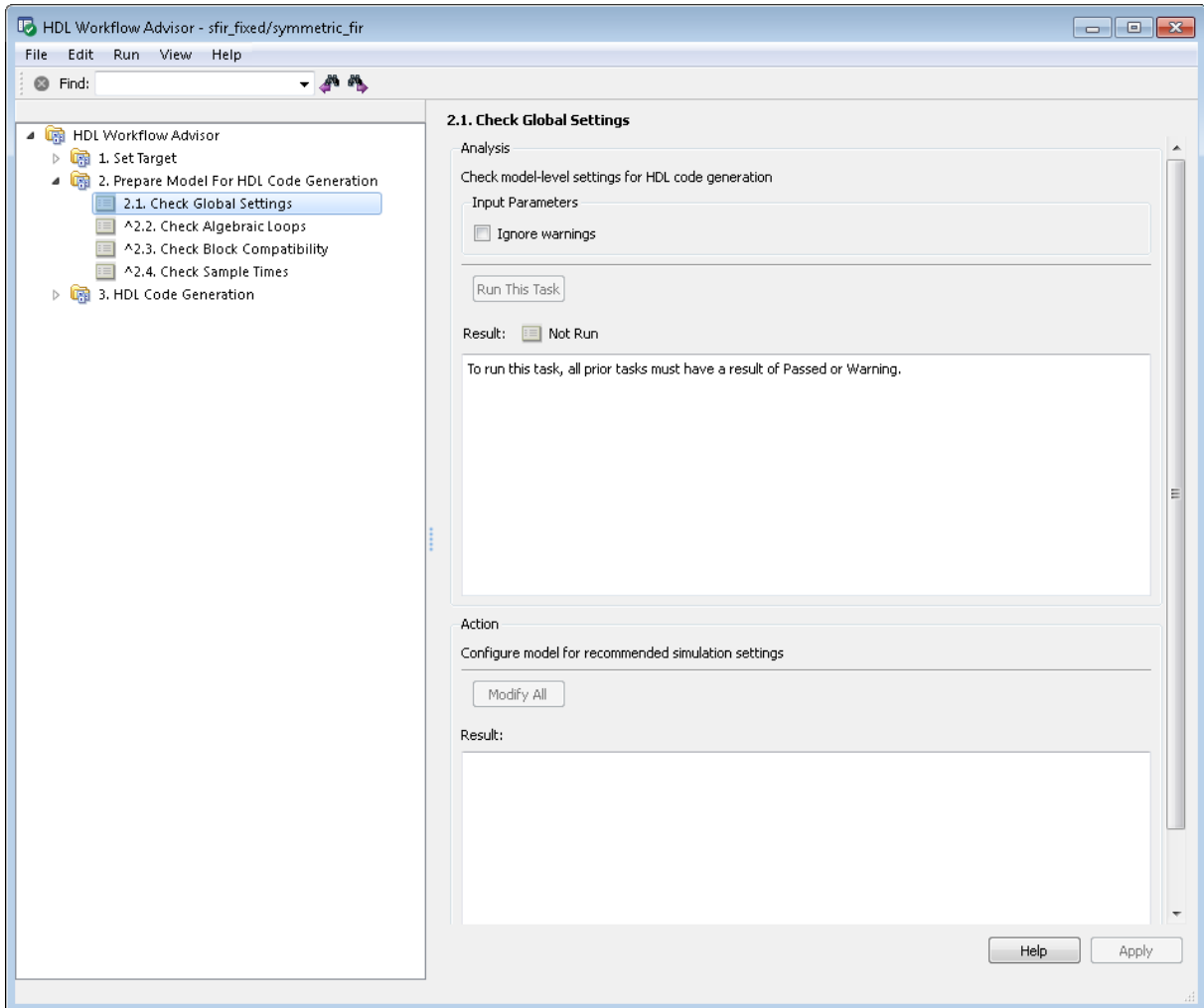
To start the HDL Workflow Advisor from the command line, enter `hdladvisor(system)`, where `system` is a handle or name of the model or subsystem that you want to check. For more information, see the `hdladvisor` function reference page.

## Using the HDL Workflow Advisor Window

The following figure shows the top-level view of the HDL Workflow Advisor. The left pane lists the folders in the HDL Workflow Advisor hierarchy. Each folder represents a group or category of related tasks.



Expanding the folders shows available tasks in each folder. The following figure shows the expanded **Prepare Model For HDL Code Generation** folder, with the **Check Global Settings** task selected.



From the left pane, you can select a folder or an individual task. The HDL Workflow Advisor displays information about the selected folder or task in the right pane.

The content of the right pane depends on the selected folder or task. For some tasks, the right pane contains simple controls for running the task and a display area for status messages and other task results. For other tasks (for example, setting code or test bench generation parameters), the right pane displays many parameter and option settings.

When you right-click a folder or an individual task in the left pane, a context menu appears. The context menu lets you:

- Select a task or a group of tasks to run sequentially (see “Task Execution Order” on page 19-9).
- Reset the status of one or more tasks to **Not Run**. Resetting status enables you to rerun tasks.
- View context-sensitive help (CSH) for an individual task.



## Selecting and Running HDL Workflow Advisor Tasks

In this section...
“Task Execution Order” on page 19-9
“Changing the Device Under Test” on page 19-11
“Selecting and Running Tasks Individually” on page 19-13
“Selecting and Running a Sequence of Tasks” on page 19-15

### Task Execution Order

The HDL Workflow Advisor displays folders, subfolders, and tasks in a numbered hierarchy. The numbering represents a *sequential* workflow. That is, the HDL Workflow Advisor does not enable a given task for execution until the previous tasks have executed.

For example, the tasks in the **Prepare Model For HDL Code Generation** folder are numbered as follows:

**2.1 Check Global Settings**

**2.2 Check Algebraic Loops**

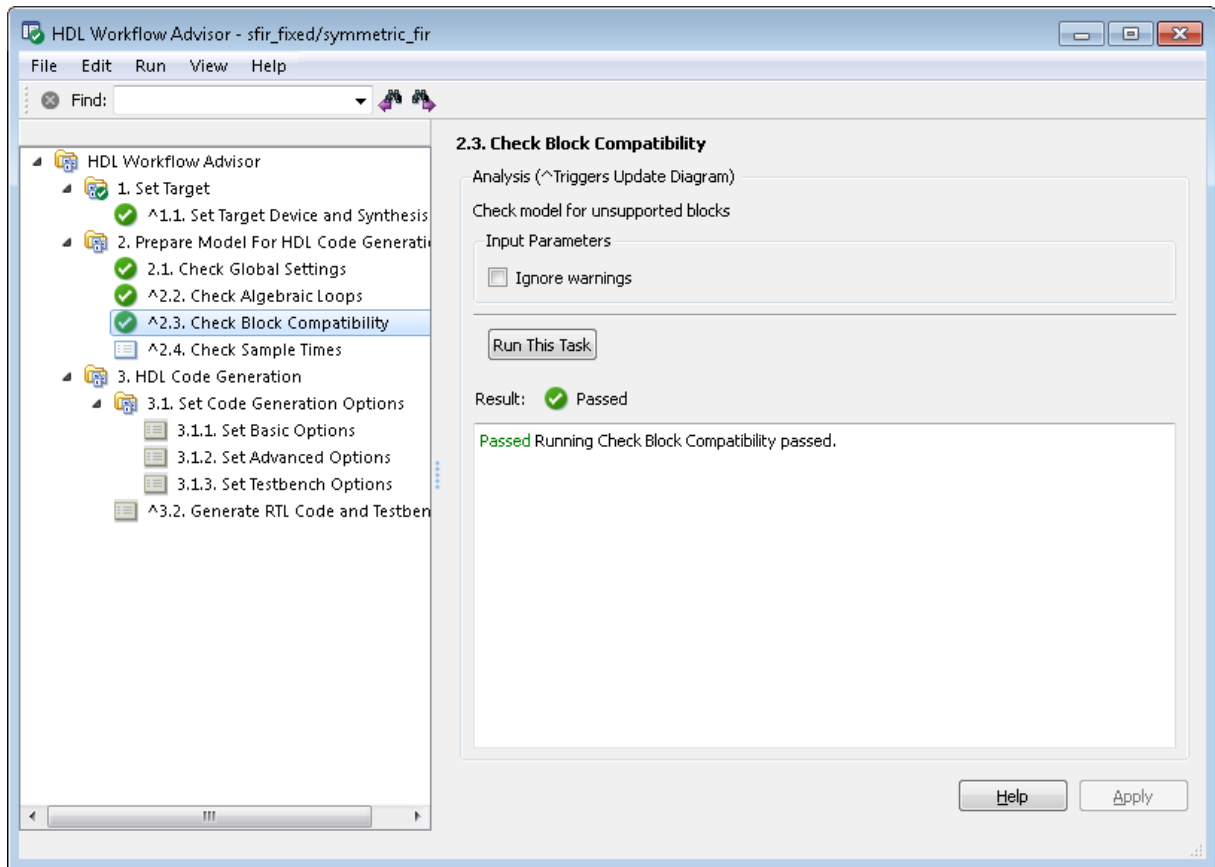
**2.3 Check Block Compatibility**

**2.4 Check Sample Times**

These tasks must execute in the order 2.1 ... 2.4.

### What the Task Icons Represent

Icons represent the execution state of each task in the list. For an example, see the following figure.



In this figure:

- The green check mark icons to the left of tasks 1.1 and 2.1 – 2.3 indicate that these tasks have executed.
- The light blue icon to the left of task 2.4 indicates that this task is enabled for execution. You can execute this individual task by:
  - Selecting **Run This Task** from the right-click context menu or
  - Clicking the **Run This Task** button in the right pane of the HDL Workflow Advisor.

- The gray icons to the left of the tasks below 3.1 indicate that these tasks are not currently enabled for execution as individual tasks. You can execute a group of such tasks by selecting one of them and then selecting **Run To Selected Task** from the right-click context menu.

## Resetting and Rerunning Tasks

Tasks that the Workflow Advisor has not yet run default to a Not Run state. If you need to rerun a task at some point in the workflow for some reason, you must first reset the task to a Not Run state. For example, you might change some code generation parameters for one of the **Set Code Generation Options** tasks. In such a case, you should rerun that task and validate your parameter settings. Before you can do this, you must reset the task to a Not Run state.

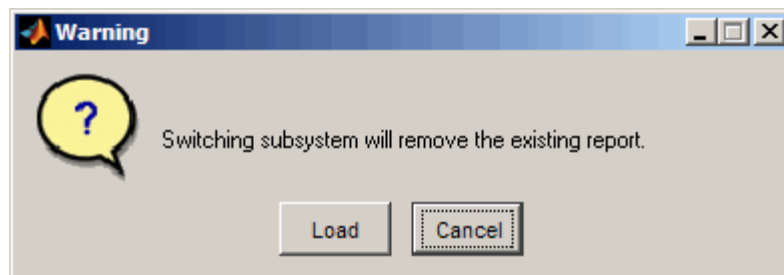
To reset a task:

- 1 Right-click the task icon and select **Reset This Task**.
- 2 After reset, verify that the task is in a Not Run state and enabled.

## Changing the Device Under Test

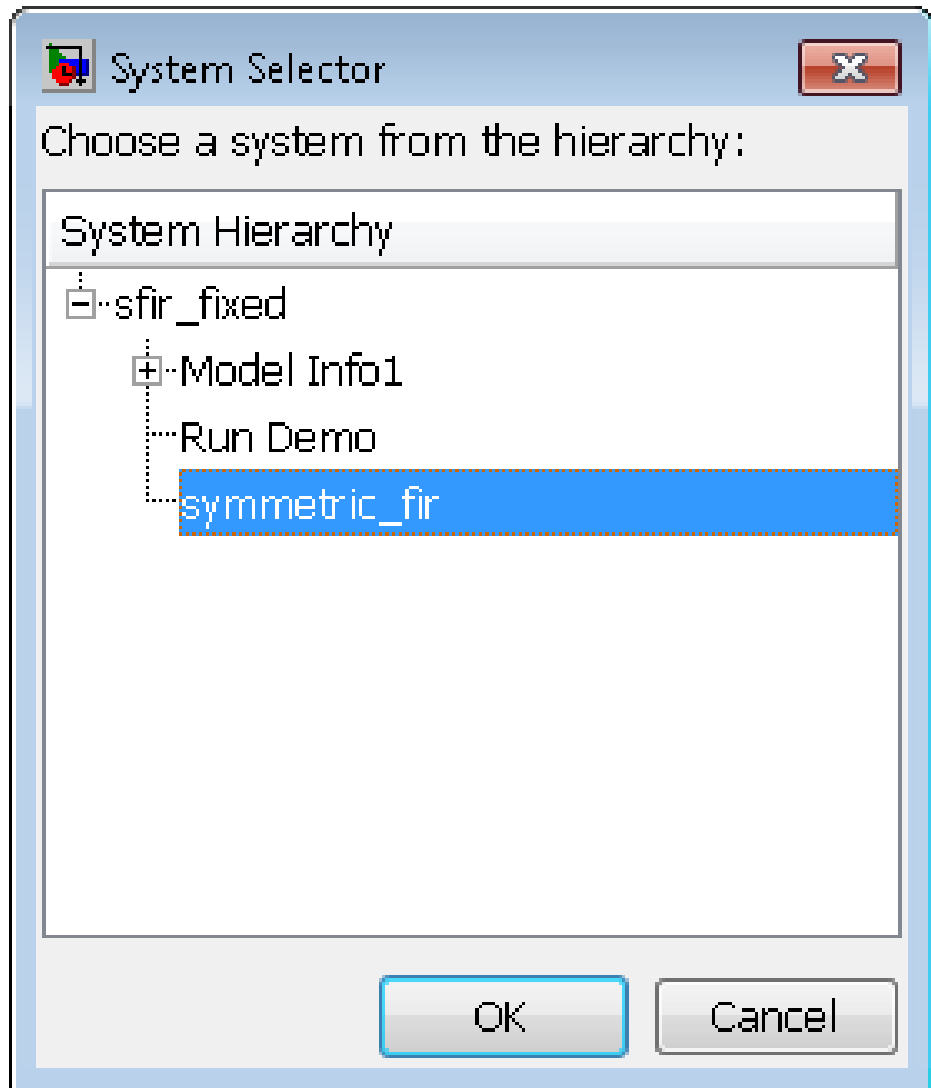
If you want to run HDL Workflow Advisor checks or tasks on a different subsystem within the same model, follow these steps:

- 1 In the HDL Workflow Advisor, select **File > Switch subsystem**. The HDL Workflow Advisor displays the following message.



- 2 Click **Load**. The System Selector window opens.

- 3 In the System Selector window, select the DUT that you want to review.



- 4 Click **OK**. The HDL Workflow Advisor is now ready to run with the selected DUT.

## Selecting and Running Tasks Individually

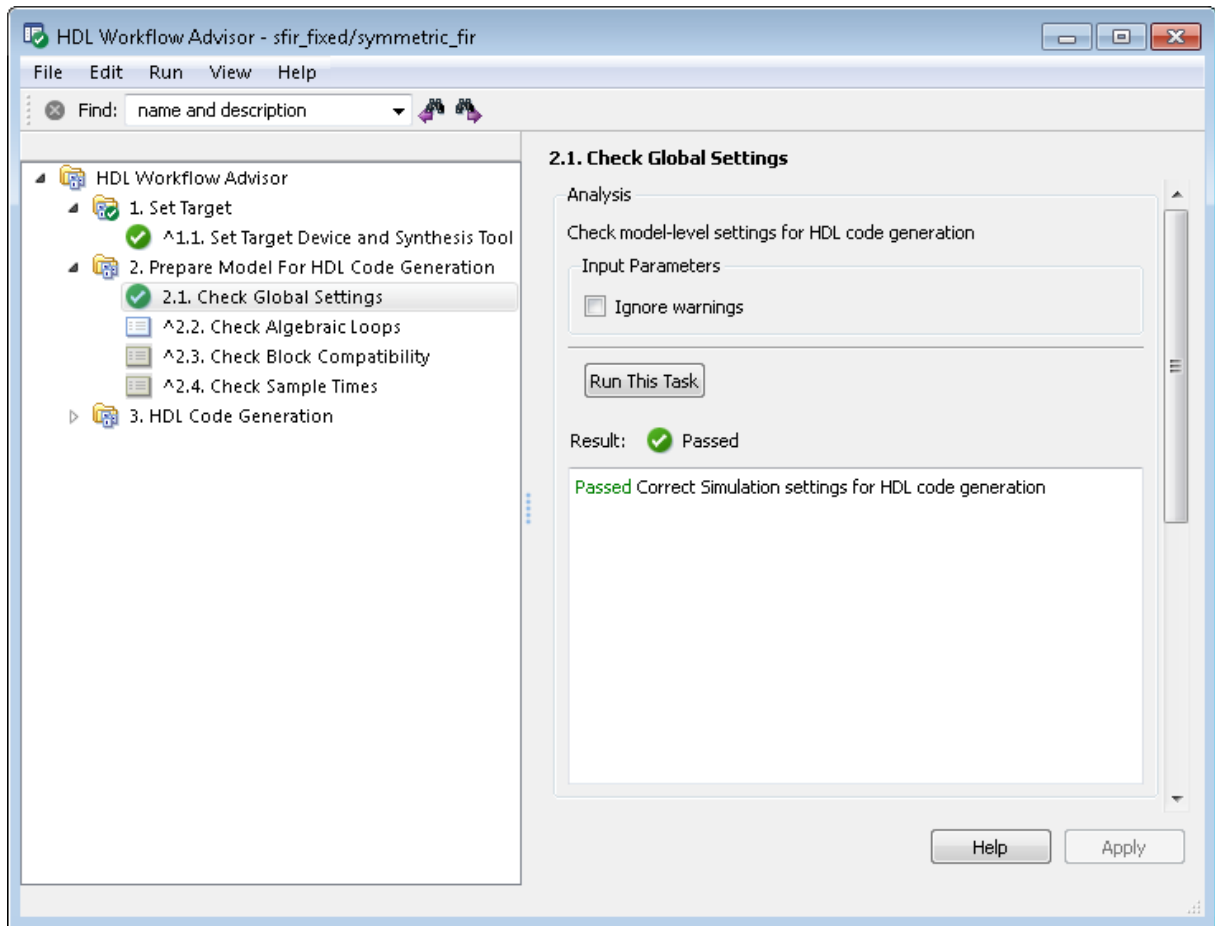
The HDL Workflow Advisor does not enable a given task for execution until the previous tasks have executed. At a given time, only one task in the HDL Workflow Advisor hierarchy is enabled.

To perform a single task on the DUT and view the task results:

- 1** Locate and open the task folder that contains the desired task.
- 2** Inspect the desired task icon and verify that it is enabled.
  - If the task you want to run is disabled, you must first run the tasks that precede it. See “Selecting and Running a Sequence of Tasks” on page 19-15.
  - If the task you want to run is enabled, continue to the next step.
- 3** Right-click the task icon and select **Run This Task**.

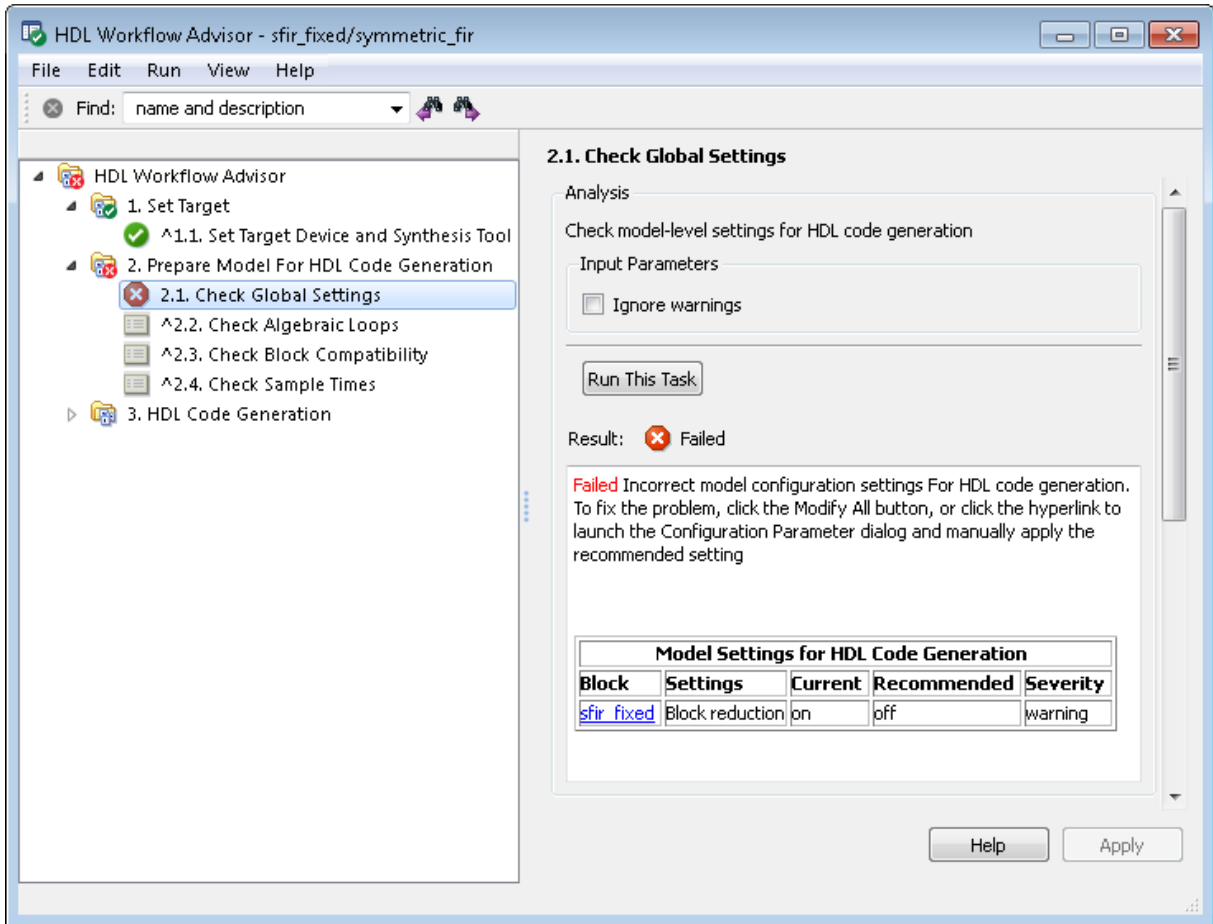
The HDL Workflow Advisor runs the task. While the task runs, a progress indicator appears.

- 4** If the check completes, the HDL Workflow Advisor displays a green check mark icon to the left of the completed task. The HDL Workflow Advisor also enables the next task in the hierarchy. The following figure shows the HDL Workflow Advisor after completion of the **Check Global Settings** task.



If the task fails, the HDL Workflow Advisor displays a red check mark icon to the left of the completed task. The next task in the workflow is not enabled, and you must fix reported errors before you can proceed to the next step. (See “Fix a Workflow Advisor Warning or Failure” on page 19-25.)

The following figure shows the HDL Workflow Advisor after failure of the **Check Global Settings** task.



## Selecting and Running a Sequence of Tasks

The HDL Workflow Advisor supports two options that let you run a group of two or more tasks. The options are:

- **Run to Selected Task:** Starting with the first enabled task in the HDL Workflow Advisor hierarchy, run the tasks up to and including the selected task.

- **Run to Failure:** Starting with the first enabled task in the currently selected folder, run the tasks in the folder. Task execution continues until one of the following occurs:
  - A task fails.
  - All tasks within the folder run to completion.

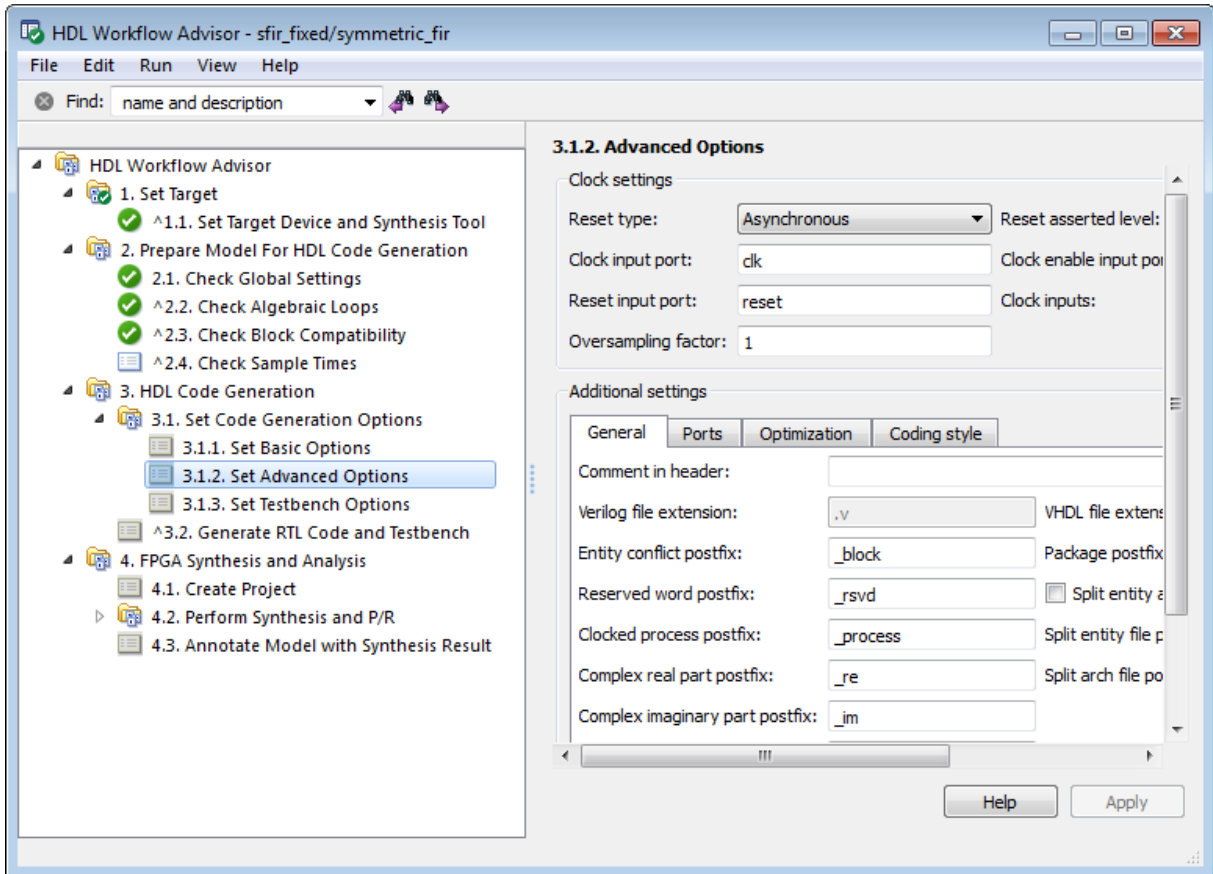
The **Run to Failure** option is available only at the folder level.

The following sections, “Run to Selected Task” on page 19-16 and “Run to Failure” on page 19-18, illustrate each option.

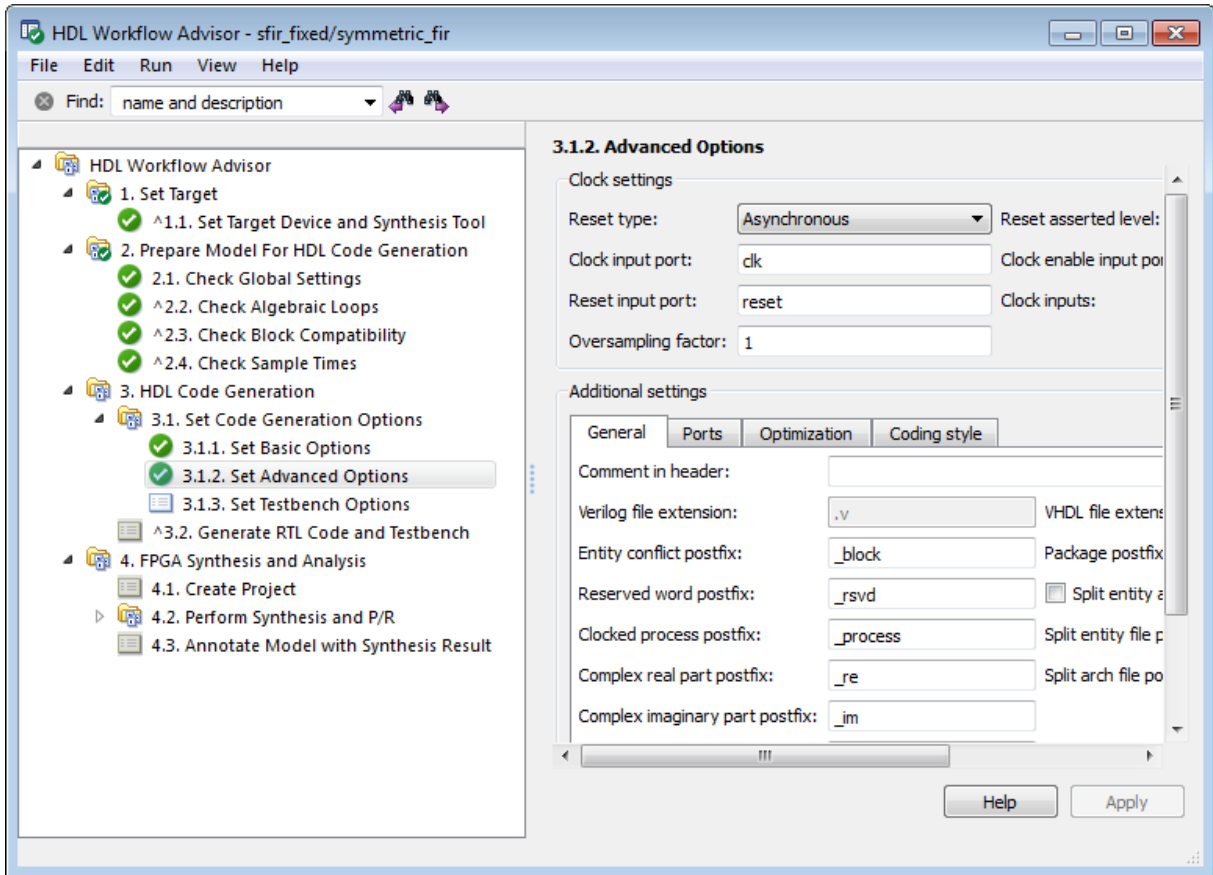
### **Run to Selected Task**

In the following figure, **Check Sample Times** is the first enabled task and **Set Advanced Options** is selected.



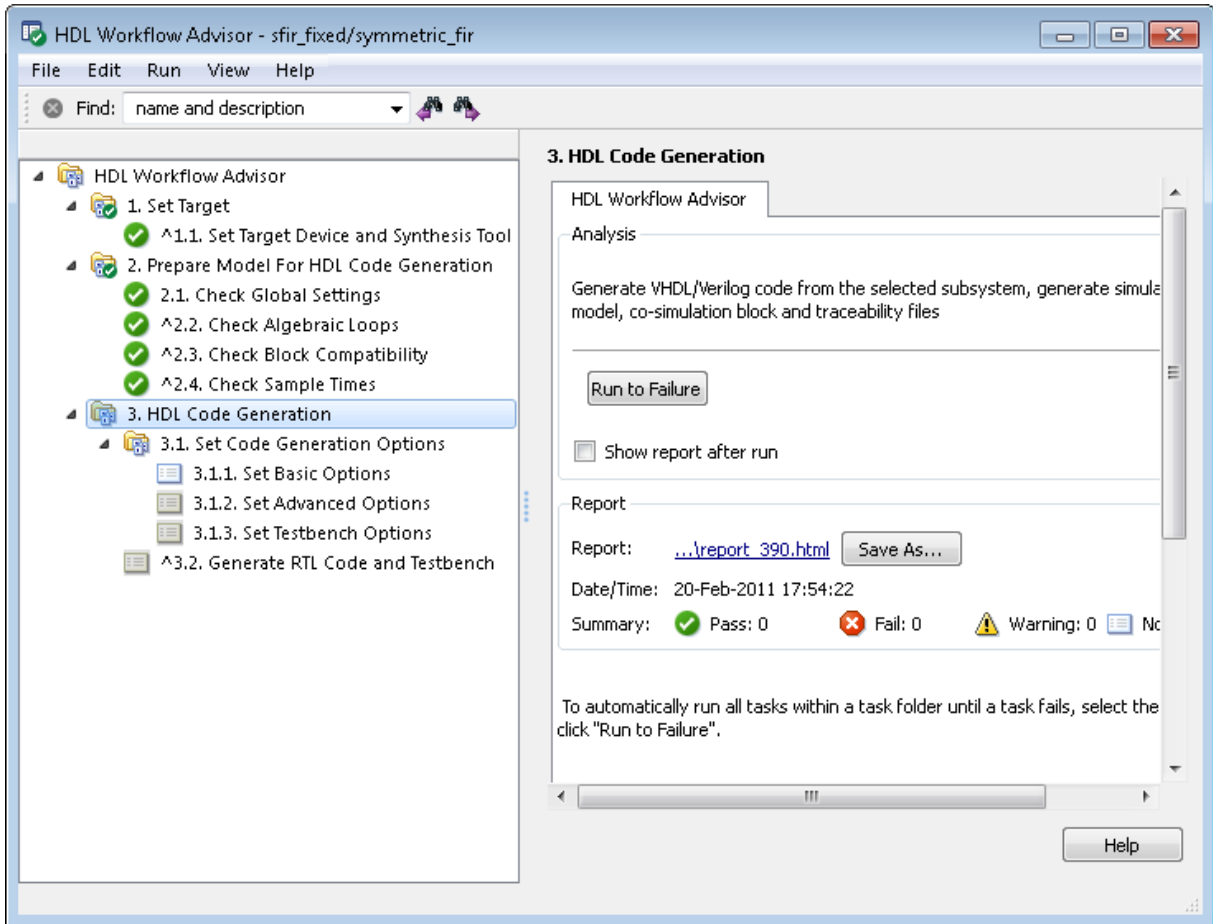


When you right-click and select **Run to Selected Task**, the HDL Workflow Advisor performs tasks starting with **Check Sample Times**, then up to and including **Set Advanced Options**. After this task sequence completes, the **Set Testbench Options** task is enabled:



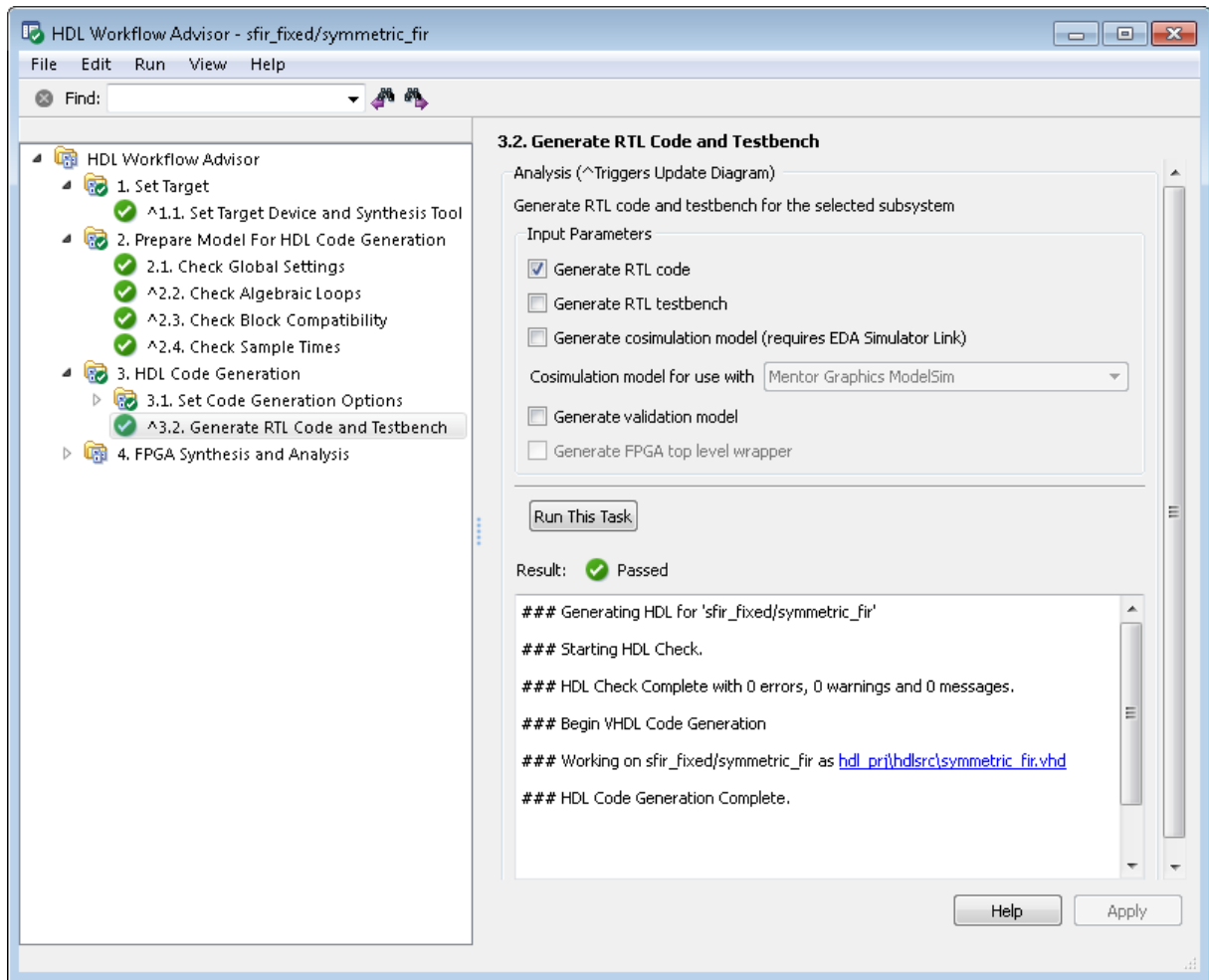
### Run to Failure

In the following figure, **Set Basic Options** is the first enabled task, and the **HDL Code Generation** folder is selected.



When you right-click and select **Run to Failure**, the HDL Workflow Advisor performs tasks within the **HDL Code Generation** folder. This includes the tasks within the **Set Code Generation Options** subfolder.

After this task sequence completes, the HDL Workflow Advisor shows the results of the most recent task executed in the right pane:



# Save and Restore HDL Workflow Advisor State

**In this section...**

“How the Save and Restore Process Works” on page 19-21

“Limitations of the Save and Restore Process” on page 19-21

“Save the HDL Workflow Advisor State” on page 19-21

“Restore the HDL Workflow Advisor State” on page 19-23

## How the Save and Restore Process Works

By default, the coder saves the state of the most recent HDL Workflow Advisor session. The next time you activate the HDL Workflow Advisor, it returns to that state.

You can also save the current settings of the HDL Workflow Advisor to a named *restore point*. At a later time, you can restore the same settings by loading the restore point data into the HDL Workflow Advisor.

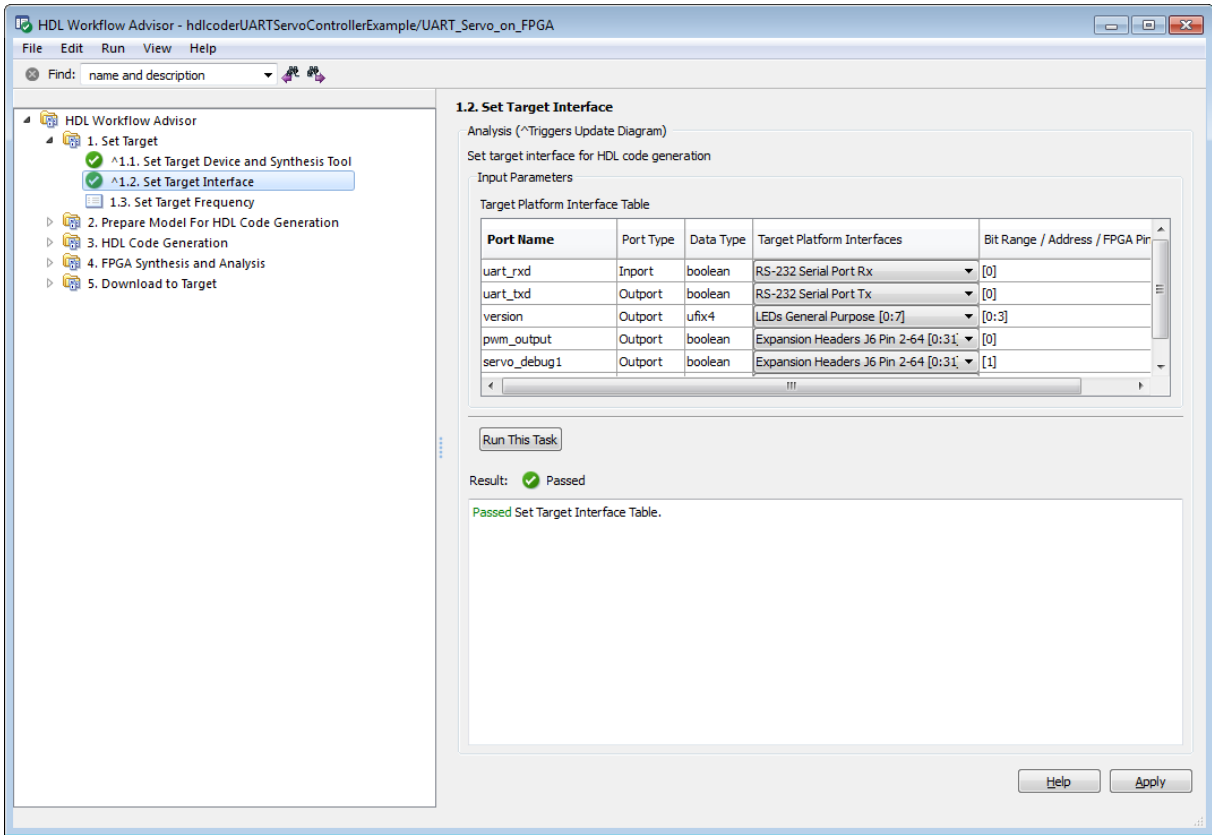
## Limitations of the Save and Restore Process

The save and restore process has the following limitations:

- Operations that you perform outside the HDL Workflow Advisor is not included in the save/restore process.
- The state of HDL Workflow Advisor tasks involving third-party tools are not saved or restored.

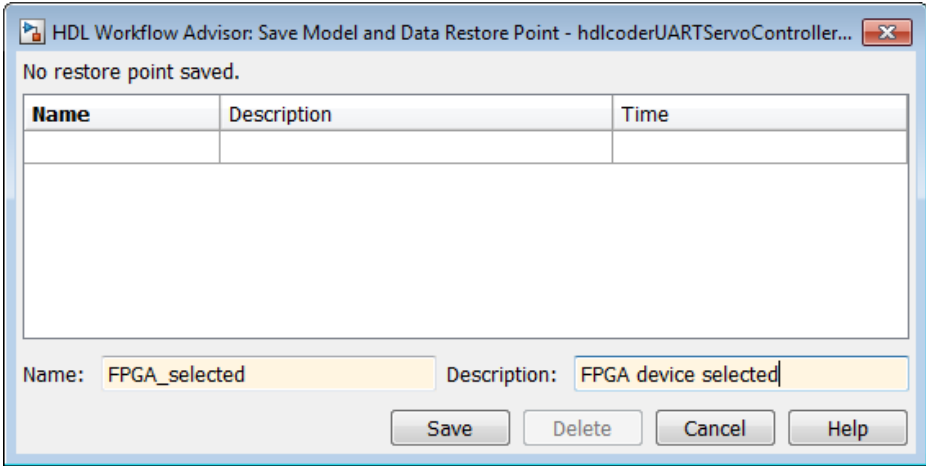
## Save the HDL Workflow Advisor State

You can create and save a restore point after completion of a task sequence. For example, the following figure shows the HDL Workflow Advisor after completion of the **Set Target Interface** task.



To save the HDL Workflow Advisor settings:

- 1** In the HDL Workflow Advisor, select **File > Save Restore Point As**.
- 2** In the **Name** field, enter a name for the restore point.
- 3** In the **Description** field, you can add an optional description of the restore point.

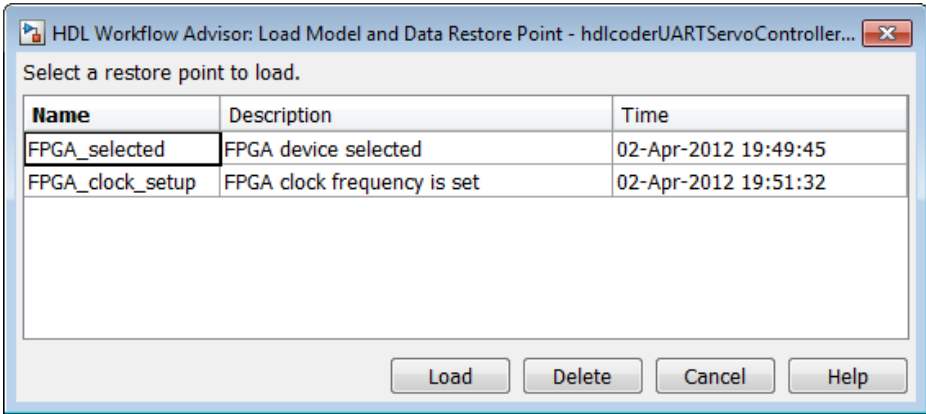


4 Click **Save**. The HDL Workflow Advisor saves a restore point of the current settings.

## Restore the HDL Workflow Advisor State

To load a restore point:

1 In the HDL Workflow Advisor, select **File > Load Restore Point**.



2 Select the restore point that you want.

**3 Click Load.**

The HDL Workflow Advisor issues a warning that the restoration will overwrite current settings.

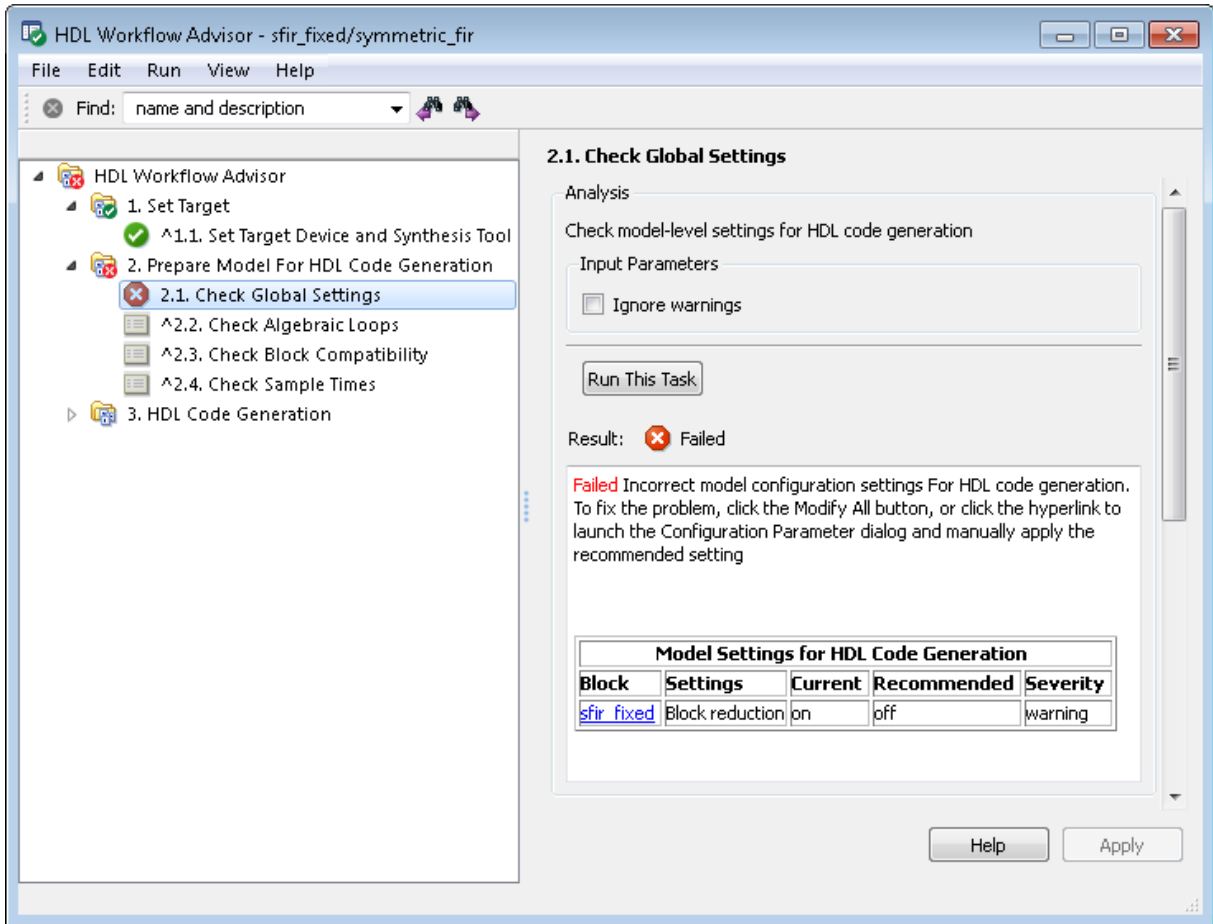
**4 Click Load** to load the restore point you selected. The HDL Workflow Advisor restores the previously saved state.



## Fix a Workflow Advisor Warning or Failure

If a task terminates due to a warning or failure condition, the right pane of the HDL Workflow Advisor shows information about the problems. This information appears in an **Analysis Result** subpane. The **Analysis Result** subpane also suggests model settings you can use to fix the problems.

Some tasks have an **Action** subpane that lets you apply the recommended actions listed in the **Analysis Result** subpane automatically. In the following example, the **Check Global Settings** task has failed, displaying an incorrect model setting in the **Analysis Result** pane.



The Action subpane, below the Analysis Result subpane, contains a **Modify All** button. To fix the problems that appear in the Analysis Result subpane, click the **Modify All** button.

After you click **Modify All**, the Analysis Result subpane reports the changes that were applied. The task is set to a Not Run and enabled state, enabling you to rerun the task and proceed to the subsequent tasks.

---

**Tip** Review the **Analysis Result** box before automatically fixing failures. If you do not want to apply all of the recommended actions, do not click **Modify All** to fix warnings or failures.

---

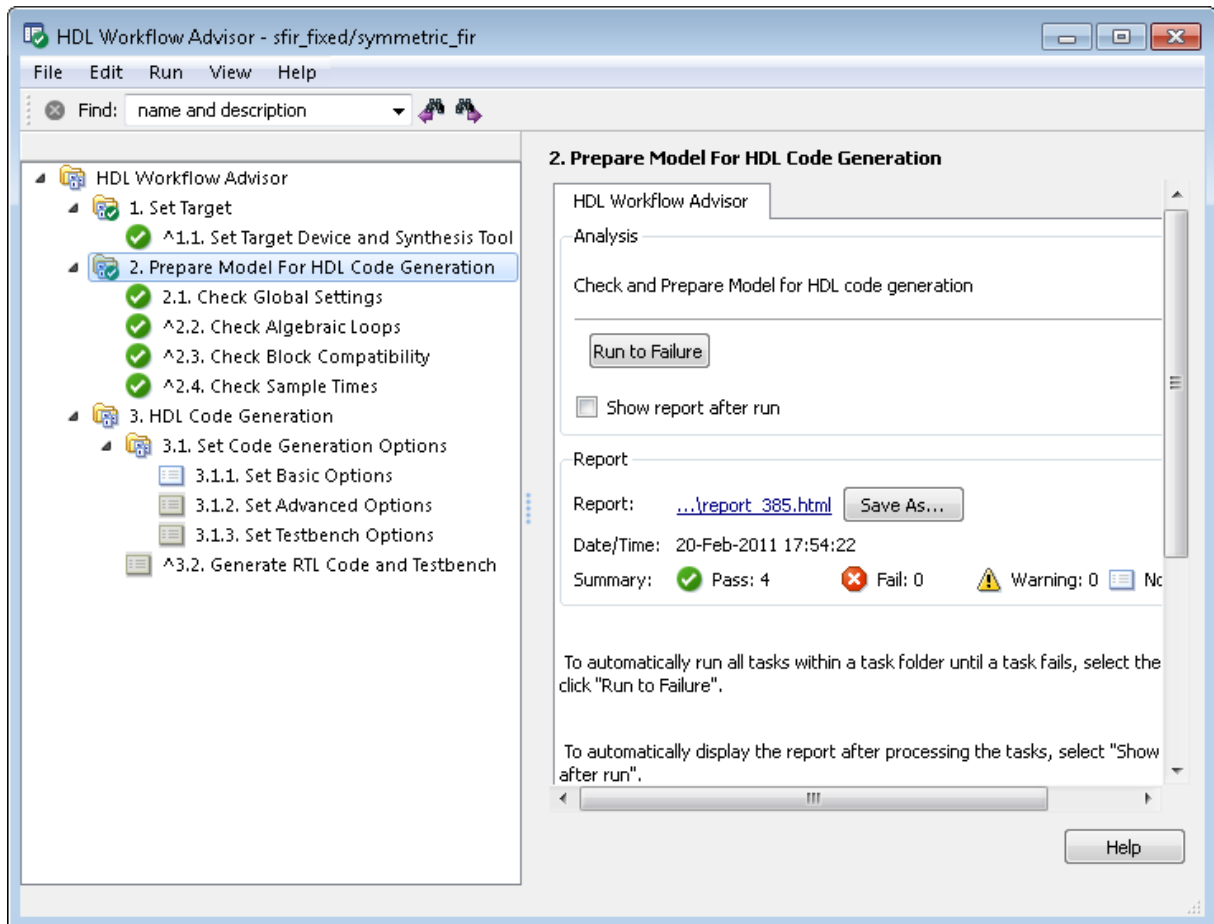
## View and Save HDL Workflow Advisor Reports

In this section...
“Viewing HDL Workflow Advisor Reports” on page 19-28
“Saving HDL Workflow Advisor Reports” on page 19-32

### Viewing HDL Workflow Advisor Reports

When the HDL Workflow Advisor runs tasks, it automatically generates an HTML report of task results. Each folder in the HDL Workflow Advisor contains a report for the checks within that folder and its subfolders.

You can access reports by selecting a folder and clicking the link in the **Report** subpane. In the following example, the **Prepare Model For HDL Code Generation** folder is selected.



The following report shows typical results for a run of the **Prepare Model For HDL Code Generation** tasks.

**Report name: Model Advisor - 2. Prepare Model For HDL Code Generation**





Simulink version: **7.7**

Model version: **1.67**

System: **sfir\_fixed/symmetric\_fir**


Current run: **20-Feb-2011 20:51:24**

**Run Summary**

<input checked="" type="checkbox"/> Pass	<input checked="" type="checkbox"/> Fail	<input checked="" type="checkbox"/> Warning	<input checked="" type="checkbox"/> Not Run	Total
 4	 0	 0	 0	4

**2. Prepare Model For HDL Code Generation**

---

 **2.1. Check Global Settings**

**Passed** Correct Simulation settings for HDL code generation

---

 **2.2. Check Algebraic Loops**


**Passed** No algebraic loop detected

---

 **2.3. Check Block Compatibility**

**Passed** Running Check Block Compatibility passed.

---

 **2.4. Check Sample Times**

**Passed** Running Check Sample Times passed.

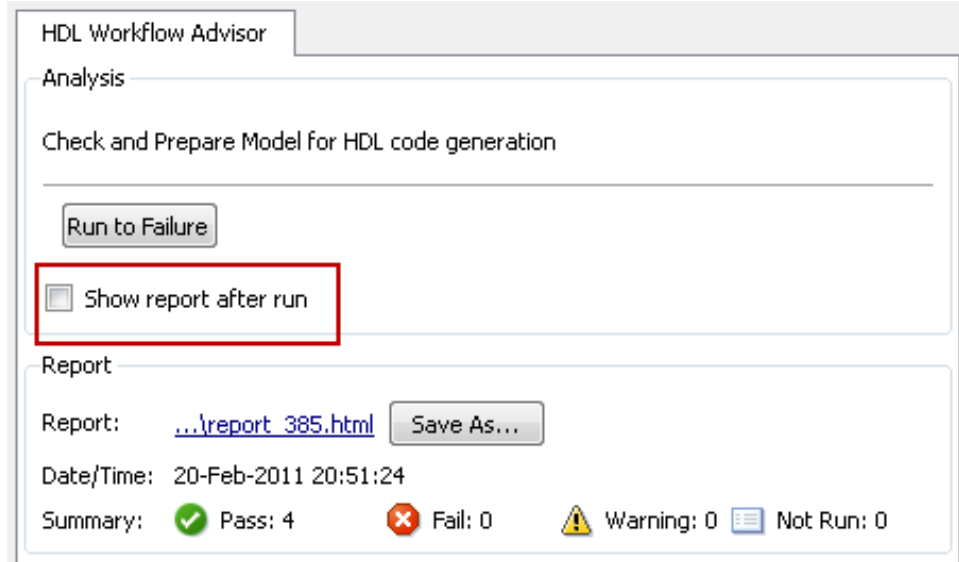
As you run checks, the HDL Workflow Advisor updates the reports with the latest information for each check in the folder. A message appears in the

report when you run the checks at different times. Time stamps indicate when checks have been run. The time of the current run appears at the top right of the report. Checks that occurred during previous runs have a time stamp following the check name.

You can manipulate the report to show only what you are interested in viewing as follows:

- The check boxes under **Run Summary** allow you to view only the checks with the status that you are interested in viewing. For example, you can remove the checks that have not run by clearing the check box next to the **Not Run** status.
- Minimize folder results in the report by clicking the minus sign next to the folder name. When you minimize a folder, the report updates to display a run summary for that folder.

You can view the report for a folder automatically each time the folder's tasks run. To do this, select **Show report after run**:



## **Saving HDL Workflow Advisor Reports**

You can archive an HDL Workflow Advisor report by saving it to a new location. To save a report:

- 1** In the HDL Workflow Advisor, navigate to the folder that contains the report you want to save.
- 2** Select the folder that you want. The right pane of the HDL Workflow Advisor shows information about that folder, including a **Report** subpane.
- 3** In the **Report** subpane, click **Save As**.
- 4** In the Save As dialog box, navigate to the location where you want to save the report, and click **Save**. The HDL Workflow Advisor saves the report to the new location.

---

**Note** If you rerun the HDL Workflow Advisor, the report is updated in the working folder, not in the save location. You can find the full path to the report in the title bar of the report window. Typically, the report is within the working folder: `s1prj\modeladvisor\HDLAdv_model_name\DUT_name\`.

---



## Set Target Device and Synthesis Tool

The HDL Workflow Advisor tasks in the **Set Target** folder enable you to select the target FPGA device, specify an FPGA synthesis tool, and specify other synthesis parameters.

The **Set Target Device and Synthesis Tool** task parameters are:

- **Target platform:** List of supported target devices.
- **Synthesis tool:** If you select a target other than **Generic ASIC/FPGA Target**, this parameter shows a synthesis tool that corresponds to the target device.

Verify that the desired synthesis tool is installed on your machine. For more information, see “Setting Up the Synthesis Tool Path”.

- **Family:** Target device family. The default is `Virtex4`.
- **Device:** Specific target device, within selected family.
- **Package:** Available package choices. The family and device determine these choices.
- **Speed:** Available speed choices. The family, device, and package determine these choices.

## FPGA Target-Specific Floating-Point Library Mapping

### In this section...

“What is an FPGA Target-Specific Floating-Point Library?” on page 19-34

“Why Map to an FPGA Target-Specific Floating Point Library?” on page 19-34

“Prerequisites for FPGA Target-Specific Floating-Point Library Mapping” on page 19-35

“Supported Xilinx Floating-Point Library Blocks” on page 19-35

“Supported Altera Floating-Point Library Blocks” on page 19-36

“How to Map to an FPGA Target-Specific Floating-Point Library” on page 19-36

“FPGA Target-Specific Library Mapping Results Analysis” on page 19-38

“Limitations for FPGA Target-Specific Floating-Point Library Mapping” on page 19-38

### What is an FPGA Target-Specific Floating-Point Library?

An FPGA target-specific floating-point library is a set of floating-point IP blocks that is optimized for synthesis on specific FPGA hardware.

Altera Megafunctions and Xilinx LogiCORE IP are examples of such libraries.

### Why Map to an FPGA Target-Specific Floating Point Library?

Mapping to an FPGA target-specific floating-point library enables you to synthesize your floating-point design without having to do floating-point to fixed-point conversion. Eliminating the floating-point to fixed-point conversion step has the following advantages:

- Reduces the loss of data precision.
- Enables you to model a wider dynamic range.

- Saves time by skipping a step in the code generation process.

## Prerequisites for FPGA Target-Specific Floating-Point Library Mapping

To map your floating-point design to an Altera or Xilinx FPGA floating-point library, you must:

- Know which Altera or Xilinx FPGA you are using.
  - If you are using a Xilinx FPGA, set up your Xilinx FPGA target-specific floating-point library tool. See “Xilinx FPGA Target-Specific Floating Point Library Setup”.
- Set up your FPGA synthesis tool. See “Setting Up the Synthesis Tool Path”.

---

**Note** If you are using Altera Quartus 10.1 or 11.0, you must turn on the `AlteraBackwardIncompatibleSinCosPipeline` global property using `hdlset_param`. For example, to turn on `AlteraBackwardIncompatibleSinCosPipeline` for a model, `my_dut`, enter the following at the command line:

```
hdlset_param('my_dut', 'AlteraBackwardIncompatibleSinCosPipeline', 'on')
```

---

## Supported Xilinx Floating-Point Library Blocks

The coder can map to the following Xilinx LogiCORE IP operations:

LogiCORE IP Operation	Block Name
Add	<code>xilfp_add_sub</code>
Subtract	<code>xilfp_add_sub</code>
Multiply	<code>xilfp_mult</code>
Divide	<code>xilfp_div</code>
Compare	<code>xilfp_compare_&lt;mode&gt;</code>

<b>LogiCORE IP Operation</b>	<b>Block Name</b>
Convert	xilfp_convert_<from>_<to>
Sqrt	xilfp_sqrt

## Supported Altera Floating-Point Library Blocks

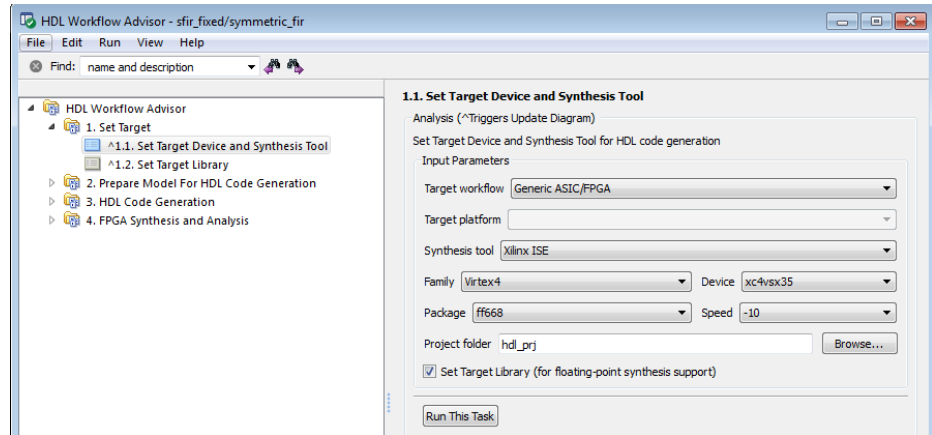
The coder can map to the following Altera Megafunction operations:

<b>Megafunction Operation</b>	<b>Block Name</b>
Add	altfp_add_sub
Subtract	altfp_add_sub
Multiply	altfp_mult
Divide	altfp_div
Compare	altfp_compare_<mode>
Convert	altfp_convert_<from>_<to>
Sqrt	altfp_sqrt
Inverse Sqrt	altfp_inv_sqrt
Abs	altfp_abs
Exp	altfp_exp
Inverse	altfp_inv
Log	altfp_log
Sine	altfp_sine
Cosine	altfp_cosine

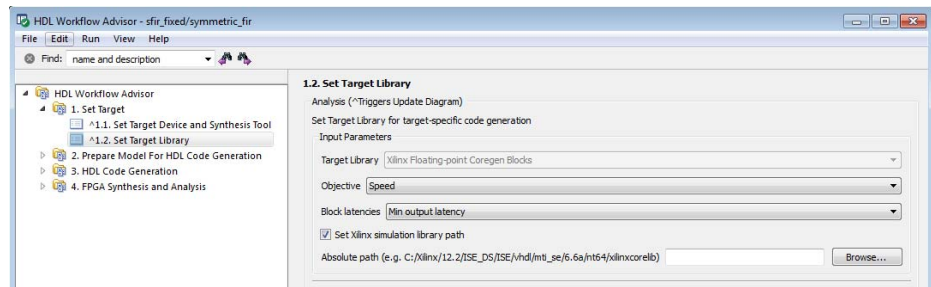
## How to Map to an FPGA Target-Specific Floating-Point Library

To map to an FPGA target-specific floating-point library:

- 1 Open the HDL Workflow Advisor.
- 2 In the left pane, click **HDL Workflow Advisor > Set Target > Set Target Device and Synthesis Tool**. The following Set Target Device and Synthesis Tool pane appears.



- 3 For **Target workflow**, select **Generic ASIC/FPGA**.
- 4 Select your **Synthesis tool** from the dropdown menu. The **Set Target Library (for floating-point synthesis support)** checkbox becomes available.
- 5 Select the **Family**, **Device**, **Package**, and **Speed** of your synthesis target.
- 6 Select **Set Target Library (for floating-point synthesis support)**. A new task, **Set Target Library**, appears in the left pane.
- 7 In the left pane, click **Set Target Library** to see the following pane.



**8 Select Objective and Block latencies.**

**9** (For Xilinx devices only) If you wish to enter the path to the pre-compiled simulation library, select **Set Xilinx simulation library path** and enter the **Absolute path**. Otherwise, the coder automatically detects the simulation library path.

## FPGA Target-Specific Library Mapping Results Analysis

To see your target-specific library mapping results, you must enable generation of the Resource Utilization Report and Optimization Report before you begin code generation. To learn how to generate these reports, see “Create and Use Code Generation Reports” on page 14-2.

The Resource Utilization Report shows the number of target-specific hardware resources used by your design. To learn more about the Resource Utilization Report, see “Resource Utilization Report Section” on page 14-23.

The Optimization Report shows whether the coder was able to meet the minimum or maximum block latencies you chose from the Set Target Library pane. To learn more about the Optimization Report, see “Optimization Report Section” on page 14-25.

## Limitations for FPGA Target-Specific Floating-Point Library Mapping

Data type limitations:

- Complex data type is not supported

- Conversion between double and single precision data types is not supported

Unsupported Simulink blocks:

- MATLAB Function
- Chart
- Truth Table
- FFT
- Lookup Tables
- RAMs
- Extract Bits
- MinMax
- DTI
- Counters
- Triggered subsystem

Unsupported Simulink block modes:

- Sum with ' - ' ports
- Sum with more than 2 inputs
- Product with more than 2 inputs
- Switch with a control input other than  $u2 \neq 0$ .
- Sum of Elements with an architecture other than Tree
- Product of Elements with an architecture other than Tree

Unsupported HDL Workflow Advisor modes:

- Cosimulation
- FPGA-in-the-Loop
- Turnkey

## FPGA Synthesis and Analysis

### In this section...

“FPGA Synthesis and Analysis Tasks Overview” on page 19-40

“Creating a Synthesis Project” on page 19-40

“Performing Synthesis, Mapping, and Place and Route” on page 19-43

“Annotating Your Model with Critical Path Information” on page 19-47

### FPGA Synthesis and Analysis Tasks Overview

The tasks in the **FPGA Synthesis and Analysis** folder let you run third-party FPGA synthesis and analysis tools without leaving the HDL Workflow Advisor environment. Tasks in this category include:

- Creation of FPGA synthesis projects for supported FPGA synthesis tools
- Launching supported FPGA synthesis tools to perform synthesis, mapping, and place/route tasks
- Annotation of your original model with critical path information obtained from the synthesis tools

---

**Note** A supported synthesis tool must be installed, and the synthesis tool executable must be on the system path to perform the tasks in the **FPGA Synthesis and Analysis** folder. See “Supported Third-Party Synthesis Tools” for more information.

---

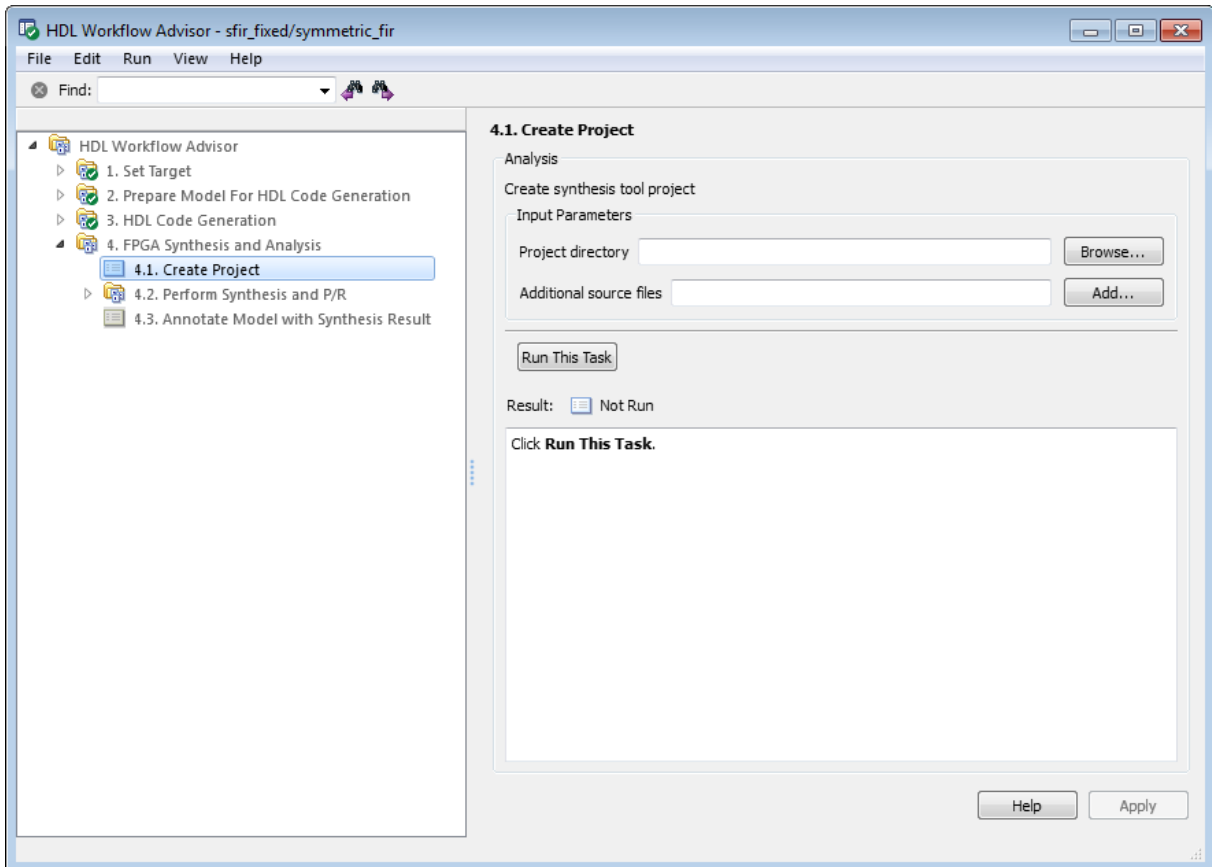
### Creating a Synthesis Project

The **Create Project** task does the following:

- Realizes a synthesis project for the tool from the previously generated HDL code
- Creates a link to the project files in the **Result** subpane
- (Optional) Launches the synthesis tool and opens the synthesis project



The following figure shows the **Create Project** task in an enabled state, after HDL code generation.

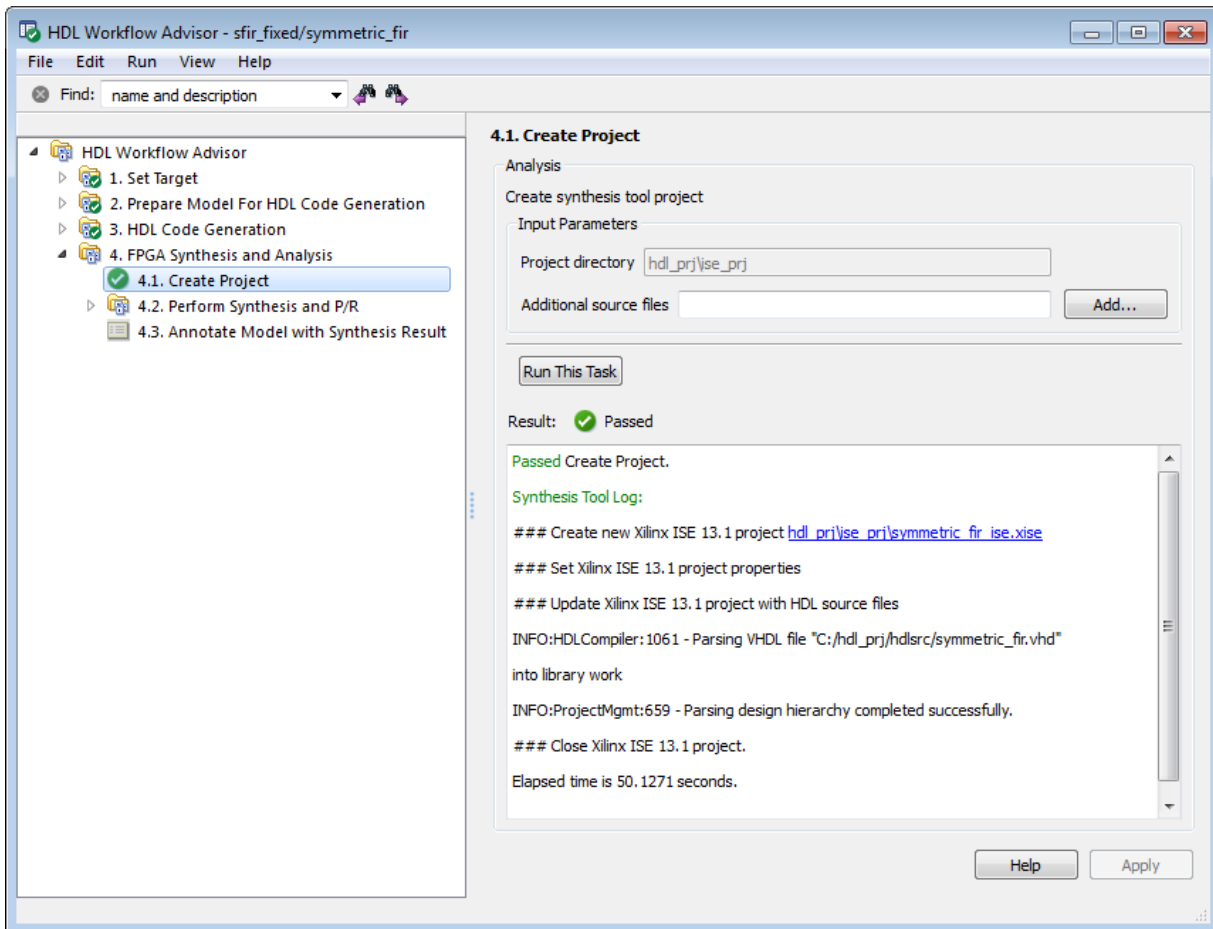


The **Create Project** task parameters are:

- **Project directory:** The HDL Workflow Advisor writes the project files to a subfolder of the `hdlsrc` folder. You can enter the path to an alternative folder, or click the **Browse** button to navigate to the desired folder.
- **Additional source files:** To include HDL files (or other synthesis files, such as UCF or SDC files) that the code does not generate in your synthesis

project, enter the full path to the desired files. Click the **Add** button to locate each file.

The following figure shows the HDL Workflow Advisor after passing the **Create Project** task. If you want to view the synthesis project, click the hyperlink in the **Result** subpane. This link launches the synthesis tool and opens the synthesis project.



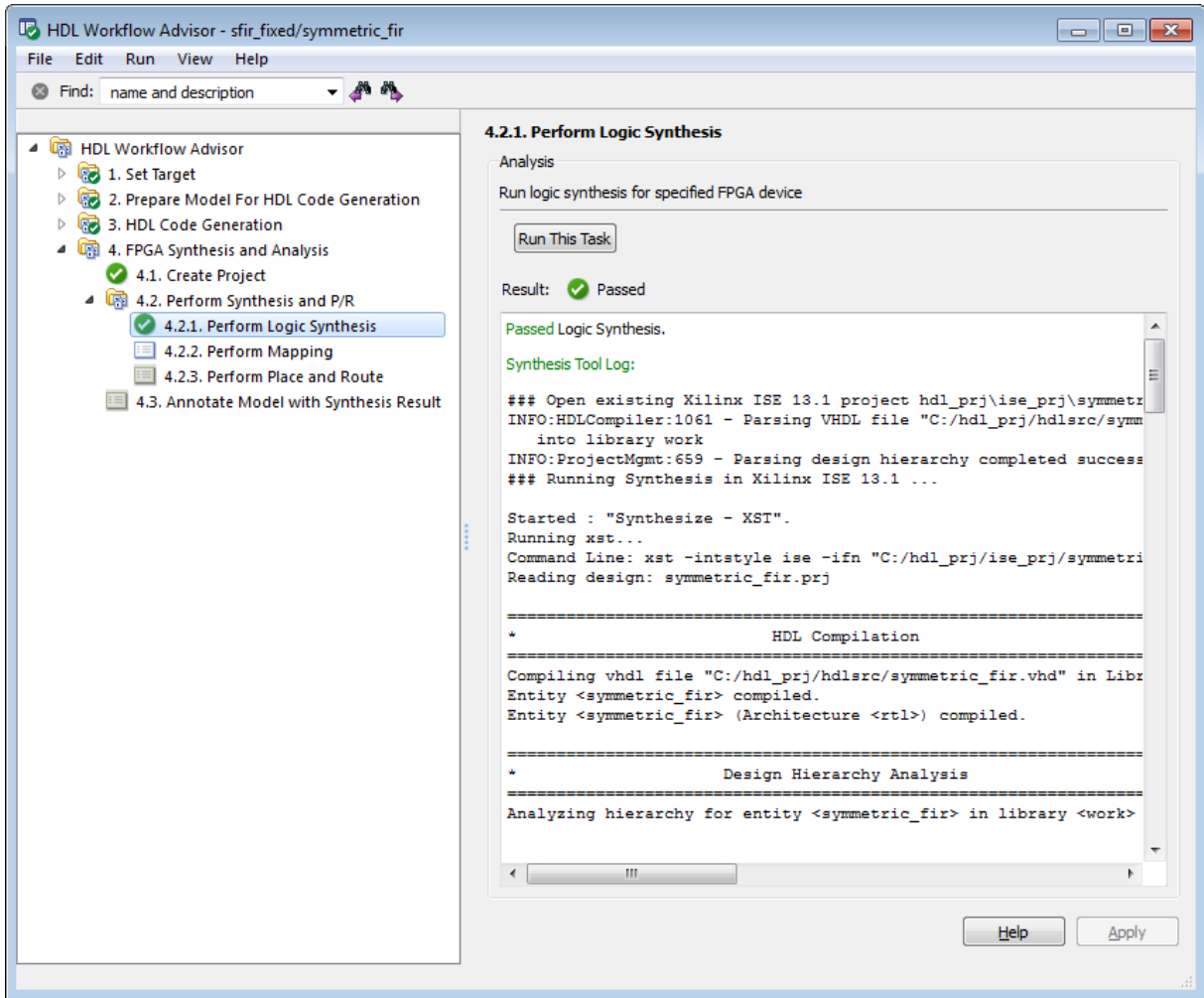
## Performing Synthesis, Mapping, and Place and Route

### Performing Logic Synthesis

The **Perform Logic Synthesis** task does the following:

- Launches the synthesis tool in the background.
- Opens the previously generated synthesis project, compiles HDL code, synthesizes the design and emits netlists and related files.
- Displays a synthesis log in the **Result** subpane.

The **Perform Logic Synthesis** task does not have input parameters. The following figure shows the HDL Workflow Advisor after passing the **Perform Logic Synthesis** task.



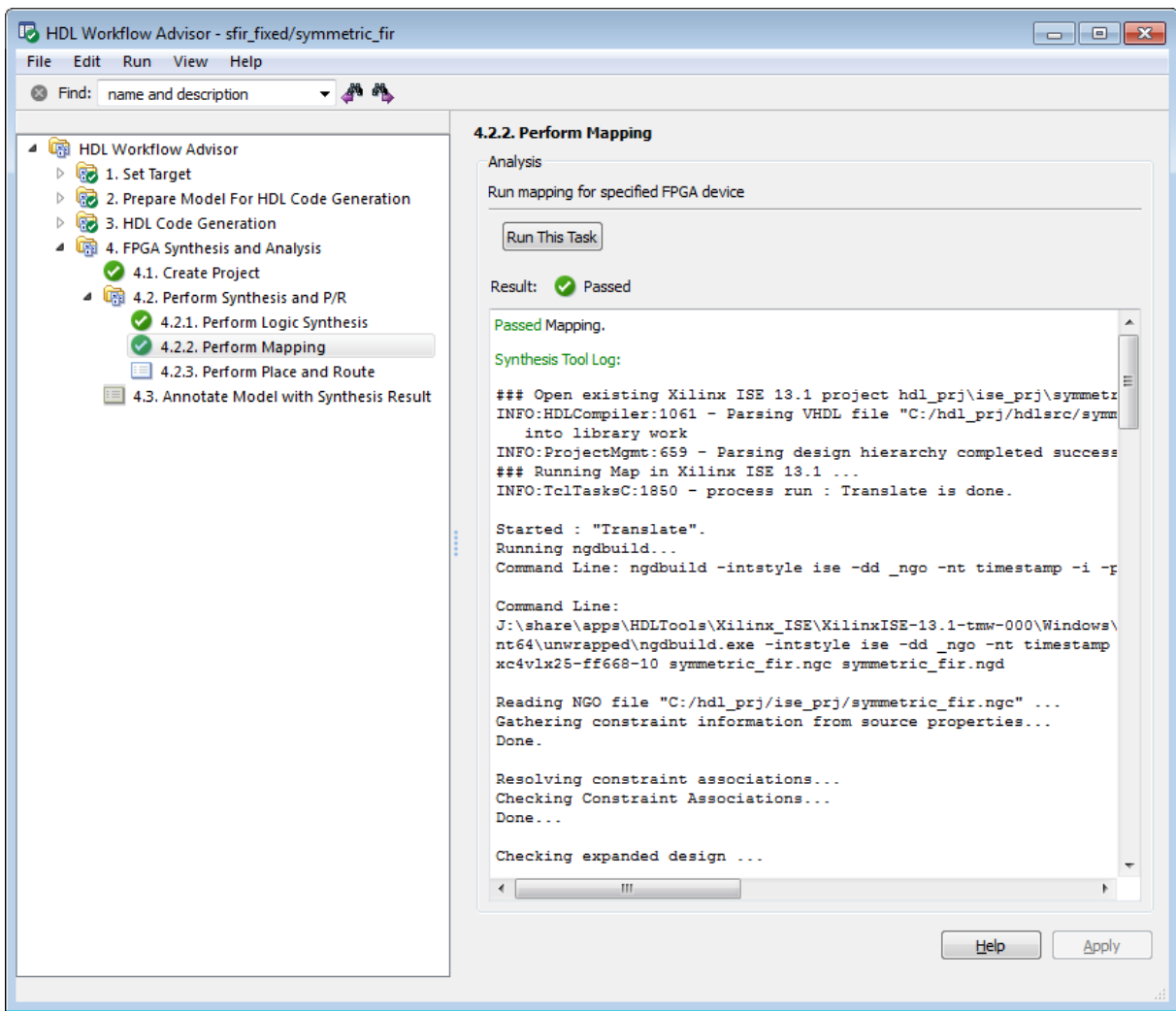
## Performing Mapping

The **Perform Mapping** task does the following:

- Launches the synthesis tool in the background.
- Runs a mapping process that maps the synthesized logic design to the target FPGA.

- Emits a circuit description file for use in the place and route phase.
- Displays a log in the **Result** subpane.

The **Perform Mapping** task does not have input parameters. The following figure shows the HDL Workflow Advisor after passing the **Perform Mapping** task.



## Performing Place and Route

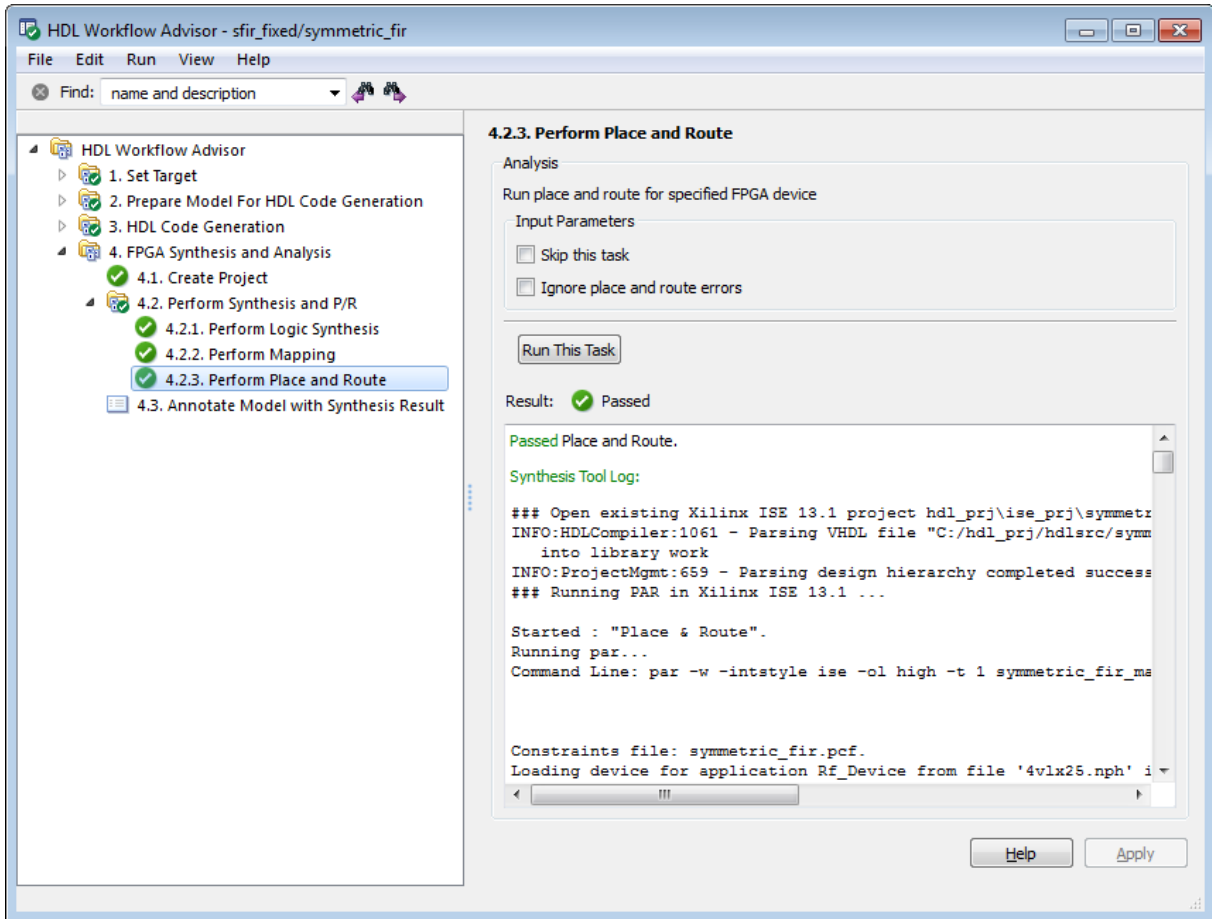
The **Perform Place and Route** task does the following:

- Launches the synthesis tool in the background.
- Runs a place and route process using the circuit description produced by the mapping process, and emits a circuit description suitable for programming an FPGA.
- Emits pre- and post-routing timing information for use in critical path analysis and back annotation of your source model.
- Displays a log in the **Result** subpane.

Unlike other tasks in the HDL Workflow Advisor hierarchy, **Perform Place and Route** is optional. If you select **Skip this task** in the right-hand pane, the HDL Workflow Advisor executes the workflow, but omits the **Perform Place and Route** task, marking it Passed. Select **Skip this task** if you prefer to do place and route work manually.

If the **Perform Place and Route** task fails, you can select **Ignore place and route errors** to continue to the **Annotate Model with Synthesis Result** task. This allows you to use post-mapping timing results to find critical paths in your model even if place and route fails.

The following figure shows the HDL Workflow Advisor after passing the **Perform Place and Route** task.



## Annotating Your Model with Critical Path Information

The **Annotate Model with Synthesis Result** task helps you identify critical paths in your model. In this task, you can analyze pre- or post-routing timing information from the **Perform Place and Route** task and visually highlight one or more critical paths in your model.

---

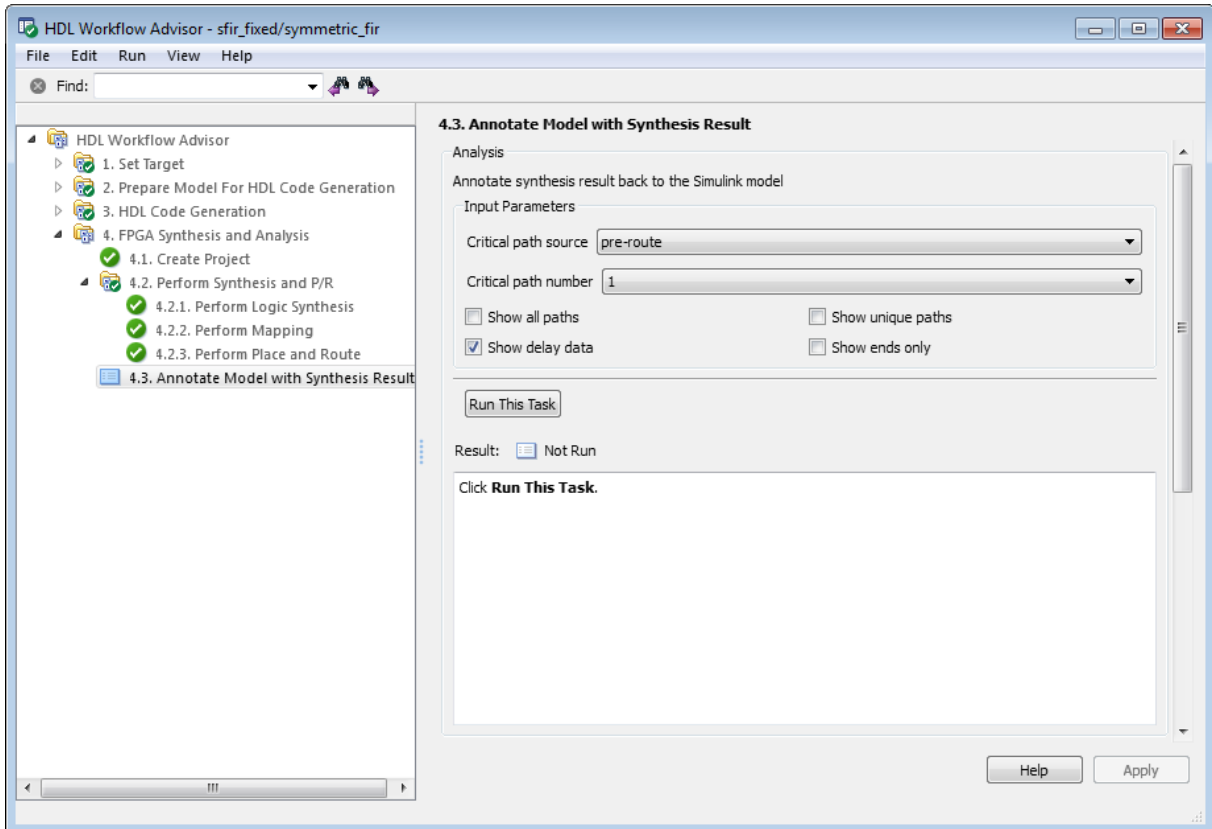
**Note** When you select a specific target device in the **Set Target Device and Synthesis Tool** task, **Generate FPGA top level wrapper** is automatically selected in the **Generate RTL Code and Testbench** task. In this case, the coder generates an HDL code wrapper and a constraint file that contains pin map information and clock constraints.

When **Generate FPGA top level wrapper** is selected, **Annotate Model with Synthesis Result** is not available. To perform back-annotation analysis, clear the check box for **Generate FPGA top level wrapper** in the **Generate RTL Code and Testbench** task.

---

The following figure shows the **Annotate Model with Synthesis Result** task in an enabled state.



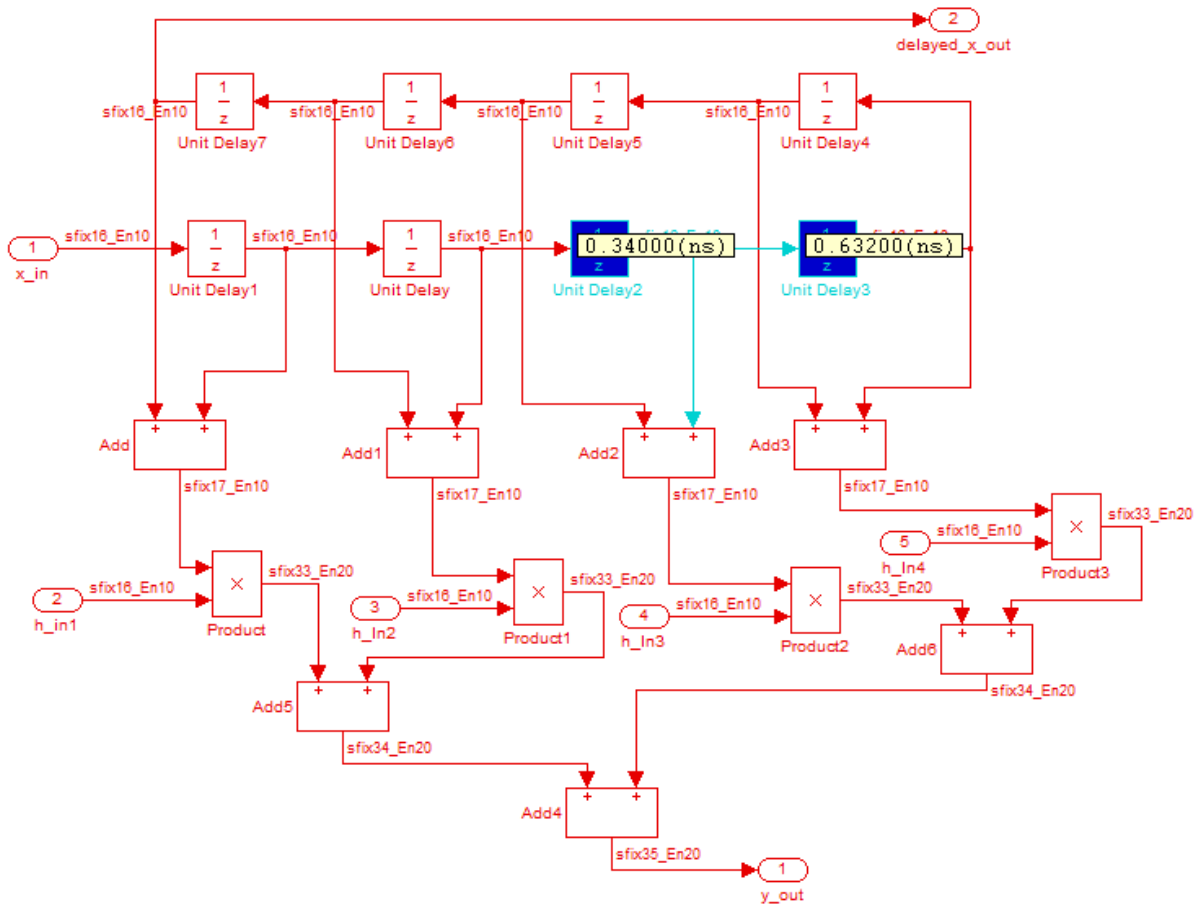


The task parameters are:

- **Critical path source:** Select pre-route or post-route. The default is pre-route.
- **Critical path number:** You can annotate up to 3 critical paths. Select the number of paths you want to annotate. The default is 1.
- **Show all paths:** Show critical paths, including duplicate paths. The default is off.
- **Show unique paths:** Show only the first instance of a path that is duplicated. The default is off.

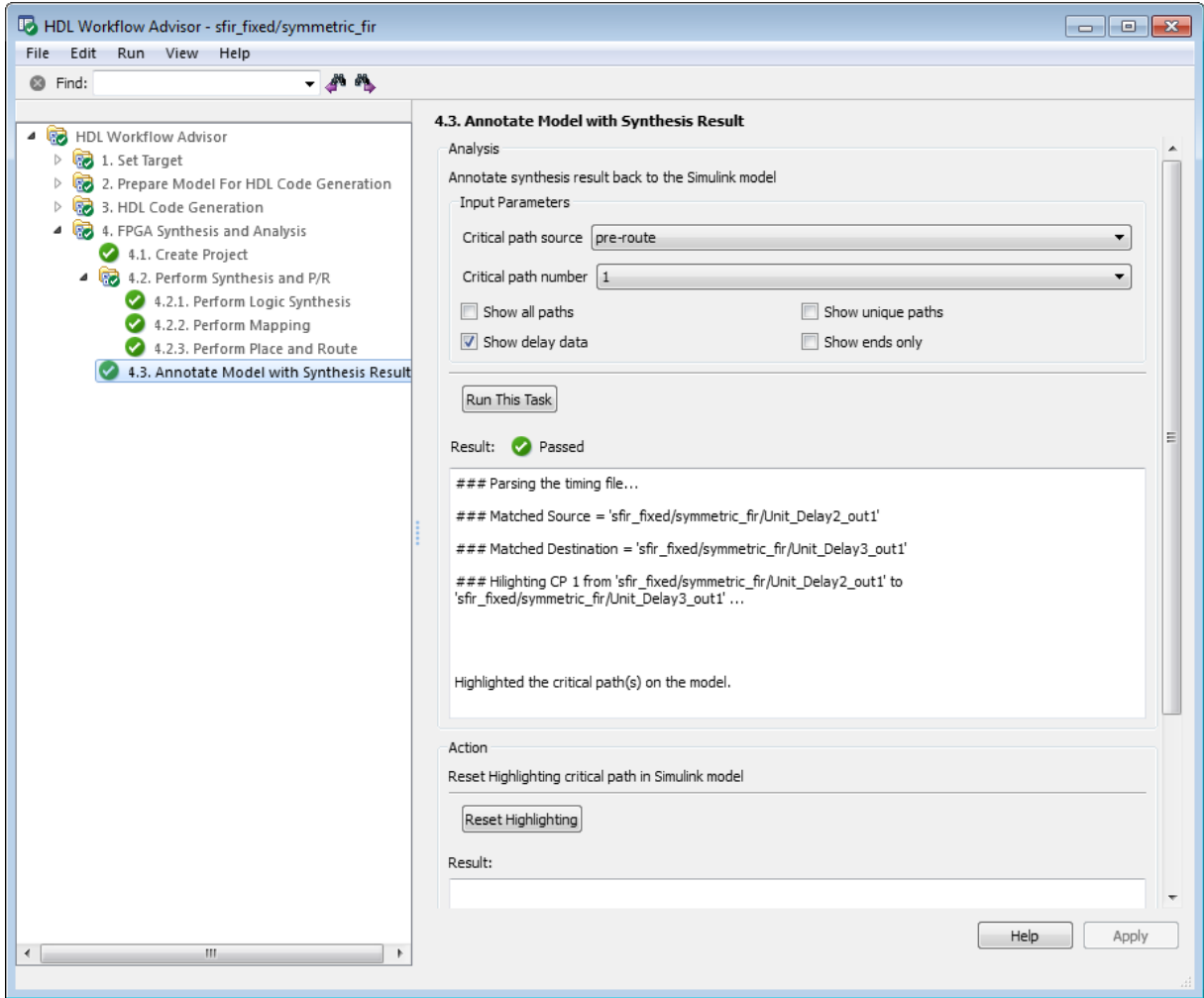
- **Show delay data:** Annotate the cumulative timing delay on each path. The default is on.
- **Show ends only:** Show the endpoints of each path, but omit the connecting signal lines. The default is off.

When the **Annotate Model with Synthesis Result** task runs to completion, the coder displays the DUT with critical path information highlighted. The following figure shows a subsystem after critical path annotation. Using default options, the annotation includes the endpoints, signal lines, and delay data.



After the **Annotate Model with Synthesis Result** task runs to completion, the HDL Workflow Advisor enables the **Reset Highlighting** button in the **Action** subpane. When you click this button, the HDL Workflow Advisor:

- Clears critical path annotations from the model.
- Resets the **Annotate Model with Synthesis Result** task.



## FPGA-in-the-Loop

### In this section...

“How FPGA-in-the-Loop Works” on page 19-53

“Using the HDL Workflow Advisor for FPGA-in-the-Loop” on page 19-55

### How FPGA-in-the-Loop Works

- “FPGA-in-the-Loop Process” on page 19-53
- “Design Considerations for FPGA-in-the-Loop” on page 19-55

### FPGA-in-the-Loop Process

FPGA-in-the-Loop (FIL) provides the capability to use Simulink for testing designs in real hardware for any suitable DUT. The HDL code is generated using the HDL Coder software. FIL then performs the following actions:

- Generates a Simulink FIL block that represents the HDL code
- Creates a programming file and loads the design onto an FPGA
- Transmits data from Simulink to the FPGA
- Receives data from the FPGA
- Exercises the design in a real environment

FIL, along with your FPGA design software, provides block generation, synthesis, logical mapping, PAR (place-and-route), programming file generation, and a communications channel. These capabilities are specifically designed for a particular board and tailored to your RTL code. You must have an HDL Verifier license for FIL.

The following sections explain more about the FIL block generation process:

- “FPGA-in-the-Loop Programming File” on page 19-54
- “Communication Channel” on page 19-54
- “Downstream Workflow Automation” on page 19-54

**FPGA-in-the-Loop Programming File.** The FIL process adds the logic the DUT needs to communicate with Simulink. Generally, the size of the additional logic is very small and has minimal impact on the fit of your design onto the FPGA.

---

**Note** If a design does not fit in the device or does not meet timing goals, the coder software cannot create the programming file. In such situations, you may see a warning that the design does not meet the timing goals. Either make changes to some part of your design, or use a different development board.

---

You may not need to make changes to the generated FIL block. Whether or not you change values on the FIL block depends on your Simulink model. You should review the FIL block settings, and make adjustments, if they are required, for your Simulink design.

**Communication Channel.** FIL provides the communication channel for sending and receiving data between Simulink and the FPGA. This channel uses a Gigabit Ethernet connection. Because communication between Simulink and the FPGA is strictly synchronized, the FIL simulation provides a more dependable verification method.

**Downstream Workflow Automation.** To create the FIL programming file, the software performs the following tasks:

- Generates HDL code for the specified DUT and creates an ISE project.
- Along with the FPGA design software, synthesizes, maps, places and routes, and creates a programming file for the FPGA.
- Downloads the programming file to the FPGA on the development board through the board's normal configuration connection. Typically, that connection is a serial line over a USB cable (see board manufacturer's instructions for how to make this connection).

Clicking **Load** on the FIL block mask initiates the programming file download.

## Design Considerations for FPGA-in-the-Loop

Keep the following rules in mind when you design the DUT to be used with FIL.

- Use Single tasking solver mode (set with Configuration Parameters). FIL does not support multitasking solver mode.
- Use discrete, fixed step solvers or variable-step solvers. FIL supports both types of solvers.
- Incompatibilities with Simulink

Be aware that HDL Verifier FIL simulation currently does not support the following:

- Instantiation of the FIL block in a triggered subsystem
- Instantiation of the FIL block in an asynchronous function-call subsystem
- A continuous sample time
- A nonzero sample time offset

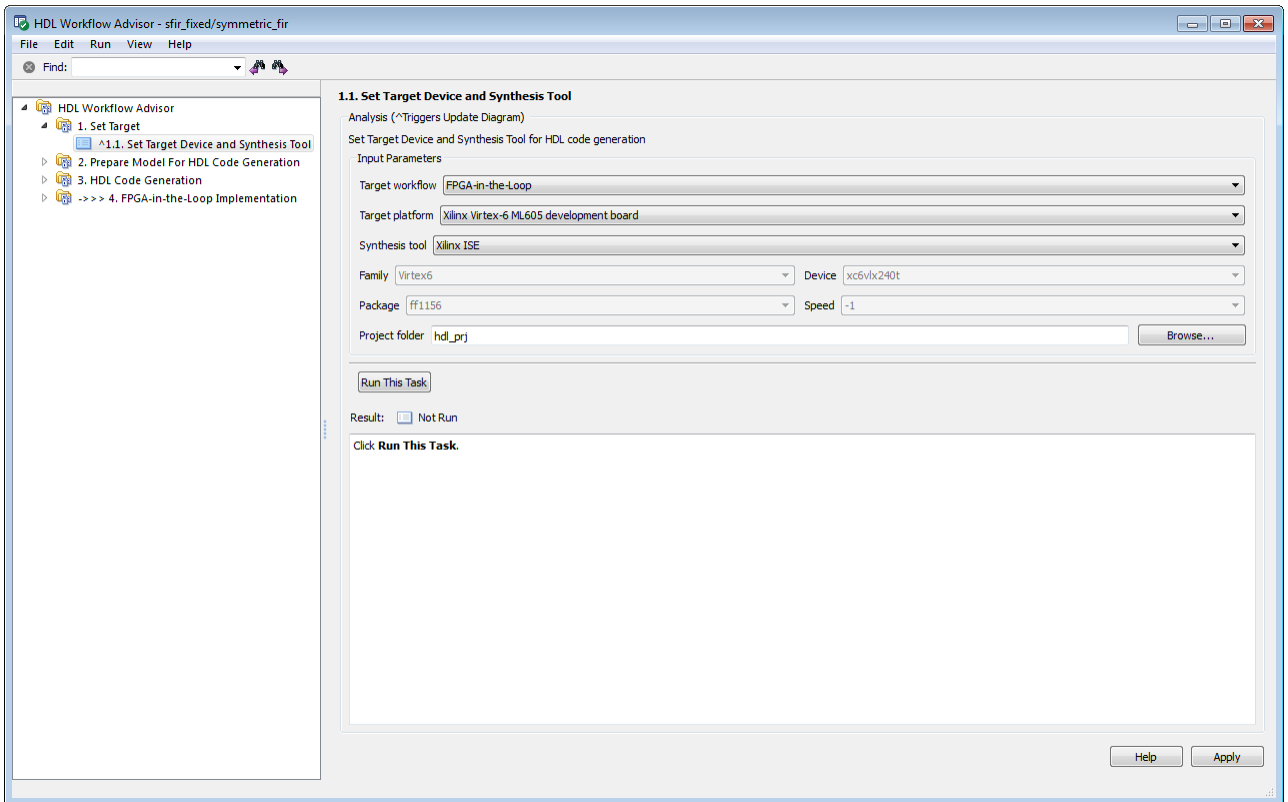
**Incompatibilities with Simulink.** With the current release, HDL Verifier FIL simulation does not support the following:

## Using the HDL Workflow Advisor for FPGA-in-the-Loop

The following steps describe how to use the HDL Workflow Advisor for creating and executing FIL. Before you begin, verify that you have a supported version of your FPGA design software installed and the tool executable is reachable from your system path.

- 1 Follow instructions for invoking the HDL Workflow Advisor. See “Open the HDL Workflow Advisor” on page 19-3.
- 2 At step 1, **Set Target**, click **1.1 Set Target Device and Synthesis Workflow** and do the following:
  - Select **FPGA-in-the-Loop** from the dropdown list at **Target Workflow**.

- b** Under **Target Platform**, select a development board from the dropdown list. **Family**, **Device**, **Package**, and **Speed** are filled in by the HDL Workflow Advisor.
- c** For **Folder**, enter the folder name where the project files are to be placed. The default is `hdl_prj` under the current working folder.



- 3** At step 2, **Prepare Model for HDL Code Generation**, perform steps 2.1–2.4 as described in “Prepare Model For HDL Code Generation Overview” on page 21-10.

In addition, perform step 2.5 **Check FPGA-in-the-Loop Compatibility** to verify that the model is compatible with FIL.



- 4** At step 3, **HDL Code Generation**, perform steps 3.1 and 3.2 as described in “HDL Code Generation Overview” on page 21-17.
- 5** At step 4.1, **Set FPGA-in-the-Loop Options**, change these options if required:
- Adjust the board IP and MAC addresses.

Address	Instructions
<b>Board IP address</b>	<p>Use this option for setting the board’s IP address if it is not the default IP address (192.168.0.2).</p> <p>You may need to change your computer’s IP address to a different subnet from 192.168.0.x when you set up the network adapter. You would also need to change the address if the default board IP address 192.168.0.2 is in use by another device. If so, change the Board IP address according to the following guidelines:</p> <ul style="list-style-type: none"> <li>• The subnet address, typically the first three bytes of board IP address, must be the same as those of the host IP address.</li> <li>- The last byte of the board IP address must be different from that of the host IP address.</li> <li>- The board IP address must not conflict with the IP addresses of other computers.</li> </ul> <p>For example, if the host IP address is 192.168.8.2, then you can use 192.168.8.3, if available.</p>
<b>Board MAC address</b>	<p>Under most circumstances, you do not need to change the Board MAC address. You will need to do so if you connect more than one FPGA development board to a single computer. (You must have a separate NIC for each board.) You must change the Board MAC address for additional boards so that each address is unique.</p>

Address	Instructions
	To change the Board MAC address, click in the <b>Board MAC address</b> field. Specify an address that is different from that belonging to any other device attached to your computer. To obtain the Board MAC address for a specific FPGA development board, refer to the label affixed to the board or consult the product documentation.

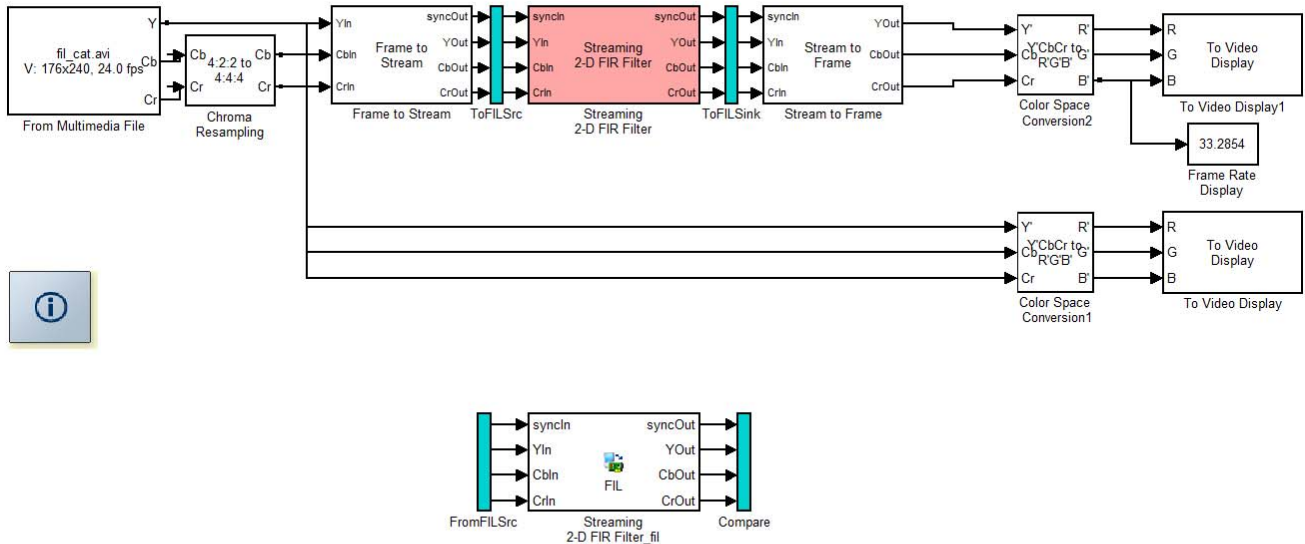
- Specify additional files.

At **Specify additional source files for the HDL design**, indicate additional source files for the DUT using **Add**. To (optionally) display the full paths to the source files, check the box titled **Show full paths to source files**. The HDL Workflow Advisor attempts to identify the source file; if the file type is incorrect, you can fix it by selecting from the dropdown list at **File Type**.

- 6 At step 4.2, **Build FPGA-in-the-Loop**, click **Run this task**.

During the build process, the following actions occur:

- The HDL Workflow Advisor generates a FIL block named after the top-level module and places it in a new model. The next figure shows an example of the new model containing the FIL block.



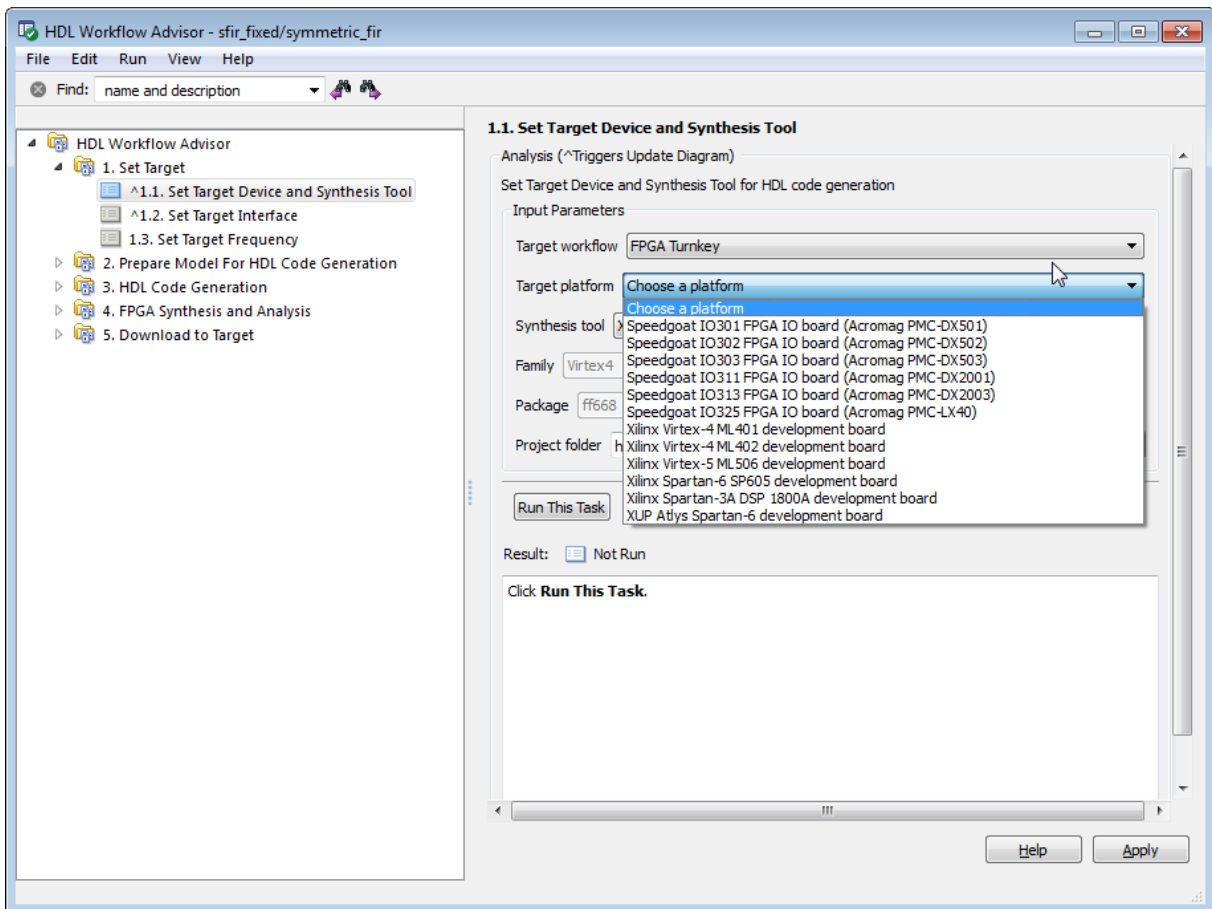
- After new model generation, the HDL Workflow Advisor opens a command window:
  - In this window, the FPGA design software performs synthesis, fit, PAR, timing analysis, and FPGA programming file generation.
  - When the process completes, a message in the command window prompts you to close the window.
- The HDL Workflow Advisor builds a testbench model around the generated FIL block.

## 7 Download FPGA programming file and run FIL simulation.

See the instructions for “Performing FPGA-in-the-Loop Simulation” in the HDL Verifier product documentation.

## Automated Workflows for Specific Target Devices and Synthesis Tools

The HDL Workflow Advisor helps you perform complete automated workflows for a number of target devices. The **Target platform** menu of the **Set Target Device and Synthesis Tool** task lists the supported target devices.



After you select the desired target device and configure its I/O interface, you can let the HDL Workflow Advisor perform the subsequent model checking, HDL code generation, and FPGA synthesis and analysis tasks, without

your intervention. See the following sections for information on automated workflows for specific types of targets:

- “xPC Target Interface Generation for Speedgoat Boards” on page 19-62
- “Target Xilinx FPGA Development Boards” on page 19-72

## xPC Target Interface Generation for Speedgoat Boards

### In this section...

“Select a Speedgoat Target Device” on page 19-62

“Set the Target Interface for Speedgoat Boards” on page 19-65

“Code Generation, Synthesis, and Generation of xPC Target Interface Subsystem” on page 19-69

This example shows how to generate a hardware-in-the-loop interface for Speedgoat board programming with xPC Target.

To run this example, you must:

- Have a license for xPC Target software.
- Use Xilinx ISE 10.1.

### Select a Speedgoat Target Device

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**Note** Before selecting a Speedgoat target device, see “Supported Third-Party Synthesis Tools”.

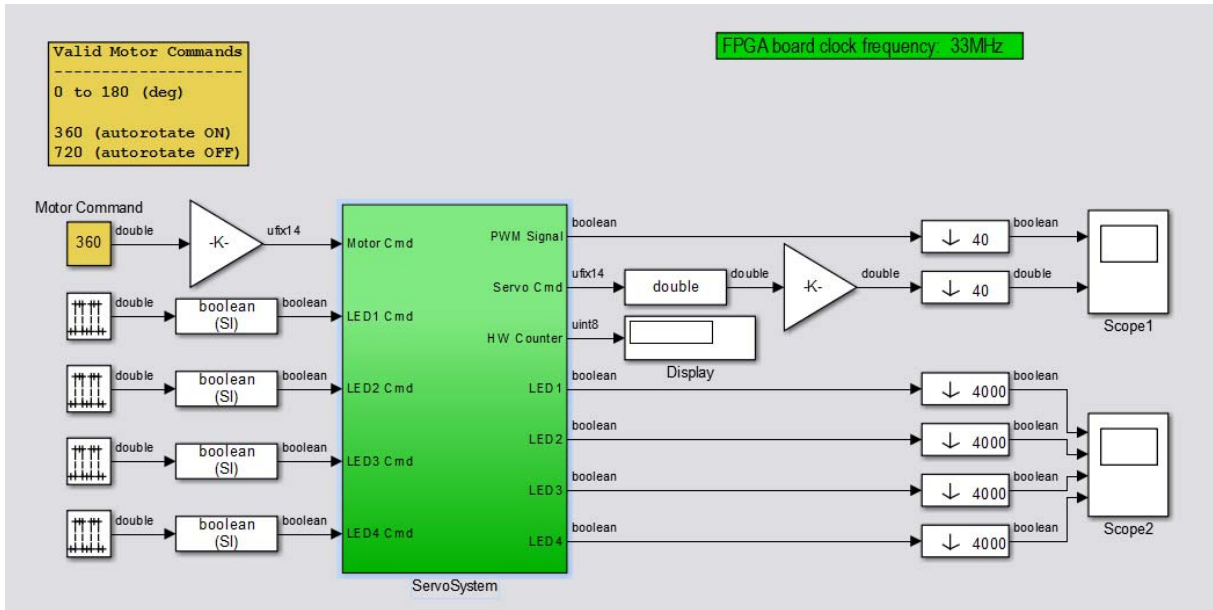
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To select a target Speedgoat board:

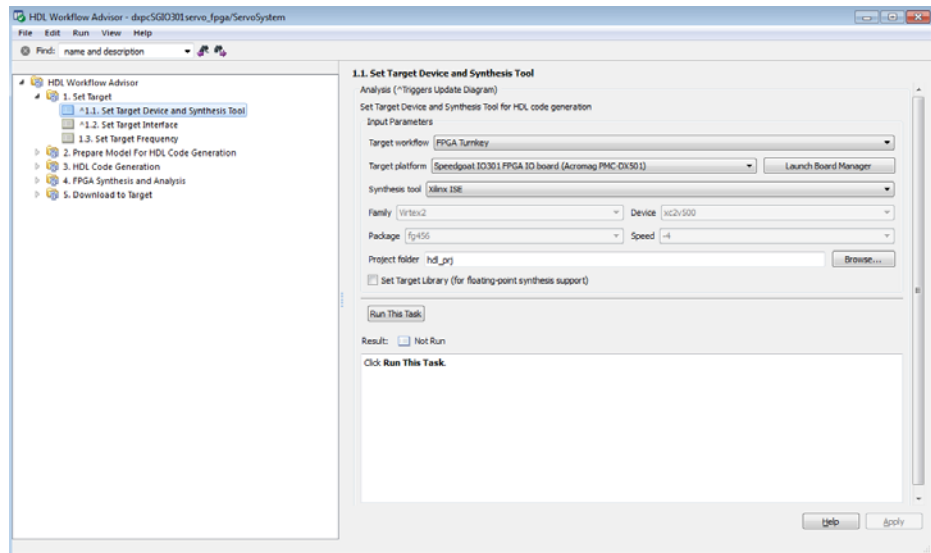
- 1 Open the model.

```
dxpcSGI0301servo_fpga
```

The `ServoSystem` subsystem is the device under test (DUT) for HDL code generation.



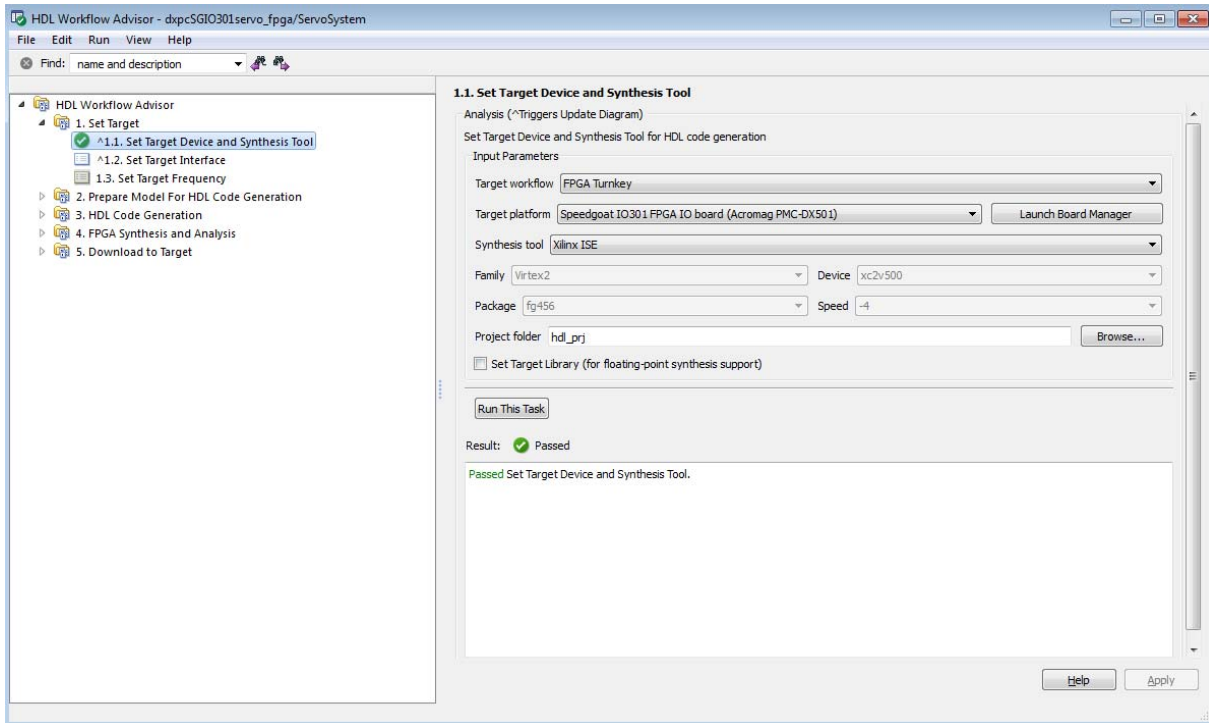
- Right-click the ServoSystem block, and select **HDL Code > HDL Workflow Advisor**.
- In the HDL Workflow Advisor, select **Set Target > Set Target Device and Synthesis Tool**.
- Set **Target workflow** to **FPGA Turnkey**. On the left, the **Set Target Interface** and **Set Target Frequency** steps appear under **Set Target** along with the **FPGA Synthesis and Analysis** and **Download to Target** tasks.
- From the **Target platform** menu, select the Speedgoat IO301 board. xPC Target and HDL Workflow Advisor support the same set of Speedgoat devices. For a list of supported boards, see “FPGA Support”.



## 6 Click Run This Task.

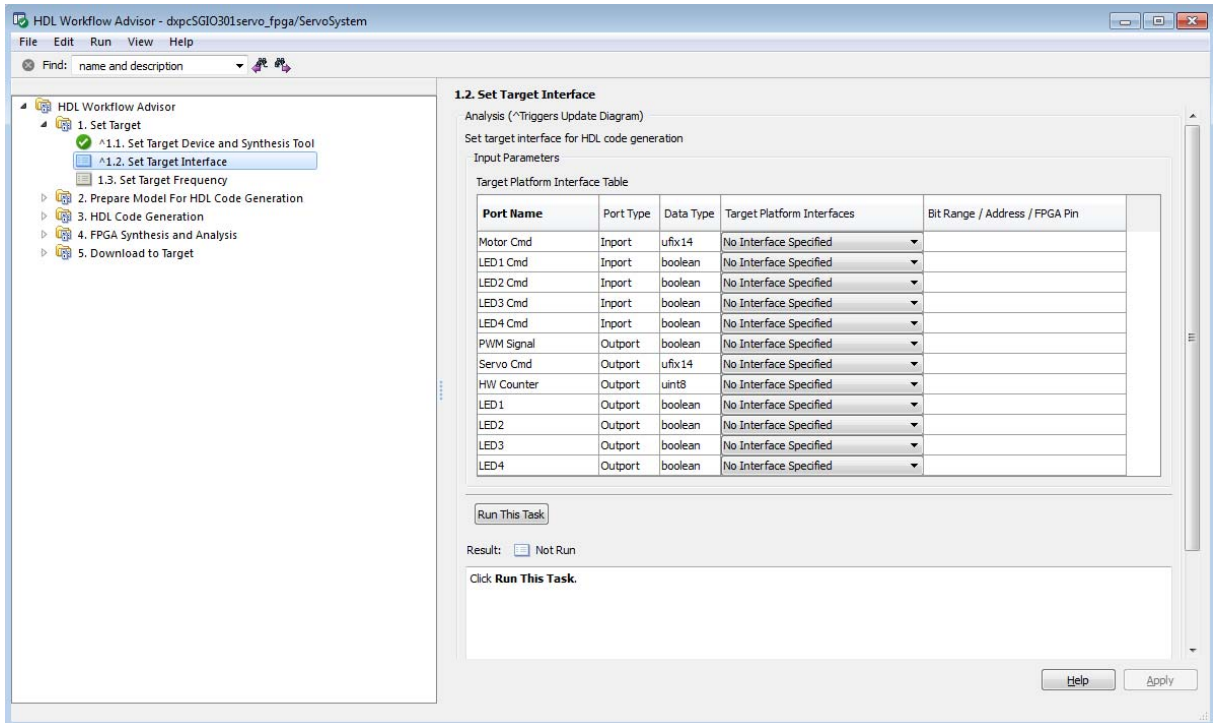
After the **Set Target Device and Synthesis Tool** task is complete, the HDL Workflow Advisor enables the next task in the hierarchy, **Set Target Interface**. After the **Set Target Device and Synthesis Tool** task runs, the HDL Workflow Advisor looks like this figure.





## Set the Target Interface for Speedgoat Boards

The **Set Target Interface** task in the HDL Workflow Advisor enables you to define how the inputs and outputs of the DUT map to the inputs and outputs of your Speedgoat target device.



Using the **Target Platform Interface** and **Bit Range / Address / FPGA Pin** columns, you can allocate each port on the DUT to an I/O resource on the target device. To allocate ports:

- 1 In the left pane of the HDL Workflow Advisor, select the **Set Target Interface** task.
- 2 In the Target Platform Interface Table, click the **Target Platform Interfaces** column for a port that you want to allocate. The HDL Workflow Advisor displays a dropdown list with the available I/O resources for the target device.
- 3 Select an option from the menu. The **Target Platform Interfaces** menu has the following options for each port:
  - **No Interface Specified** (default): The port is not allocated to a resource on the target device.

- **Specify FPGA Pin {'LSB', ..., 'MSB'}**: Enter one or more FPGA pin names as a cell array of strings. In the **Bit Range / Address / FPGA Pin** column, enter the pin name specification. The number of pin names must equal the width of the port on the DUT. For the required format for pin names, see your Speedgoat board documentation.
- **TTL I/O Channel [0:63]**: The port is allocated to a specified bit position [b] or range of bit positions [lsb:msb]. The width of the specification, in bits, must equal the width of the port on the DUT.

When you select **TTL I/O Connector [0:63]**, the HDL Workflow Advisor automatically allocates a bit range.

- **PCI Interface**: Specifies an address (in hexadecimal) in the 32-bit PCI address space of the Speedgoat target device. PCI addresses increase in increments of 4 (for example, x"8100", x"8104", ...).

When you select **PCI Interface**, the HDL Workflow Advisor automatically allocates the next available address, starting at x"8100".

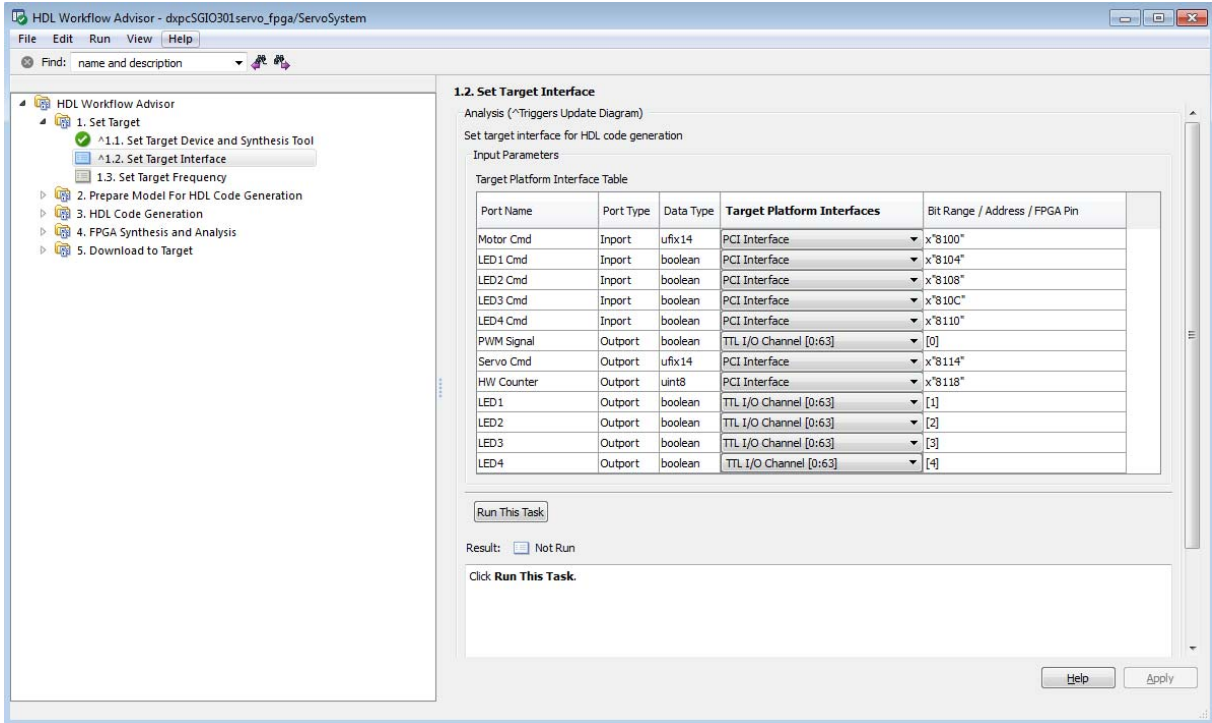
The PCI interface supports both scalar and vector data types. The coder automatically generates PCI DMA transfers for large vectors.

If you select **TTL I/O Connector [0:63]** or **PCI Interface**, the HDL Workflow Advisor automatically displays a default bit range or address in the **Bit Range / Address / FPGA Pin** column.

To change a value entered by the HDL Workflow Advisor, double-click in the **Bit Range / Address / FPGA Pin** column and edit the value.

- 4 Allocate ports as required by your design. When you have finished allocating ports, click **Apply**.

This figure shows the Target Platform Interface Table in a typical configuration. All ports have been allocated to a PCI Interface address or a single bit on the TTL I/O Connector.



**Note** At least one output port must be allocated to the target device. If all ports are left unallocated, the **Set Target Interface** task shows an error and terminates.

**5** Click **Run This Task**.

**6** In the **Set Target Frequency** task, set your FPGA clock frequency and click **Run This Task**.

## Code Generation, Synthesis, and Generation of xPC Target Interface Subsystem

After selecting the target device and configuring its port interface, you can enable the HDL Workflow Advisor to perform the next sequence of tasks automatically. These tasks include:

- **Prepare Model For HDL Code Generation:** Checking the model for HDL code generation compatibility.
- **HDL Code Generation:** Setting HDL-related options of the Model Configuration Parameters dialog box and generating HDL code.
- **FPGA Synthesis and Analysis:** Executing synthesis and timing analysis in Xilinx ISE; back annotating the model with critical path information obtained during synthesis.
- **Download to Target :** Generating an FPGA programming file and a model that contains an xPC Target interface subsystem.

---

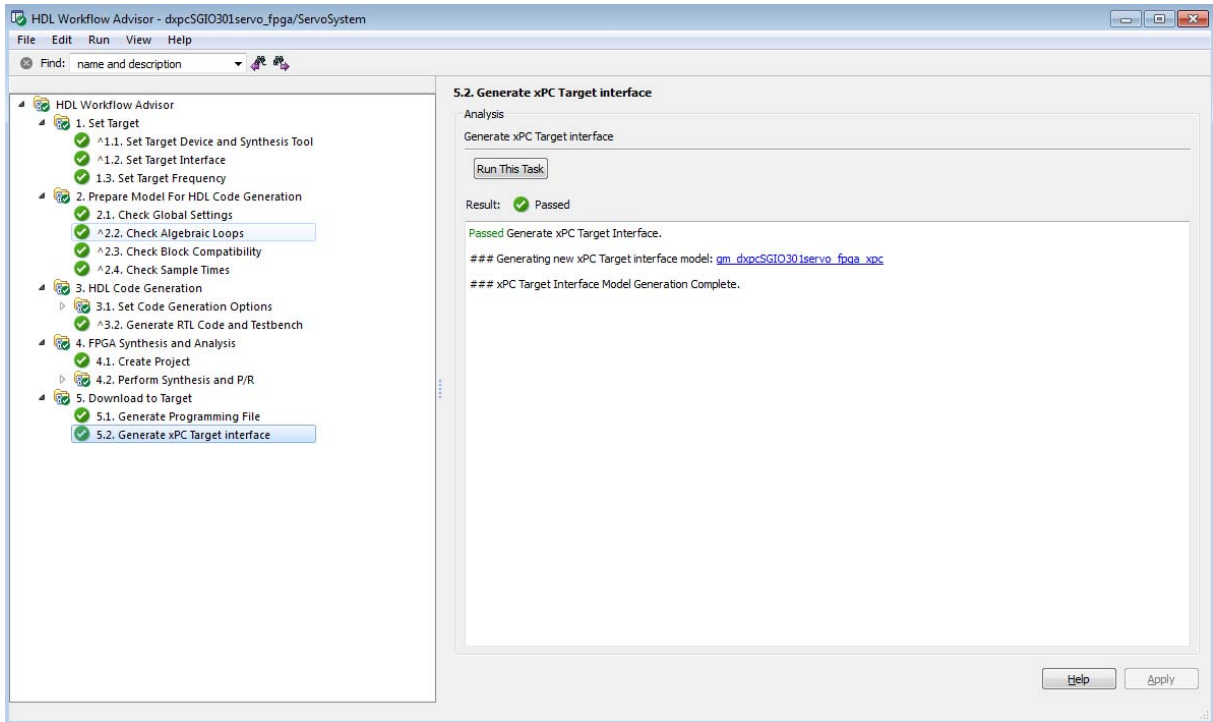
**Note** The **Download to Target** tasks do not actually download anything to a target device. They create an interface subsystem that you can plug into an xPC Target model.

---

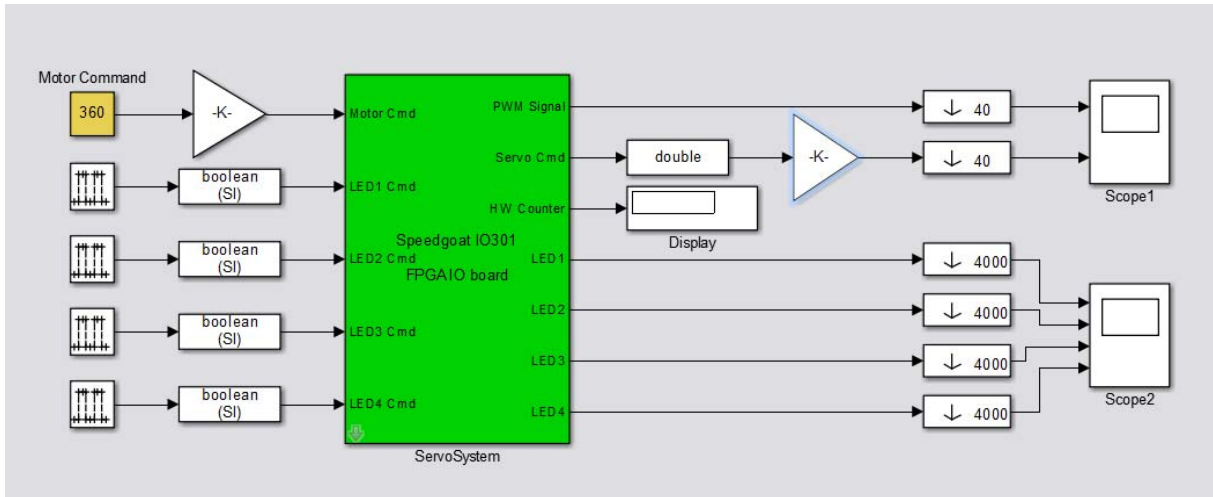
To run this sequence of tasks automatically:

- 1** Open the **Download to Target** task group.
- 2** Right-click **Generate xPC Target interface** and select **Run to Selected Task**.
- 3** As the **Run to Selected Task** sequence executes, the HDL Workflow Advisor displays a progress indicator for each task.

After the task sequence is complete, you see the **Result** subpane.



**4** The **Result** pane displays a link to a generated model — `gm_dxpcSGIO301servo_fpga_xpc`. Click the link to open the model.



The model contains the xPC Target interface subsystem. This new subsystem replaces the DUT (ServoSystem) in the original model. It replaces the internals of the original DUT with an xPC Target FPGA block and other blocks to work with the algorithm on the FPGA.

- 5** Save the gm\_dxpcSGI0301servo\_fpga\_xpc model.
- 6** To learn how to use the generated model with xPC Target, see “FPGA Models” in the xPC Target documentation.

## Target Xilinx FPGA Development Boards

### In this section...

“Select the Target Device” on page 19-72

“Set the Target Interface” on page 19-74

“Code Generation, Synthesis, and Programming of Target Device” on page 19-78

This example shows how to target a Xilinx FPGA development board for synthesis.

The `hdlcoderUARTServoControllerExample` model is designed to work with a Xilinx Virtex-5 ML506 development board. The `UART_Servo_on_FPGA` subsystem receives commands through UART ports. The subsystem generates a pulse width modulation (PWM) waveform to control a servo motor.

### Select the Target Device

---

**Note** Before selecting a Xilinx target device, see “Supported Third-Party Synthesis Tools”.

---

To select the Virtex-5 ML506 development board as the target device:

- 1 Add the example directory to your MATLAB path.

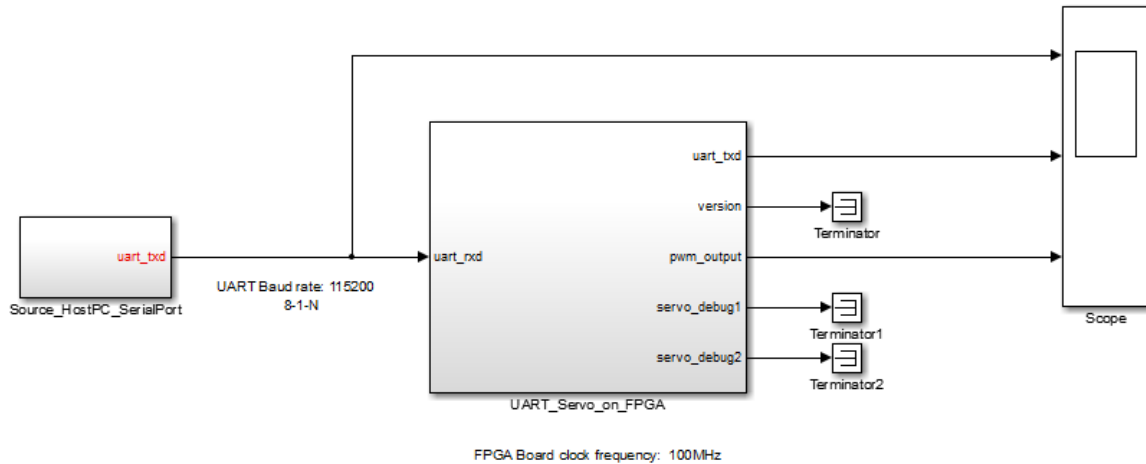
```
addpath(fullfile(docroot, 'toolbox', 'hdlcoder', 'examples'))
```

- 2 Open the model.

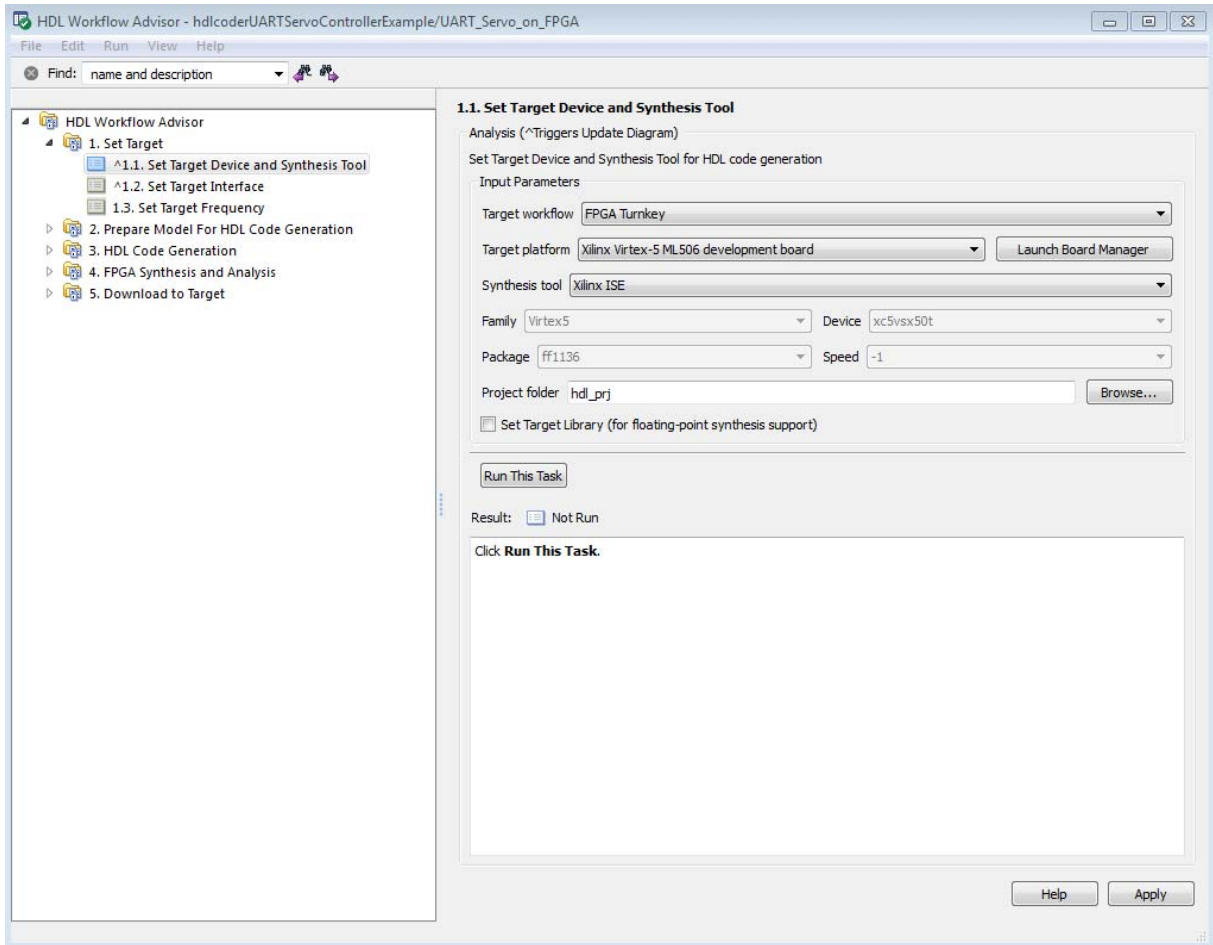
```
hdlcoderUARTServoControllerExample
```



Example of an FPGA Servo Motor Controller with UART interface



- 3** Right-click the `UART_Servo_on_FPGA` subsystem and select **HDL Code > HDL Workflow Advisor**.
- 4** In the HDL Workflow Advisor, select **Set Target > Set Target Device and Synthesis Tool**.
- 5** Set **Target workflow** to `FPGA Turnkey`.
- 6** Set **Target platform** to `Xilinx Virtex-5 ML506 development board`.

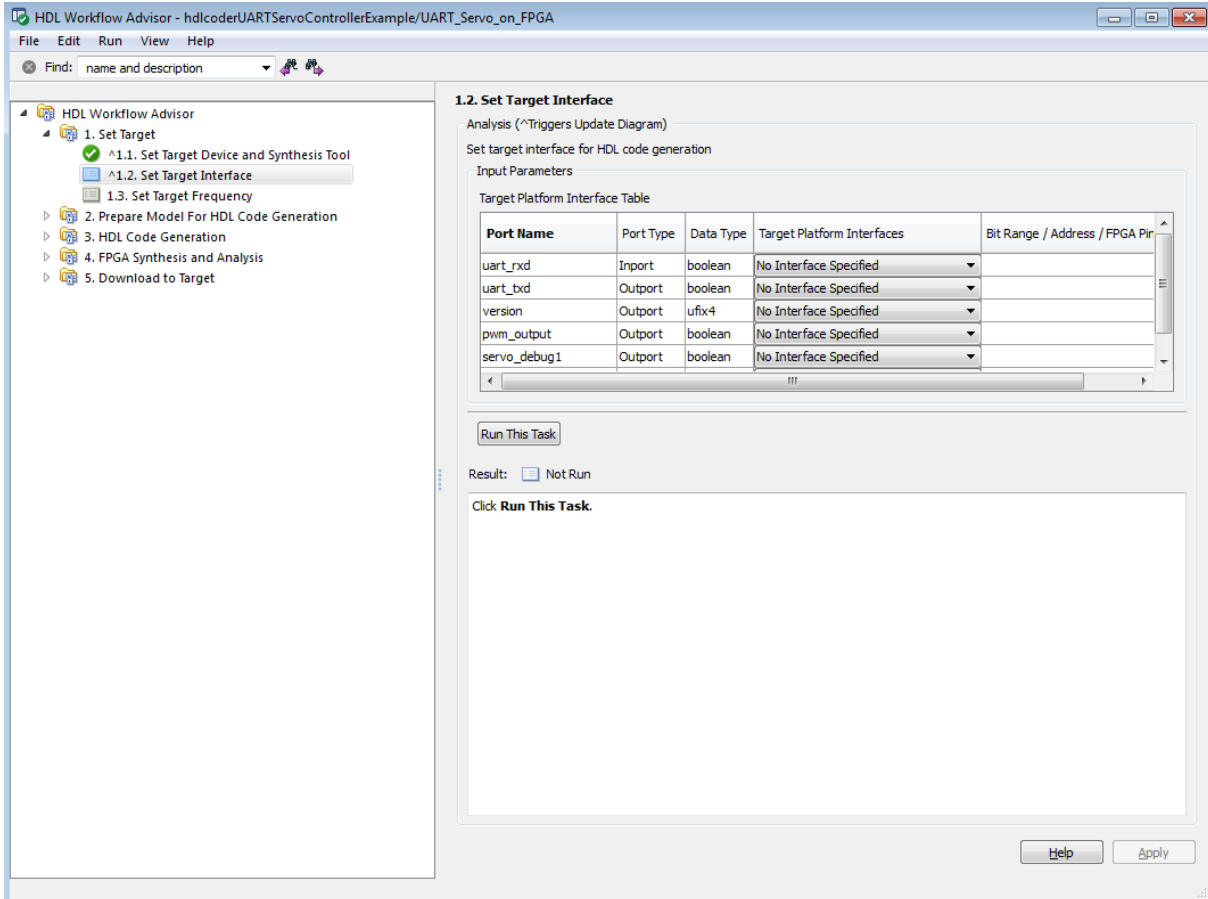


7 Click **Run This Task** .

## Set the Target Interface

To map the inputs and outputs of the DUT to the Xilinx Virtex-5 ML506 device:

- 1 In the left pane of the HDL Workflow Advisor, click **Set Target Interface**. The figure shows the initial state of the Target Platform Interface Table.



- 2** For each port, select an option from the **Target Platform Interfaces** menu.

For detailed information on each **Target Platform Interfaces** option, see your Xilinx Virtex-5 ML506 development board documentation. This example uses only the following options:

- RS232 Serial Port Rx
- RS232 Serial Port Tx
- LEDs General Purpose [0 7]

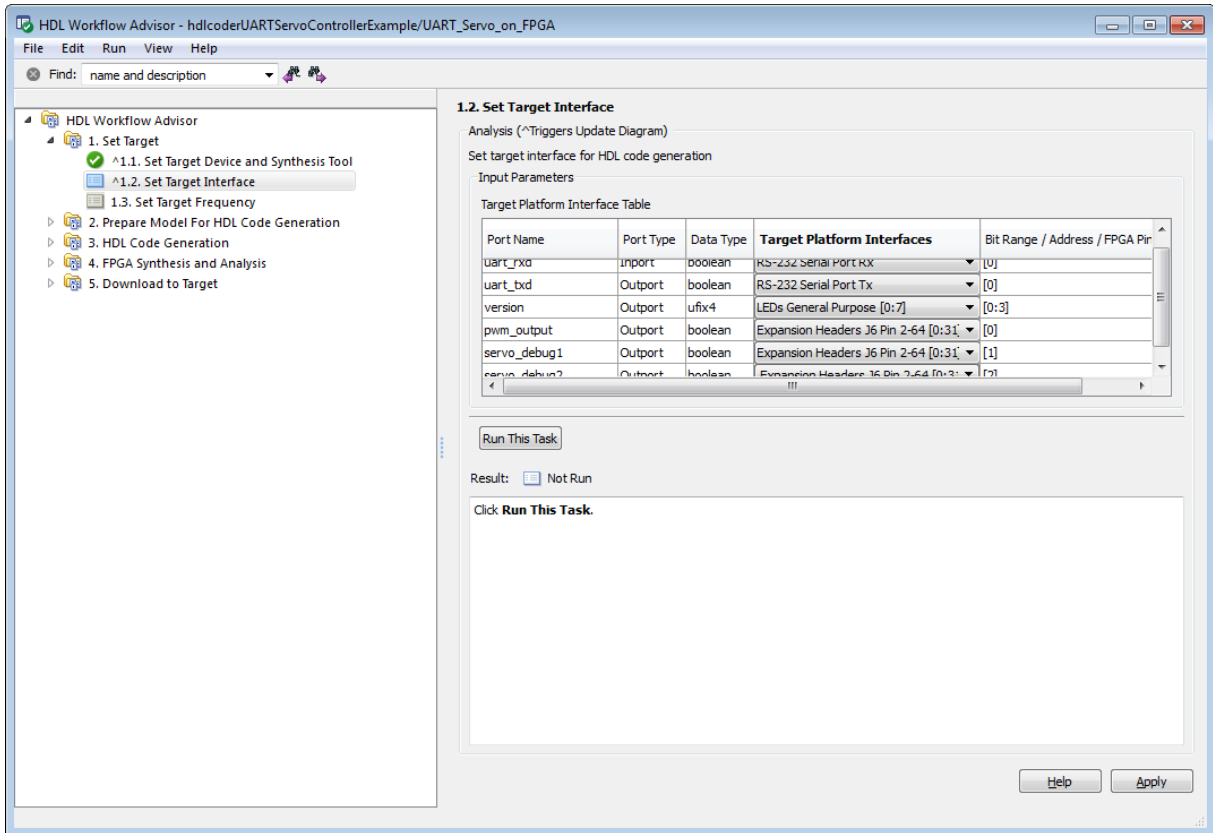
- Expansion Headers J6 Pin 2 64 [0:31]

Each port is allocated to a specified bit position [b] or range of bit positions [lsb:msb]. The width of the specification, in bits, must equal the width of the port on the DUT.

When you select any of these options, the HDL Workflow Advisor automatically allocates a bit range. Double-click in the **Bit Range / Address / FPGA Pin** column to edit the value.

- 3 When you have finished allocating ports, click **Apply**.

The following figure shows the Target Platform Interface Table in a typical configuration.




---

**Note** You must allocate at least one output port must to the target device. If you do not allocate any ports, the **Set Target Interface** task displays an error and terminates.

---

**4** Click **Run This Task**.

**5** In the **Set Target Frequency** task, set your FPGA clock frequency and click **Run This Task**. In this example, the target frequency must be set to 100MHz (the default) due to the fixed UART baud rate.

## Code Generation, Synthesis, and Programming of Target Device

After selecting the target device and configuring its port interface, you can enable the HDL Workflow Advisor to perform the next sequence of tasks automatically. These tasks include:

- **Prepare Model For HDL Code Generation:** Checking the model for HDL code generation compatibility.
- **HDL Code Generation:** Setting HDL-related options of the Model Configuration Parameters dialog box and generating HDL code.
- **FPGA Synthesis and Analysis:** Executing synthesis and timing analysis in Xilinx ISE. Back-annotating the model with critical path information obtained during synthesis.
- **Download to Target** has two subtasks:
  - **Generate Programming File:** Generating an FPGA programming file.
  - **Program Target Device:** Downloading the programming file to the Xilinx Virtex-5 ML506 development board.

---

**Tip** Before executing the **Program Target Device** task, make sure that your host PC is properly connected to the Xilinx Virtex-5 ML506 development board via a JTAG programming cable.

---

To run this sequence of tasks automatically:

- 1** Open the **Download to Target** task group.
- 2** Right-click **Program Target device** and select **Run to Selected Task**.

The task sequence concludes by programming your target board with the generated programming file. You can then read the code generation and synthesis log files.

# FPGA Board Customization

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- “What Is FPGA Board Customization?” on page 20-2
- “Create Custom FPGA Board Definition” on page 20-7
- “Add Xilinx KC705 Evaluation Board for FIL Simulation” on page 20-8
- “FPGA Board Manager Reference” on page 20-22
- “New FPGA Board Wizard Reference” on page 20-25
- “FPGA Board Editor Reference” on page 20-36

## What Is FPGA Board Customization?

In this section...
“Feature Description” on page 20-2
“Custom Board Management” on page 20-2
“FPGA Board Requirements” on page 20-3

### Feature Description

Both HDL Coder and HDL Verifier software include a set of predefined FPGA boards you can use with the Turnkey or FPGA-in-the-Loop (FIL) workflows (you can view the lists of these supported boards in the HDL Workflow Advisor or in the FIL Wizard). With the FPGA Board Manager, you can add additional boards to use either of these workflows. All you need to add a board is the relevant information from the board specification documentation.

The FPGA Board Manager is the hub for accessing wizards and dialog boxes that take you through the steps necessary to create a custom board configuration. You can also access options to import a custom board, remove a board, make a copy of a board for further modification, and verify a new board.

### Custom Board Management

You manage FPGA custom boards through the following user interfaces:

- “FPGA Board Manager Reference” on page 20-22: portal to adding, importing, deleting, and otherwise managing board definition files.
- “New FPGA Board Wizard Reference” on page 20-25: This wizard guides you through creating a custom board definition file with information you obtain from the board specification documentation.
- “FPGA Board Editor Reference” on page 20-36: user interface for viewing or editing board information.

To begin, review the “FPGA Board Requirements” on page 20-3 and then follow the steps described in “Create Custom FPGA Board Definition” on page 20-7.



## FPGA Board Requirements

- “FPGA Device” on page 20-3
- “FPGA Design Software” on page 20-4
- “General Hardware Requirements” on page 20-4
- “Hardware Requirements for FPGA-in-the-Loop” on page 20-4

### FPGA Device

The following table lists the FPGA device families supported in the FPGA-in-the-Loop (FIL) and FPGA Turnkey workflows.

FPGA Device Family	FPGA-in-the-Loop	FPGA Turnkey
Altera Cyclone III	Yes	Yes
Altera Cyclone IV GX	Yes	Yes
Altera Cyclone IV E	Yes	Yes
Altera Arria II	Yes	Yes
Altera Stratix IV	Yes	Yes
Xilinx Kintex-7	Yes	Yes
Xilinx Spartan-3A DSP	No	Yes
Xilinx Spartan3E	No	Yes
Xilinx Spartan6	Yes*	Yes
Xilinx Virtex4	Yes	Yes
Xilinx Virtex5	Yes	Yes
Xilinx Virtex6	Yes	Yes

\*Ethernet PHY RGMII interface is not supported for Xilinx Spartan6 family when used with FPGA-in-the-Loop.

For FPGA development boards that have more than one FPGA devices, only one such device can be used with FIL or FPGA Turnkey.

## FPGA Design Software

Altera Quartus II or Xilinx ISE is required. See product documentation for HDL Coder or HDL Verifier for the specific software versions required.

The following MathWorks tools are required to use FIL or FPGA Turnkey.

Workflow	Required Tools
FPGA-in-the-Loop	<ul style="list-style-type: none"> <li>• HDL Verifier</li> <li>• Fixed-Point Toolbox</li> </ul>
FPGA Turnkey	<ul style="list-style-type: none"> <li>• HDL Coder</li> <li>• Simulink</li> <li>• Simulink Fixed Point™</li> </ul>

## General Hardware Requirements

To use a FPGA development board, make sure that you have the following FPGA resources:

- **Clock:** An external clock connected to the FPGA is required. The clock can be differential or single-ended. The accepted clock frequency is from 5 MHz to 300 MHz. When used with FIL, there are additional requirements to the clock frequency (see “Hardware Requirements for FPGA-in-the-Loop” on page 20-4).
- **Reset:** An external reset signal connected to the FPGA is optional. When supplied, this signal functions as the global reset to the FPGA design.
- **JTAG download cable:** A JTAG download cable that connects host PC and FPGA board is required for the FPGA programming. The FPGA must be programmable using Xilinx iMPACT or Altera Quartus Programmer.

## Hardware Requirements for FPGA-in-the-Loop

An Ethernet connection between the FPGA board and its host PC is required for FIL. On the FPGA board, the Ethernet MAC is implemented in FPGA. An Ethernet PHY chip is required to be on the FPGA board to connect the physical medium to the Media Access (MAC) layer in the FPGA.

**Supported Ethernet PHY Device.** The FIL feature is tested with the following Ethernet PHY chips and may not work with other Ethernet PHY devices.

Ethernet PHY Chip	Test
Marvell® Alaska 88E1111	For GMII, RGMII, and 100 Base-T MII interfaces
National Semiconductor DP83848C	For 100 Base-T MII interface only

**Ethernet PHY Interface.** The Ethernet PHY chip must be connected to the FPGA using one of the following interfaces:

Interface	Note
Gigabit Media Independent Interface (GMII)	Only 1000 Mbits/s speed is supported using this interface.
Reduced Gigabit Media Independent Interface (RGMII)	Only 1000 Mbits/s speed is supported using this interface.
Media Independent Interface (MII)	Only 100 Mbits/s speed is supported using this interface.

**Note** For GMII, the TXCLK (clock signal for 10/100 Mbits signal) signal is not required because only 1000 Mbits/s speed is supported.

In addition to the standard GMII/RGMII/MII interface signals, FPGA-in-the-Loop also requires an Ethernet PHY chip reset signal (ETH\_RESET\_n). This low-active reset signal performs the PHY hardware reset by FPGA. It is active-low.

#### **Special Clock Frequency Requirement for GMII/RGMII Interface.**

When GMII/RGMII interfaces are used, an exact 125MHz clock is required by FPGA to drive the 1000 Mbits/s communication. This clock is derived from the user supplied external clock using the clock module or PLL.

Not all external clock frequencies can derive an exact 125 MHz clock frequency. The acceptable clock frequencies vary depending on the FPGA

device family. The recommended clock frequencies are 50, 100, 125, and 200 MHz.

**Special Timing considerations for RGMII.** When the RGMII interface is used, the MAC on the FPGA assumes that the data are aligned with the edges of reference clock as specified in the original RGMII v1.3 standard. In this case, PC board designs provide additional trace delay for clock signals (RGMII v1.3).

The RGMII v2.0 standard allows the transmitter to integrate this delay so that PC board delay is not required. Marvell Alaska 88E1111 has internal registers to add internal delays to RX and TX clocks. The internal delays are not added by default. This means you use the MDIO module to configure Marvell 88E1111 to add internal delays. (See “FIL I/O” on page 20-30 for the usage of the MDIO module.)

## Create Custom FPGA Board Definition

- 1 Be ready with the following:
  - a Board specification document. Any format you are comfortable with is fine, but if you have it in an electronic version, you can search for the information as it is required.
  - b If you plan to validate (test) your board definition file, set up FPGA design software tools:

For validation, you must have Xilinx or Altera on your path. Use the function `hdlsetuptoolpath` to configure the tool for use with MATLAB. For example:

```
>> hdlsetuptoolpath('ToolName', 'Xilinx ISE', 'ToolPath', 'C:\Xilinx\13.4\ISE_DS\ISE\bin\nt64\ise.exe
```

- 2 Open the FPGA Board Manager by typing `fpgaBoardManager` in the MATLAB command window. Alternatively, if you are using the HDL Workflow Advisor, you can click **Launch Board Manager** at Step 1.1.
- 3 Open the New FPGA Board Wizard by clicking **Create New Board**. For a description of all the tasks you can perform with the FPGA Board Manager, see “FPGA Board Manager Reference” on page 20-22.
- 4 The wizard guides you through entering all board information. At each page, fill in the required fields. For assistance in entering board information, see “New FPGA Board Wizard Reference” on page 20-25.
- 5 Save the board definition file. This is the last step and is automatically instigated when you click **Finish** in the New FPGA Board Wizard. See “Save Board Definition File” on page 20-17.

Your custom board definition now appears in the list of available FPGA Boards in the FPGA Board Manager. If you are using HDL Workflow Advisor, it also shows in the **Target platform** list.

Follow the example “Add Xilinx KC705 Evaluation Board for FIL Simulation” on page 20-8 for a demonstration of adding a custom FPGA board with the New FPGA Board Manager.

## Add Xilinx KC705 Evaluation Board for FIL Simulation

### In this section...

“Overview” on page 20-8

“What You Need to Know Before Starting” on page 20-8

“Start New FPGA Board Wizard” on page 20-9

“Provide Basic Board Information” on page 20-10

“Specify FPGA Interface Information” on page 20-11

“Enter FPGA Pin Numbers” on page 20-13

“Run Optional Validation Tests” on page 20-15

“Save Board Definition File” on page 20-17

“Use New FPGA Board” on page 20-18

### Overview

For FPGA-in-the-Loop, you can use your own qualified FPGA board even if is not in the pre-registered FPGA board list supplied by MathWorks. Using the New FPGA Board Wizard, you can create a board definition file that describes your custom FPGA board.

In this example, you can follow the workflow of creating a board definition file for the Xilinx KC705 evaluation board to use with FIL simulation.

### What You Need to Know Before Starting

- You need to know the following types of information about the board:
  - FPGA interface to the Ethernet PHY chip
  - Clock pins names and numbers
  - Reset pins names and numbers

In this example, the above information is supplied to you in this section. In general, you can find this type of information in the board specification

file. This examples uses the KC705 Evaluation Board for the Kintex-7 FPGA User Guide, published by Xilinx.

- For validation, you must have Xilinx or Altera on your path. Use the function `hdlsetuptoolpath` to configure the tool for use with MATLAB. For example:

```
>> hdlsetuptoolpath('ToolName', 'Xilinx ISE', 'ToolPath', 'C:\Xilinx\13.4\ISE_DS\ISE\bin\nt64\ise.exe');
```

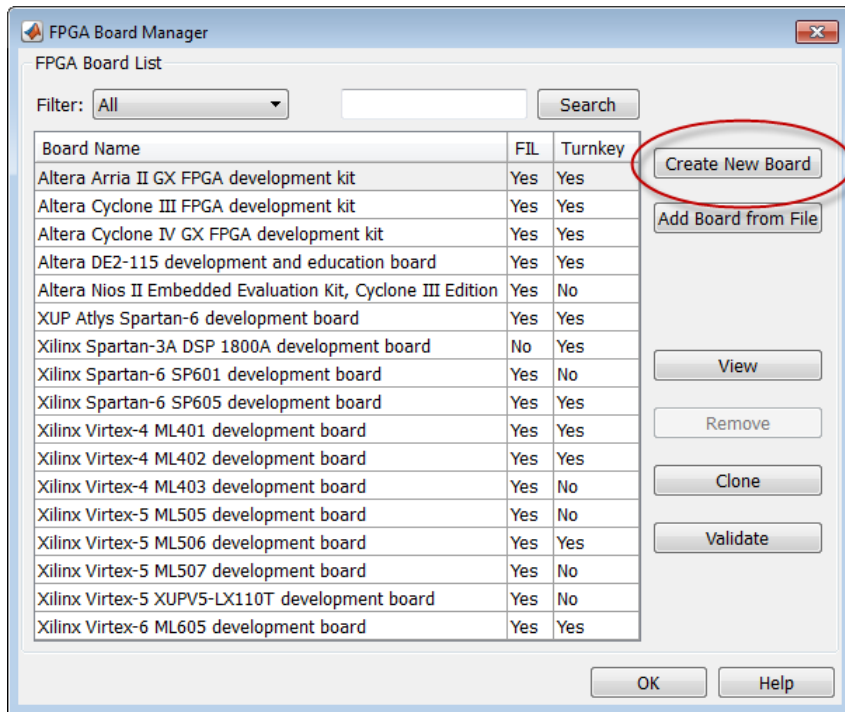
- If you want to verify programming the FPGA board after you add its definition file, you will need to have the custom board attached to your computer. However, having the board connected is not necessary for creating the board definition file.

## Start New FPGA Board Wizard

- 1 Start the FPGA Board Manager by entering the following command at the MATLAB prompt:

```
>>fpgaBoardManager
```

- 2 Click **Create New Board** to open the New FPGA Board Wizard.

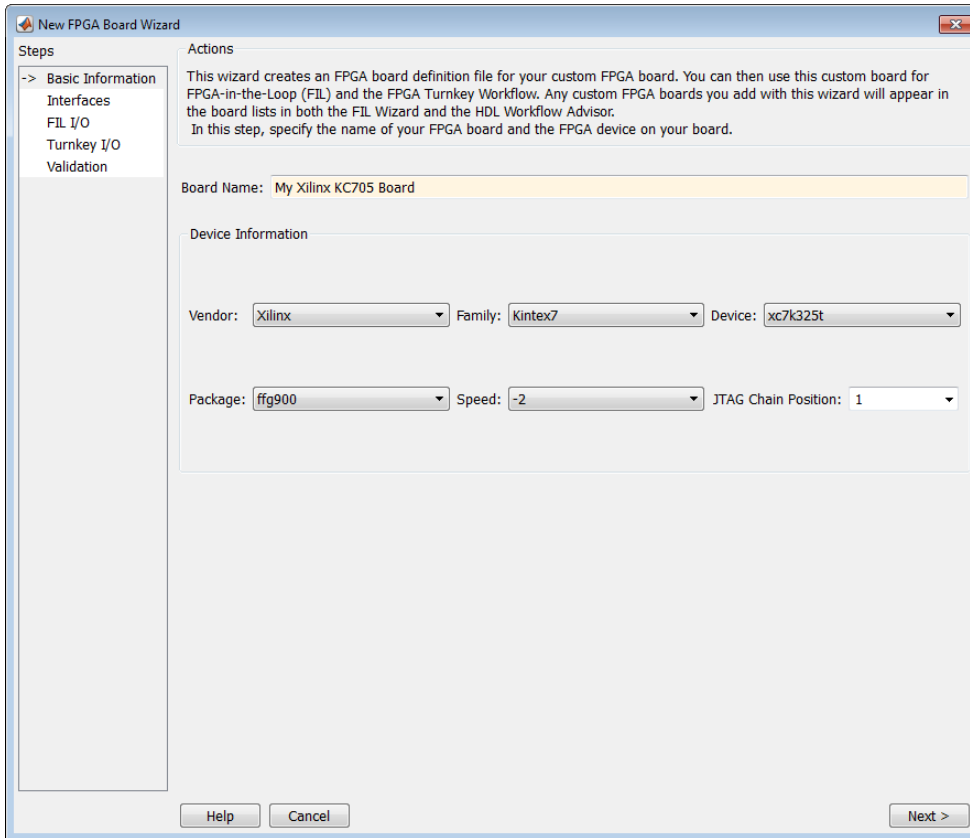


## Provide Basic Board Information

- In the Basic Information pane, enter the following information:
  - Board Name:** Enter "My Xilinx KC705 Board"
  - Vendor:** Select Xilinx
  - Family:** Select Kintex7
  - Device:** Select xc7k325t
  - Package:** Select ffg900
  - Speed:** Select -2
  - JTAG Chain Position:** Select 1

The wizard should now look like the following image.





The information you just entered can be found in the KC705 Evaluation Board for the Kintex-7 FPGA User Guide.

**2** Click **Next**.

## Specify FPGA Interface Information

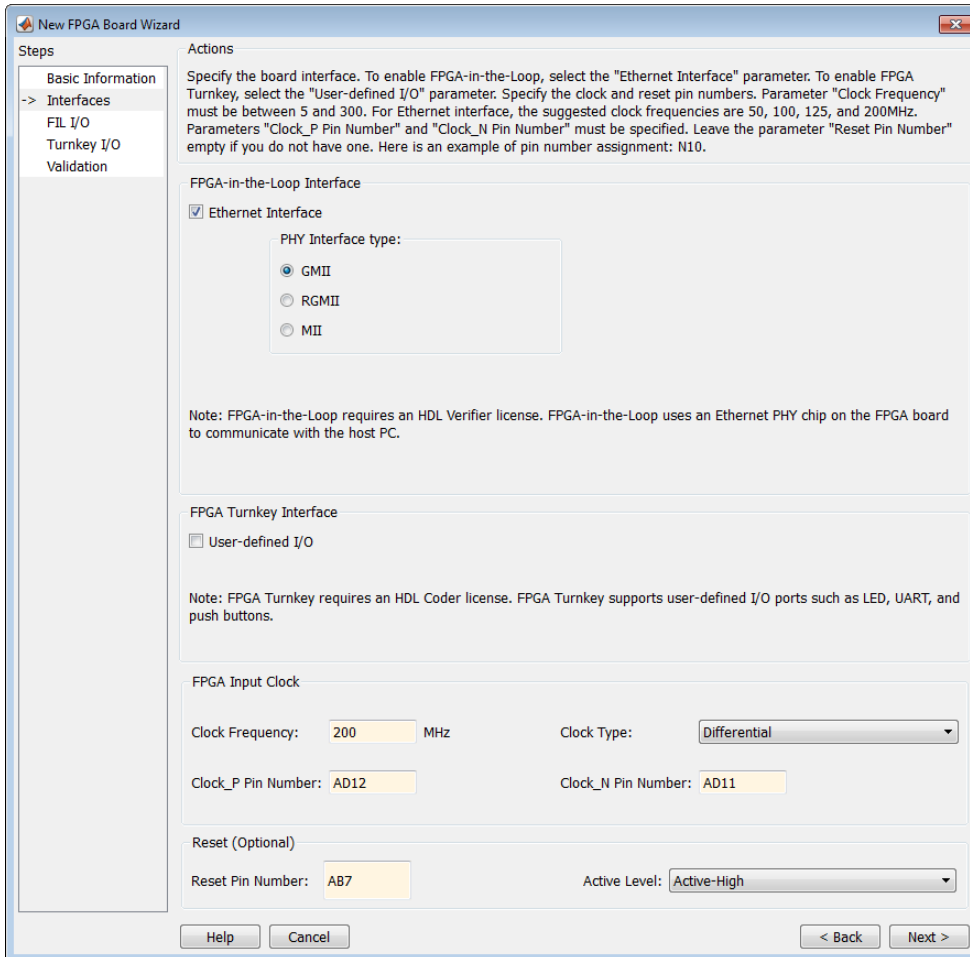
**1** In the **Interfaces** pane, perform the following tasks.

- a** Check the **Ethernet Interface** option in the **FPGA-in-the-Loop Interface** section. This option is required for using your board with **FPGA-in-the-Loop**.

- b** Select **GMII** in the PHY Interface Type. This option indicates that the onboard FPGA is connected to the Ethernet PHY chip via a GMII interface.
- c** Leave the **User-defined I/O** option in the FPGA Turnkey Interface section unchecked. FPGA Turnkey workflow is not the focus of this example.
- d** **Clock Frequency:** Enter 200. Note that this Xilinx KC705 board has multiple clock sources. This 200 MHz clock is one of the recommended clock frequencies for use with Ethernet interface (50, 100, 125, and 200 MHz).
- e** **Clock Type:** Select **Differential**.
- f** **Clock\_P Pin Number:** Enter AD12.
- g** **Clock\_N Pin Number:** Enter AD11.
- h** **Resent Pin Number:** Enter AB7. This will supply a global reset to the FPGA.
- i** **Active Level:** Select **Active-High**.

You can obtain all necessary information from the board design specification.

The wizard should now look like the following image.



**2** Click Next.

## Enter FPGA Pin Numbers

**1** In the FIL/I/O pane, enter the numbers for each FPGA pin. This information is required.

Note that pin numbers for RXD and TXD signals are entered from the least significant digit (LSD) to the most significant digit (MSB), separated by a comma.

For signal name...	Enter FPGA pin number...
ETH_COL	W19
ETH_CRS	R30
ETH_GTXCLK	K30
ETH_MDC	R23
ETH_MDIO	J21
ETH_RESET_n	L20
ETH_RXCLK	U27
ETH_RXD	U30,U25,T25,U28,R19,T27,T26,T28
ETH_RXDV	R28
ETH_RXER	V26
ETH_TXD	N27,N25,M29,L28,J26,K26,L30,J28
ETH_TXEN	M27
ETH_TXER	N29

**2** Click Advanced Options to expand the section.

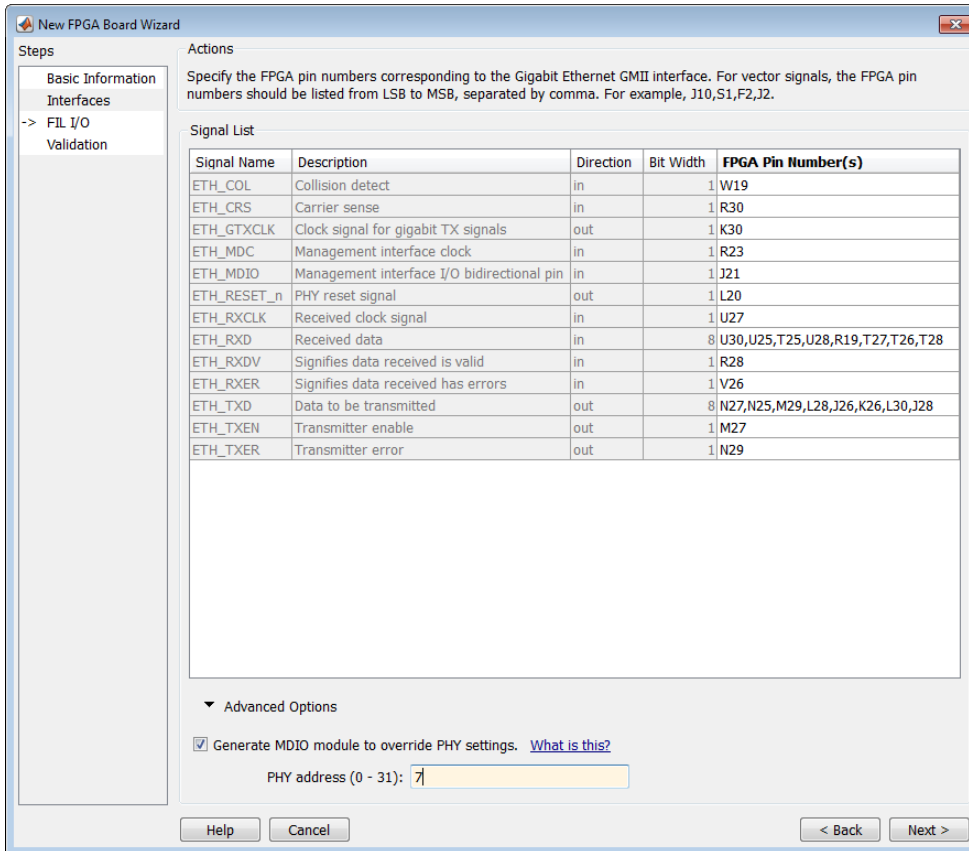
**3** Check the **Generate MDIO module to override PHY settings** option.

This option is selected for the following reasons:

- There are jumpers on the Xilinx KC705 board that configure the Ethernet PHY device to MII, GMII, RGMII, or SGMII mode. Since this example uses the GMII interfaces, the FPGA board will not work if the PHY device are set to the wrong mode. When the **Generate MDIO module to override PHY settings** option is selected, the FPGA uses the Management Data Input/Output (MDIO) bus to override the jumper settings and configure the PHY chip to the correct GMII mode.
- This option currently only applies to Marvell Alaska PHY device 88E1111 and this KC705 board is using the Marvel device.

**4 PHY address (0 – 31):** Enter 7.

The wizard should now look like the following image.

**5 Click Next.****Run Optional Validation Tests**

This step provides a validation test for you to verify if the entered information is correct by performing FPGA-in-the-Loop cosimulation. You will need Xilinx ISE 13.4 or higher versions installed on the same computer. This step is optional and you may skip it if you prefer.

---

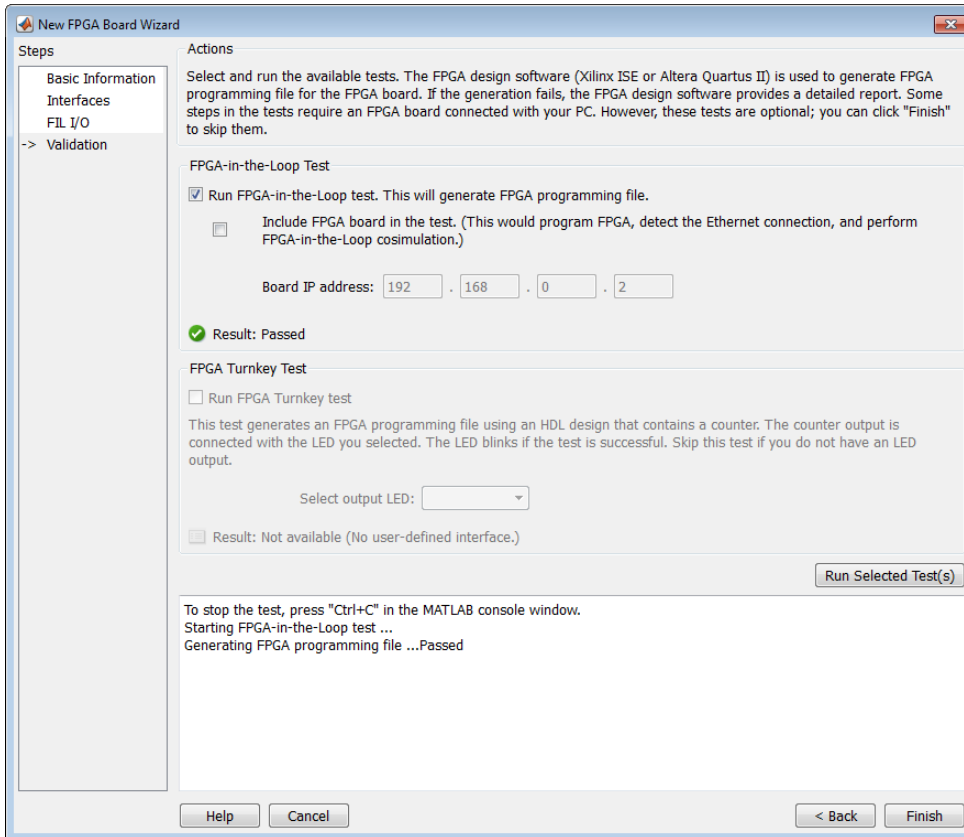
**Note** For validation, you must have Xilinx or Altera on your path. Use the function `hdlsetuptoolpath` to configure the tool for use with MATLAB. For example:

```
>> hdlsetuptoolpath('ToolName', 'Xilinx ISE', 'ToolPath', 'C:\Xilinx\13.4\ISE_DS\ISE\bin\nt64\ise.exe');
```

---

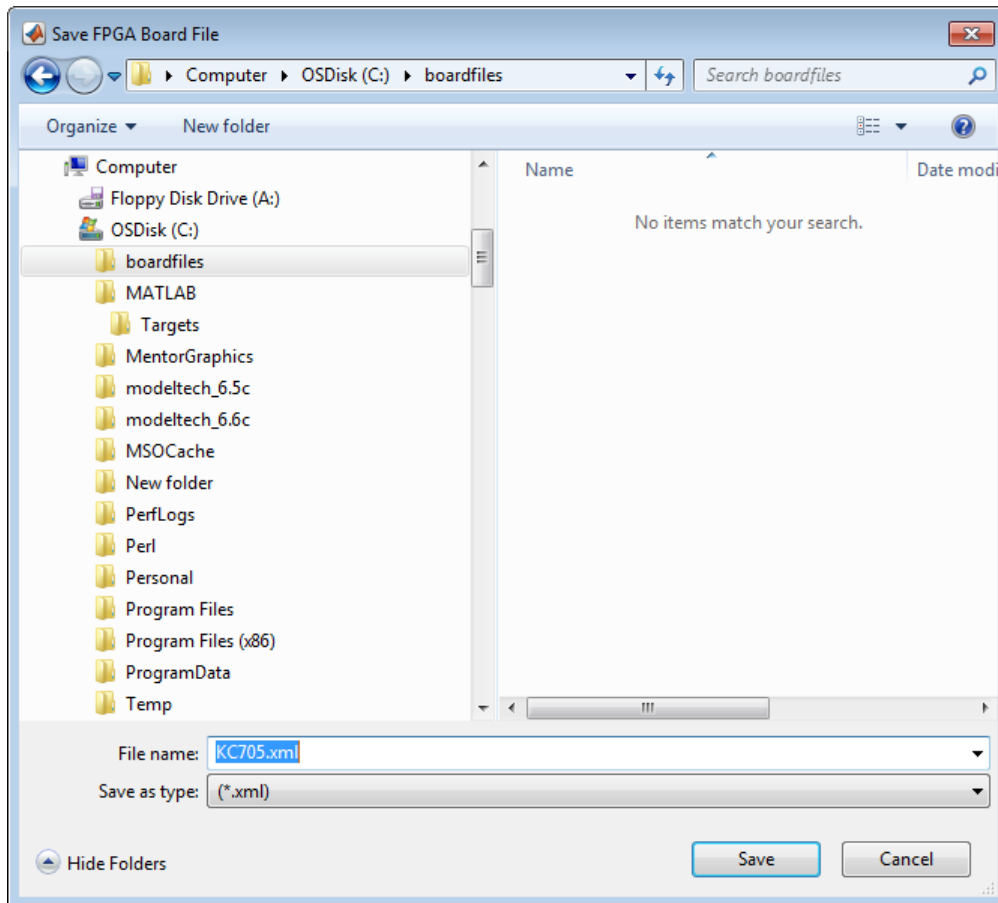
To run this test, perform the following actions.

- 1** Check the **Run FPGA-in-the-Loop test** option.
- 2** If you have the board attached, check the **Include FPGA board in the test** option. You will need to supply the IP address of the FPGA Board. This example assumes the Xilinx KC705 board is attached to your host computer and it has an IP address of 192.168.0.2.
- 3** Click **Run Selected Test(s)**. The tests will take about 10 minutes to complete.



## Save Board Definition File

- 1 Click **Finish** to exit the New FPGA Board Wizard. A **Save As** dialog pops up and asks for the location of the FPGA board definition file. For this example, save as `C:\boardfiles\KC705.xml`.

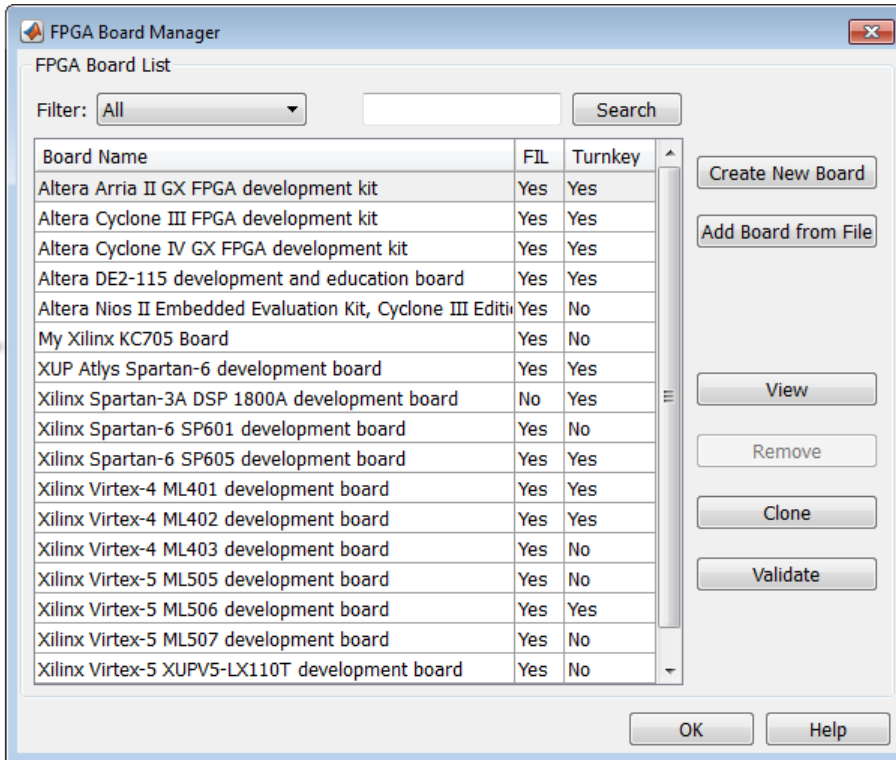


**2** Click **Save** to save the file and exit.

## Use New FPGA Board

**1** After you save the board definition file, you are returned to the FPGA Board Manager. In the FPGA Board List you can now see the new board you just defined.



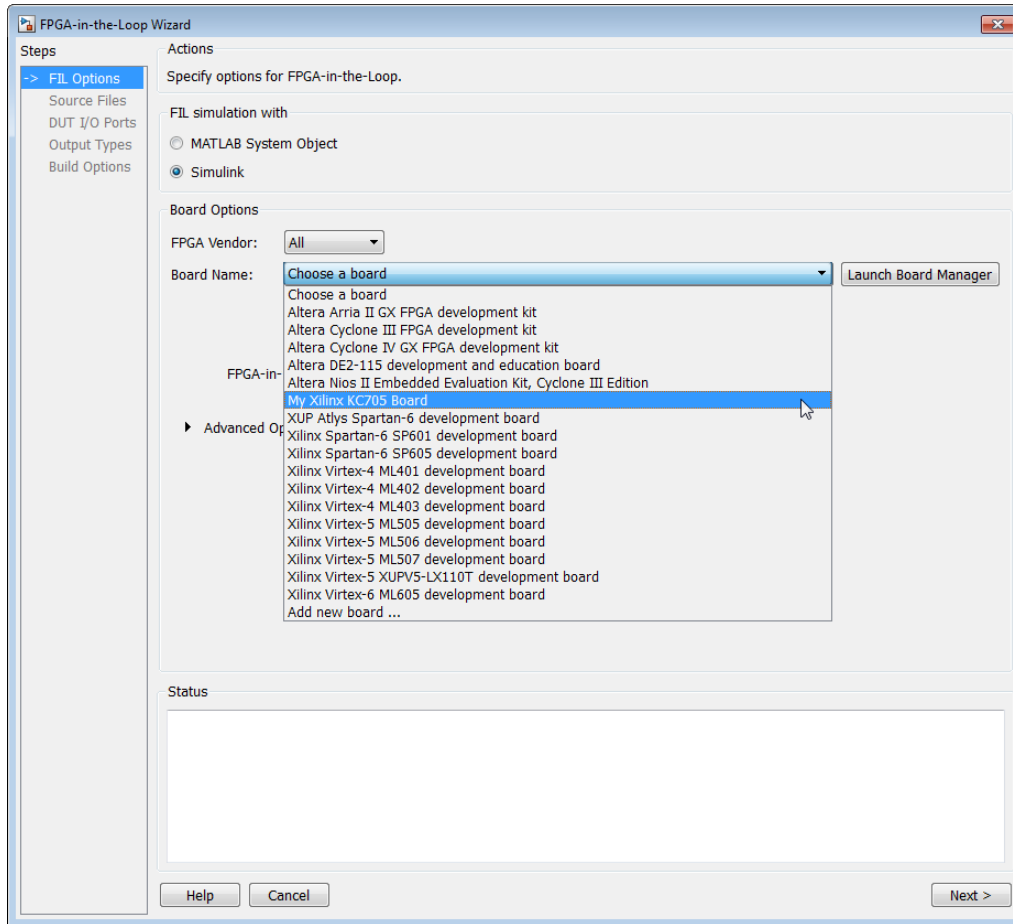


Click **OK** to close the FPGA Board Manager.

- 2 You can view the new board in the board list from either the FIL Wizard or the HDL Workflow Advisor.
  - a Start the FIL Wizard from the MATLAB prompt.

```
>>filWizard
```

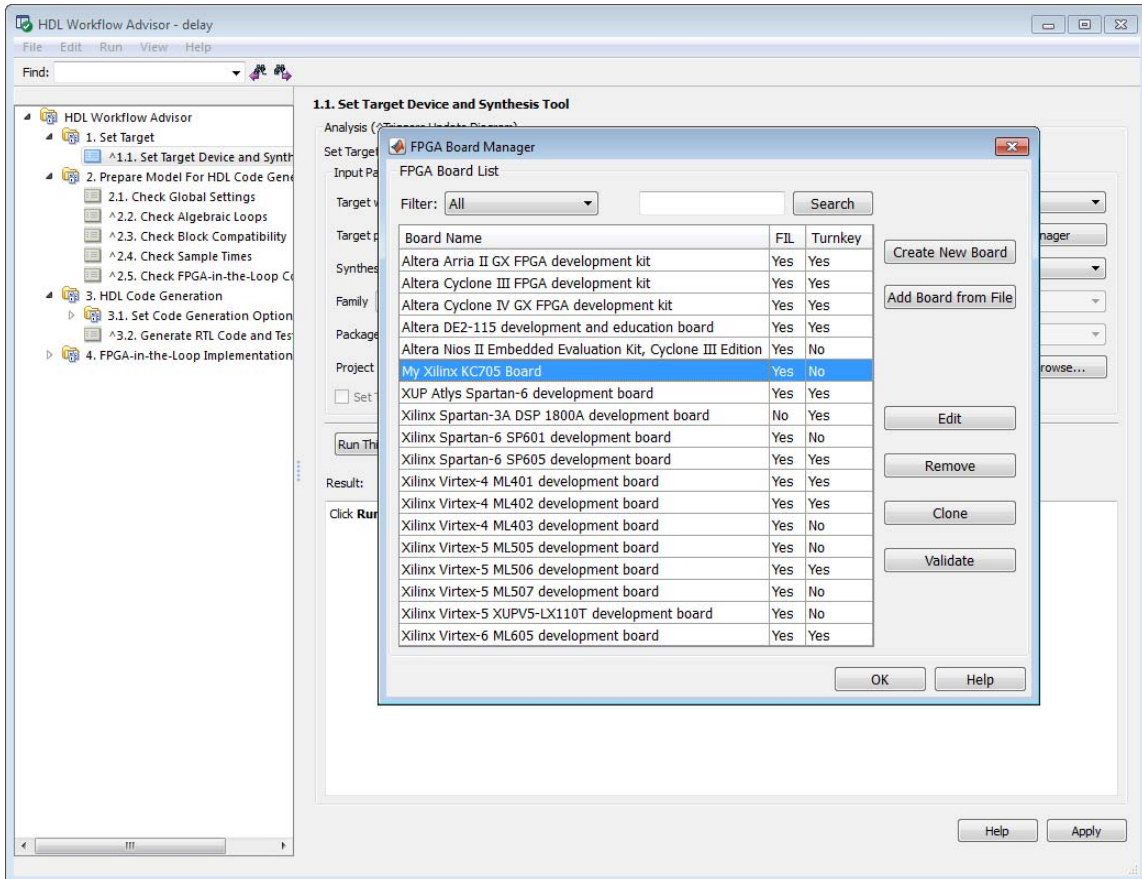
The Xilinx KC705 board appears in the board list and you can select it for FPGA-in-the-Loop simulation.



**b** Start HDL Workflow Advisor.

In step 1.1, select FPGA-in-the-Loop and click **Launch Board Manager**.

The Xilinx KC705 board appears in the board list and you can select it for FPGA-in-the-Loop simulation.



This concludes the example of adding a custom board definition file.

## FPGA Board Manager Reference

### In this section...

“Introduction” on page 20-22

“Filter” on page 20-23

“Search” on page 20-23

“Create New Board” on page 20-24

“Add Board From File” on page 20-24

“View/Edit” on page 20-24

“Remove” on page 20-24

“Clone” on page 20-24

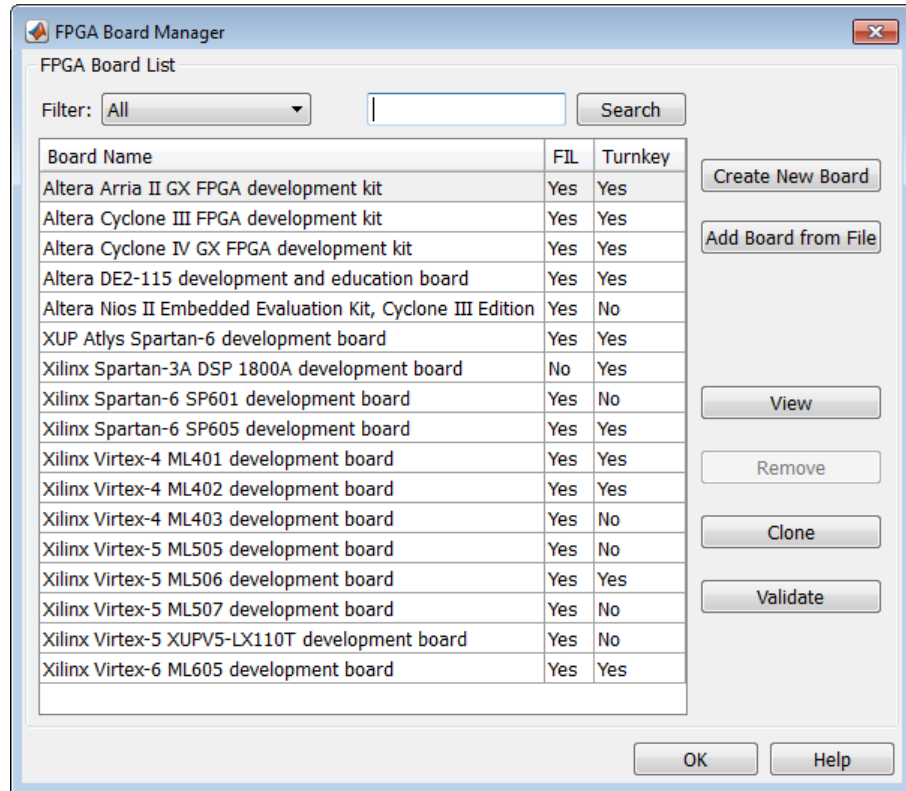
“Validate” on page 20-24

### Introduction

The FPGA Board Manager is the portal to managing custom FPGA boards. You can create a new board definition file or edit an existing one. You can even import a custom board from an existing board definition file.

You start the FPGA Board Manager by one of the following methods:

- By typing `fpgaBoardManager` in the MATLAB command window
- From the FIL Wizard by clicking **Launch Board Manager** on the first page
- From the HDL Workflow Advisor (when using HDL Coder) at Step 1.1



## Filter

Choose one of the following views:

- All boards
- Only those that were preinstalled with HDL Verifier or HDL Coder
- Only custom boards

## Search

Find a specific board in the list or those boards that fully or partially match your search string.

## **Create New Board**

Start New FPGA Board Wizard. See “New FPGA Board Wizard Reference” on page 20-25. You can find the process for creating a new board definition file in “Create Custom FPGA Board Definition” on page 20-7.

## **Add Board From File**

Import a board definition file (.xml).

## **View/Edit**

View board configurations and modify the information. You may view a read-only file but not edit it. See “FPGA Board Editor Reference” on page 20-36.

## **Remove**

Remove custom board from the list. This action does not delete the board definition XML file.

## **Clone**

Makes a copy of an existing custom board for further modification.

## **Validate**

Runs the validation tests for FIL See “Run Optional Validation Tests” on page 20-15.

## New FPGA Board Wizard Reference

Using the New FPGA Board Wizard, you can enter all the required information needed to add a board to the FPGA board list. This list applies to both FIL and Turnkey workflows. Review “FPGA Board Requirements” on page 20-3 before adding a new FPGA board to make sure it is compatible with the workflow for which you want to use it.

Several buttons in the New FPGA Board Wizard assist in navigation:

- **Back:** Go to a previous page to review or edit data already entered.
- **Next:** Go to next page when all requirements of current page have been satisfied.
- **Help:** Open Doc Center, and display this topic.
- **Cancel:** Exit New FPGA Board Wizard. You have the option to exit with or without saving the information from your session.

---

**Adding Boards Once for Multiple Users** To add new boards globally, follow these instructions. Note that to access a board added globally, all users must be using the same MATLAB installation.

- 1 Create the following folder:

```
matlabroot/toolbox/shared/eda/board/boardfiles
```

- 2 Set the basepath to this folder before starting the wizard:

```
basePath =  
fullfile(matlabroot, 'toolbox', 'shared', 'eda', 'board', 'boardfiles');
```

- 3 Copy the board description XML file to the boardfiles folder.
- 4 After copying the XML file, restart MATLAB. The new board appears in the FPGA board list for either or both the FIL and Turnkey workflows.

All boards under this directory will show-up in the FPGA board list automatically for users with the same MATLAB installation. You do not need to use FPGA Board Manager to add these boards again.

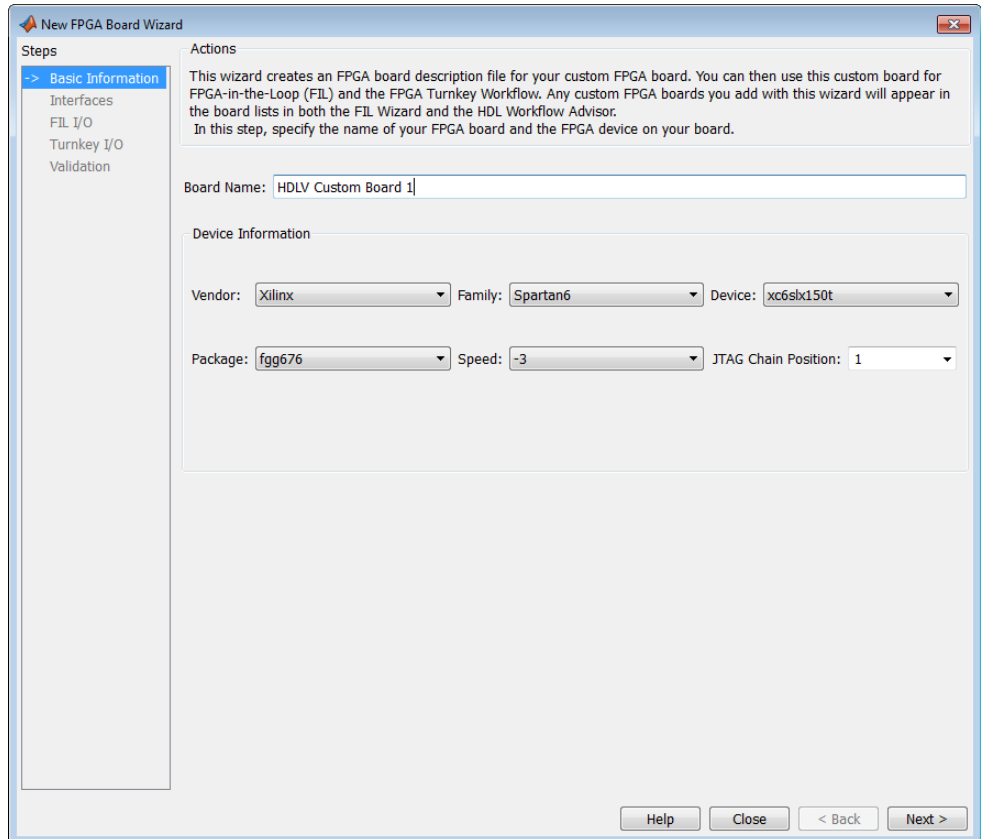
---

The workflow for adding a new FPGA board contains these steps:

<b>In this section...</b>
“Basic Information” on page 20-27
“Interfaces” on page 20-28
“FIL I/O” on page 20-30
“Turnkey I/O” on page 20-32
“Validation” on page 20-35
“Finish” on page 20-35



## Basic Information



The screenshot shows the 'New FPGA Board Wizard' dialog box. The 'Steps' pane on the left lists: Basic Information (selected), Interfaces, FIL I/O, Turnkey I/O, and Validation. The 'Actions' pane contains the following text: 'This wizard creates an FPGA board description file for your custom FPGA board. You can then use this custom board for FPGA-in-the-Loop (FIL) and the FPGA Turnkey Workflow. Any custom FPGA boards you add with this wizard will appear in the board lists in both the FIL Wizard and the HDL Workflow Advisor. In this step, specify the name of your FPGA board and the FPGA device on your board.'

Board Name:

Device Information

Vendor:  Family:  Device:

Package:  Speed:  JTAG Chain Position:

Buttons: Help, Close, < Back, Next >

**Board Name:** Enter a unique board name.

### Device Information:

- **Vendor:** Xilinx or Altera
- **Family:** Family depends on the specified vendor. See the board specification file for applicable settings.
- **Device:** Use the board specification file to select the correct device.
- For Xilinx boards only:

- **Package:** Use the board specification file to select the correct package.
- **Speed:** Use the board specification file to select the correct speed.
- **JTAG Chain Position:** Value indicates the starting position for JTAG chain. Consult the board specification file for this information.

## Interfaces

**New FPGA Board Wizard**

**Steps**

- Basic Information
- > Interfaces
- FIL I/O
- Turnkey I/O
- Validation

**Actions**

Specify the board interface. To enable FPGA-in-the-Loop, select the "Ethernet Interface" parameter. To enable FPGA Turnkey, select the "User-defined I/O" parameter. Specify the clock and reset pin numbers. Parameter "Clock Frequency" must be between 5 and 300. For Ethernet interface, the suggested clock frequencies are 50, 100, 125, and 200MHz. Parameters "Clock\_P Pin Number" and "Clock\_N Pin Number" must be specified. Leave the parameter "Reset Pin Number" empty if you do not have one. Here is an example of pin number assignment: N10.

**FPGA-in-the-Loop Interface**

Ethernet Interface

PHY Interface type:

GMII

RGMII

MII

Note: FPGA-in-the-Loop requires an HDL Verifier license. FPGA-in-the-Loop uses an Ethernet PHY chip on the FPGA board to communicate with the host PC.

**FPGA Turnkey Interface**

User-defined I/O

Note: FPGA Turnkey requires an HDL Coder license. FPGA Turnkey supports user-defined I/O ports such as LED, UART, and push buttons.

**FPGA Input Clock**

Clock Frequency:  MHz      Clock Type:

Clock\_P Pin Number:       Clock\_N Pin Number:

**Reset (Optional)**

Reset Pin Number:       Active Level:

Help    Cancel    < Back    Next >

- **FIL Interface:** If you want to use this board with FIL, check **Ethernet Interface**. Specify the **PHY Interface type** (found in the board specification file).

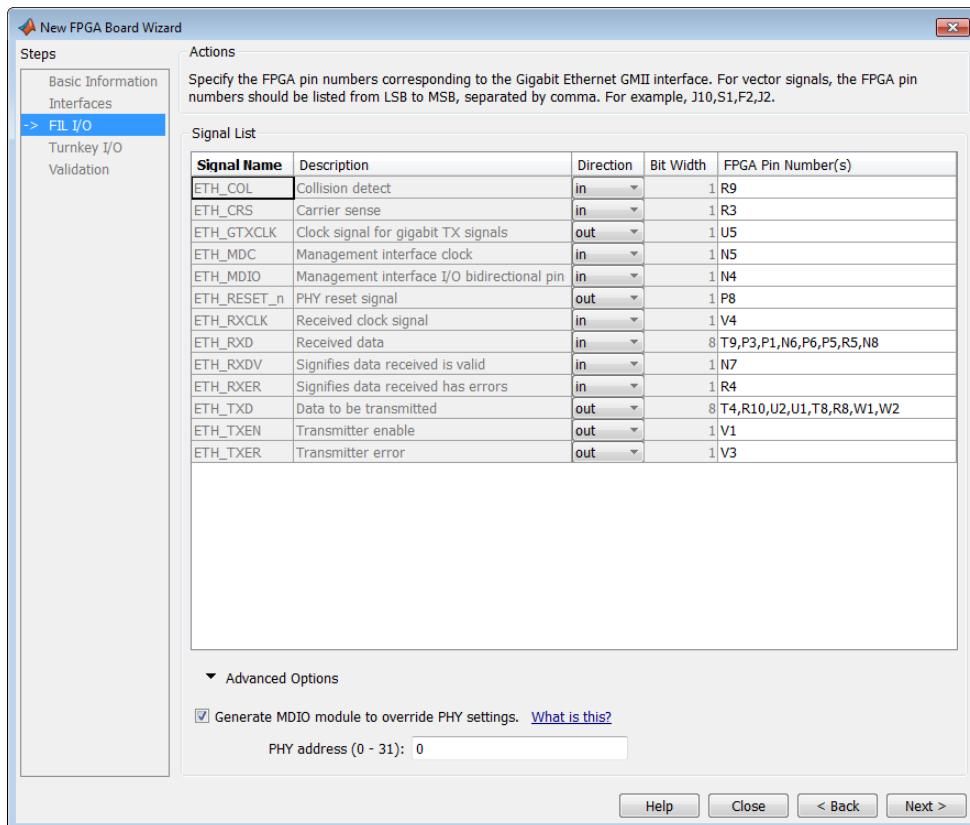
---

**Note** Not all interfaces are available for all boards. Availability depends on the board you selected in Basic Information.

---

- **FPGA Turnkey Interface:** If you want to use with board with the HDL Coder FPGA Turnkey workflow, select **User-defined I/O**.
- **FPGA Input Clock.** Clock details are required for both workflows. You can find all necessary information in the board specification file.
  - **Clock Frequency.** Must be between 5 and 300. For an Ethernet interface, the suggested clock frequencies are 50, 100, 125, and 200 MHz.
  - **Clock Pin Number** . Must be specified. Example: N10.
  - **Clock Type** : Single\_Ended or Differential.
- **Reset (Optional).** If you want to indicate a reset, find the pin number and active level in the board specification file, and enter that information.
  - **Reset Pin Number.** Leave empty if you do not have one.
  - **Active Level** : Active-Low or Active-High.

## FIL I/O



**Signal List:** You must provide all the FPGA pin numbers for the specified signals. You can find this information in the board specification file. For vector signals, list all pin numbers on the same line, separated by commas.

**Generate MDIO module to override PHY settings:** See the next section on FPGA Board Management Data Input/Output Bus (MDIO) to determine when to use this feature. If you do select this option, enter the PHY address.

### What is the Management Data Input/Output Bus (MDIO)?

Management Data Input/Output (MDIO) is a serial bus, defined in the IEEE 802.3 standard, that connects MAC devices and Ethernet PHY devices. The

FPGA MAC uses the MDIO bus to set control registers in the Ethernet PHY device on the board.

Currently only the Marvell 88E1111 PHY chip is supported by this MDIO module implementation. Do not select this checkbox if you are not using Marvell 88E1111.

The generated MDIO module is used to perform the following operations:

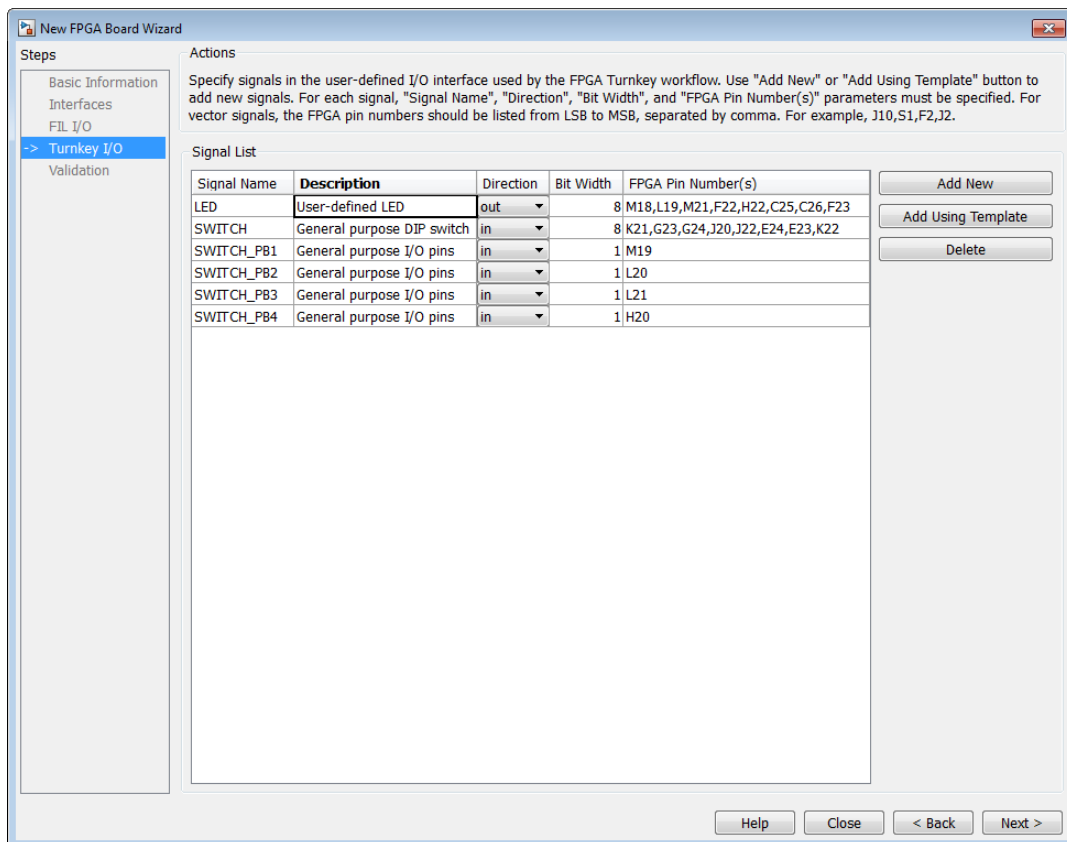
- **GMII mode:** The PHY device can start up using other modes, such as RGMII/SGMII. The generated MDIO module sets the PHY chip in GMII mode.
- **RGMII mode:** The PHY device can start up using other modes, such as GMII/SGMII. The generated MDIO module sets the PHY device in RGMII mode. In addition, the module sets the PHY chip to add internal delay for RX and TX clocks.
- **MII mode:** The generated MDIO module sets the PHY device in GMII compatible mode. The module also sets the autonegotiation register to remove the 1000 Base-T capability advertisement. This reset ensures that the autonegotiation process does not select 1000 Mbits/s speed, which is not supported in MII mode.

**When To Select MDIO:** Select the **Generate MDIO module to override PHY settings** option when both the following conditions are met:

- The onboard Ethernet PHY device is Marvell 88E1111.
- The PHY device startup settings are not compatible with the FPGA MAC. The MDIO modules for different PHY modes must override these settings, as previously described.

**Specifying the PHY Address:** The PHY address is a 5-bit integer. The value is determined by the CONFIG[0] and CONFIG[1] pin on Marvell 88E1111 PHY device. See the board manual for this value.

## Turnkey I/O



You must define at least one output port for the Turnkey I/O interface.

**Signal List:** You must provide all the FPGA pin numbers for the specified signals. You can find this information in the board specification file. For vector signals, list all pin numbers on the same line, separated by commas. The number of pin numbers must match the bit width of the corresponding signal.

**Add New:** You are prompted to enter all entries in the signal list manually.

**Add Using Template:** The wizard prepopulates a new signal entry for UART, LED, GPIO, or DIP Switch signals with the following:

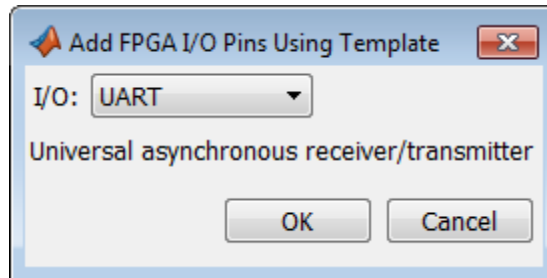
- A generic signal name
- Description
- Direction
- Bit width

You may change the values in any of these prepopulated fields.

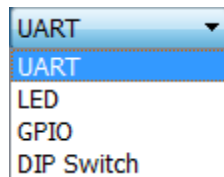
**Delete:** Delete the selected signal from list.

The following example demonstrates using the **Add Using Template** feature.

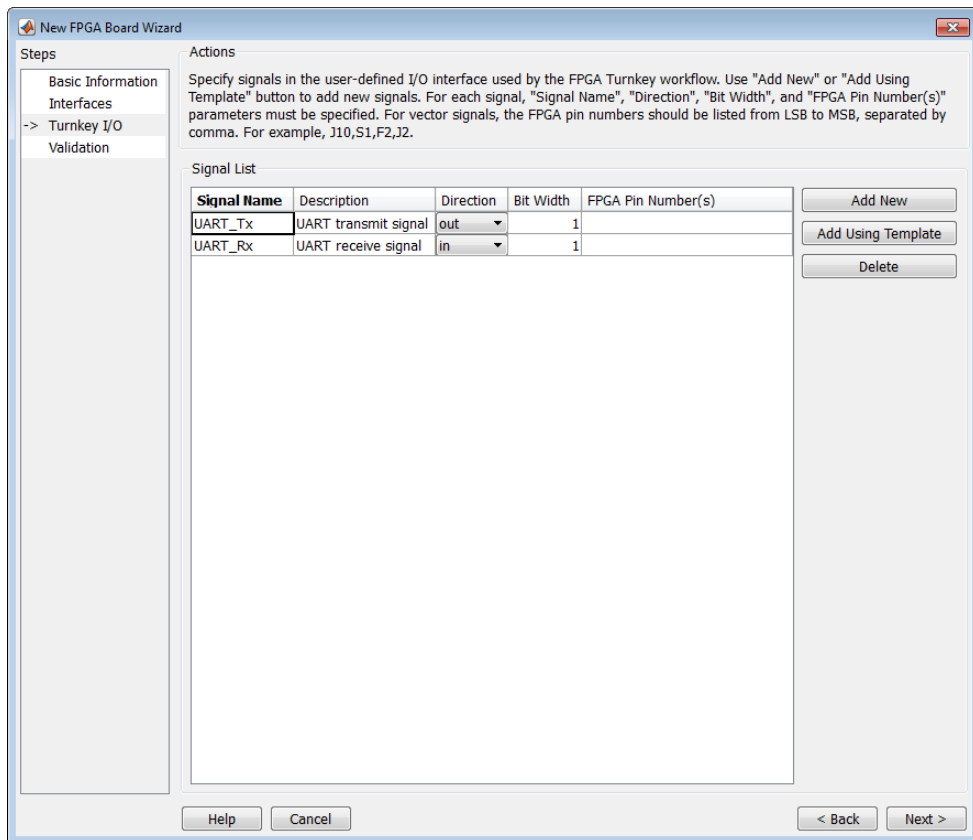
- 1 In the Turnkey I/O dialog, click **Add Using Template**.
- 2 You can now view the template dialog.



- 3 Pull down the I/O list and select from the following options:

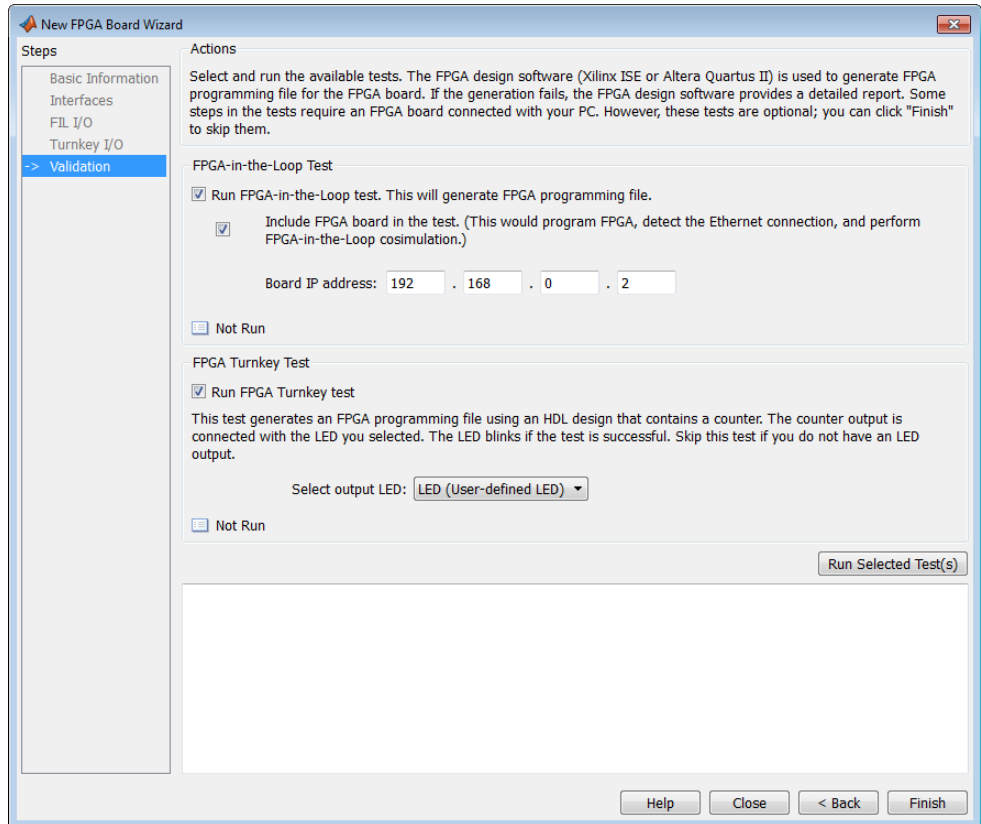


- 4 Click **OK**.
- 5 The wizard adds the specified signal (or signals) to the I/O list.





## Validation



Run the validation test. For FPGA Turnkey testing, you must have a board attached. For FIL testing, the board is optional.

## Finish

When you have completed validation, click **Finish**. See “Save Board Definition File” on page 20-17.

## FPGA Board Editor Reference

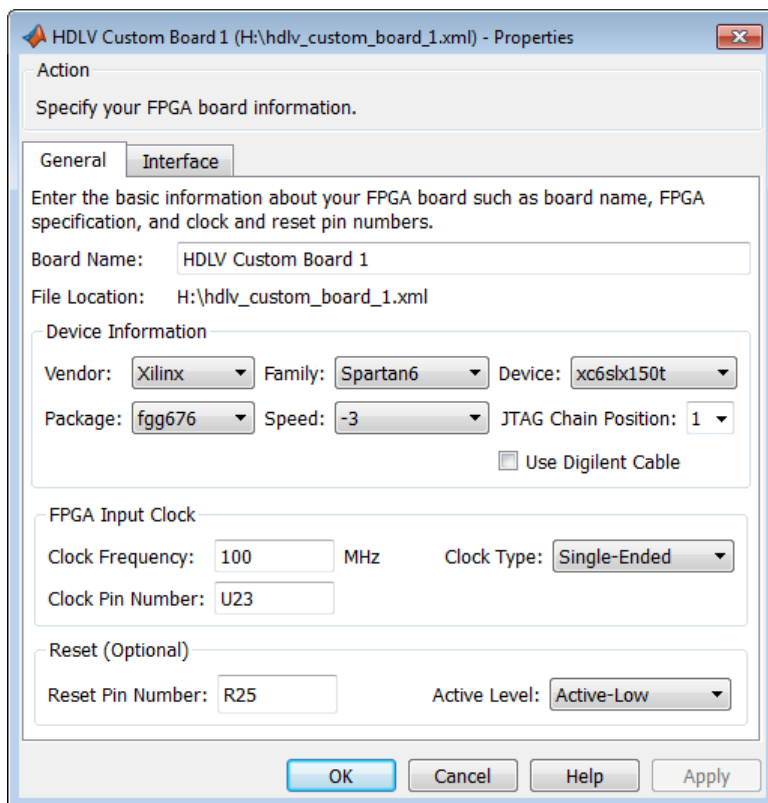
To edit a board definition XML file, you must first make it writeable. If the file is read-only, the FPGA Board Editor only lets you view the board configuration information. You cannot modify that information.

### In this section...

“General” on page 20-36

“Interface” on page 20-38

## General



The screenshot shows the 'HDLV Custom Board 1 (H:\hdlv\_custom\_board\_1.xml) - Properties' dialog box. The 'General' tab is selected. The dialog contains the following fields and options:

- Action:** Specify your FPGA board information.
- General / Interface:** Two tabs, with 'General' selected.
- Enter the basic information about your FPGA board such as board name, FPGA specification, and clock and reset pin numbers.**
- Board Name:** HDLV Custom Board 1
- File Location:** H:\hdlv\_custom\_board\_1.xml
- Device Information:**
  - Vendor:** Xilinx
  - Family:** Spartan6
  - Device:** xc6sbx150t
  - Package:** fgg676
  - Speed:** -3
  - JTAG Chain Position:** 1
  - Use Digilent Cable
- FPGA Input Clock:**
  - Clock Frequency:** 100 MHz
  - Clock Type:** Single-Ended
  - Clock Pin Number:** U23
- Reset (Optional):**
  - Reset Pin Number:** R25
  - Active Level:** Active-Low

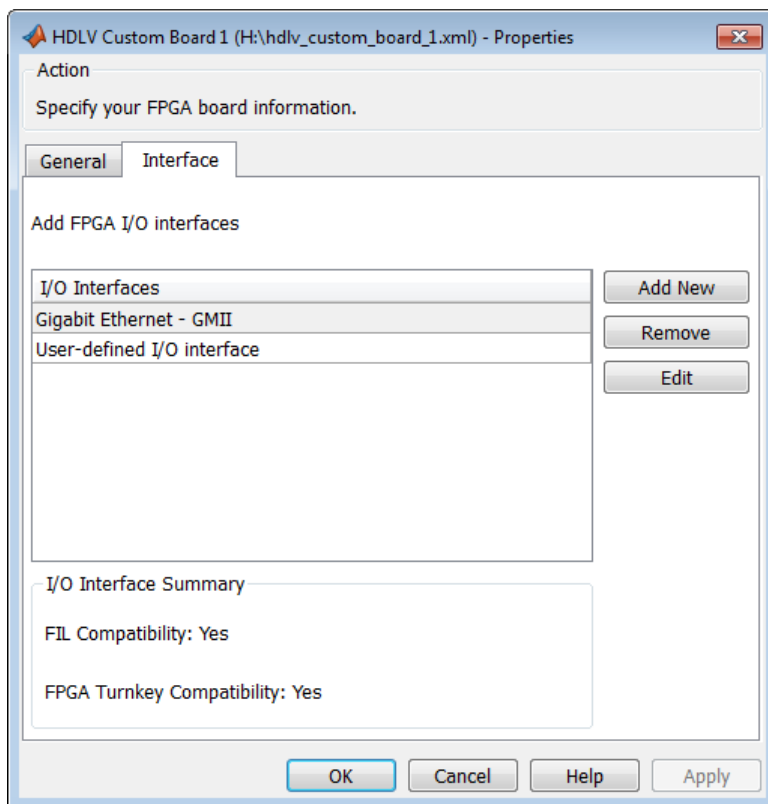
Buttons at the bottom: OK, Cancel, Help, Apply.

**Board Name:** Unique board name

**Device Information:**

- **Vendor:** Xilinx or Altera
- **Family:** Family depends on the specified vendor. See the board specification file for applicable settings.
- **Device:** Device depends on the specified vendor and family. See the board specification file for applicable settings.
- For Xilinx boards only:
  - **Package:** Package depends on specified vendor, family, and device. See the board specification file for applicable settings.
  - **Speed:** Speed depends on package. See the board specification file for applicable settings.
  - **JTAG Chain Position:** Value indicates the starting position for JTAG chain. Consult the board specification file for this information.
- **FPGA Input Clock.** Clock details are required for both the FIL and Turnkey workflows. You can find all necessary information in the board specification file.
  - **Clock Frequency.** Must be between 5 and 300. For an Ethernet interface, the suggested clock frequencies are 50, 100, 125, and 200 MHz.
  - **Clock Pin Number** . Must be specified. Example: N10.
  - **Clock Type** : Single\_Ended or Differential.
- **Reset (Optional).** If you want to indicate a reset, find the pin number and active level in the board specification file, and enter that information.
  - **Reset Pin Number.** Leave empty if you do not have one.
  - **Active Level** : Active-Low or Active-High.

## Interface



The Interface page describes the supported FPGA I/O Interfaces. Select any listed interface and click **View** to see the **Signal List**. If the board definition file has write permission, you can also **Add New** interface or **Remove** an interface.

# HDL Workflow Advisor Tasks

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## HDL Workflow Advisor Tasks

### In this section...

- “HDL Workflow Advisor Tasks Overview” on page 21-3
- “Set Target Overview” on page 21-5
- “Set Target Device and Synthesis Tool” on page 21-6
- “Set Target Library” on page 21-8
- “Set Target Interface” on page 21-9
- “Set Target Frequency” on page 21-10
- “Prepare Model For HDL Code Generation Overview” on page 21-10
- “Check Global Settings” on page 21-12
- “Check Algebraic Loops” on page 21-13
- “Check Block Compatibility” on page 21-14
- “Check Sample Times” on page 21-15
- “Check FPGA-in-the-Loop Compatibility” on page 21-16
- “HDL Code Generation Overview” on page 21-17
- “Set Code Generation Options Overview” on page 21-18
- “Set Basic Options” on page 21-19
- “Set Advanced Options” on page 21-20
- “Set Testbench Options” on page 21-21
- “Generate RTL Code and Testbench” on page 21-22
- “FPGA Synthesis and Analysis Overview” on page 21-24
- “Create Project” on page 21-25
- “Perform Synthesis and P/R Overview” on page 21-26
- “Perform Logic Synthesis” on page 21-27
- “Perform Mapping” on page 21-28
- “Perform Place and Route” on page 21-29
- “Annotate Model with Synthesis Result” on page 21-30

**In this section...**

“Download to Target Overview” on page 21-32

“Generate Programming File” on page 21-33

“Program Target Device” on page 21-34

“Generate xPC Target Interface” on page 21-35

“Save and Restore HDL Workflow Advisor State” on page 21-36

“FPGA-in-the-Loop Implementation” on page 21-36

“Set FIL Options” on page 21-36

“Build FPGA-in-the-Loop” on page 21-36

“Check USRP® Compatibility” on page 21-37

“Generate FPGA Implementation” on page 21-37

## HDL Workflow Advisor Tasks Overview

The HDL Workflow Advisor is a tool that supports a suite of tasks covering the stages of the FPGA design process. Some tasks perform model validation or checking; others run the HDL code generator or third-party tools. Each folder at the top level of the HDL Workflow Advisor contains a group of related tasks that you can select and run:

- **Set Target:** The tasks in this category enable you to select the desired target device and map its I/O interface to the inputs and outputs of your model.

**Prepare Model For HDL Code Generation:** The tasks in this category check your model for HDL code generation compatibility. The tasks also report on model settings, blocks, or other conditions (such as algebraic loops) that would impede code generation, and provide advice on how to fix such problems.

- **HDL Code Generation:** This category supports all HDL-related options of the Model Configuration Parameters dialog, including setting HDL code and test bench generation parameters, and generating code, test bench, or a cosimulation model.
- **FPGA Synthesis and Analysis:** The tasks in this category support:

- Synthesis and timing analysis through integration with third-party synthesis tools
- Back annotation of the model with critical path and other information obtained during synthesis
- **FPGA-in-the-Loop Implementation:** This category implements the phases of FIL, including providing block generation, synthesis, logical mapping, PAR (place-and-route), programming file generation, and a communications channel. These capabilities are specifically designed for a particular board and tailored to your RTL code. An HDL Verifier license is required for FIL.
- **Download to Target:** The tasks in this category depend on the selected target device and might include:
  - Generation of a target-specific FPGA programming file
  - Programming the target device
  - Generation of a model that contains an xPC Target interface subsystem

### See Also

For summary information on each HDL Workflow Advisor folder or task, select the folder or task icon and then click the HDL Workflow Advisor **Help** button.



## Set Target Overview

The tasks in the **Set Target** folder enable you to select a target FPGA device and define the I/O interface to be generated for the device. The **Set Target** folder contains the following tasks:

- **Set Target Device and Synthesis Tool:** Select a target FPGA device and synthesis tools.
- **Set Target Interface:** Use the Target Platform Interface Table to assign each port on your DUT to an I/O resource on the target device.

### See Also

For summary information on each **Set Target** task, select the task icon and then click the HDL Workflow Advisor **Help** button.

## Set Target Device and Synthesis Tool

**Set Target Device and Synthesis Tool** enables you to select an FPGA target device and an associated synthesis tool from a pulldown menu that lists the devices that HDL Workflow Advisor currently supports.

### Description

This task displays the following options:

- **Target Workflow:** A pulldown menu that lists the possible workflows that HDL Workflow Advisor support. Choose from:
  - Generic ASIC/FPGA
  - FPGA-in-the-Loop
  - FPGA Turnkey
  - Customization for the USRP® Device
- **Target platform:** A pulldown menu that lists the devices the HDL Workflow Advisor currently supports. Available for all workflows except Generic ASIC/FPGA.
- **Synthesis tool:** Select a synthesis tool, then select the **Family**, **Device**, **Package**, and **Speed** for your synthesis target. Select a Xilinx or Altera tool to make the **Set Target Library (for floating-point synthesis support)** option available.
- **Project folder:** Specify the project folder name.
- **Set Target Library (for floating-point synthesis support):** Select to map to an FPGA target-specific floating-point library. Enabling this option causes the **Set Target Library** task to appear on the left.

### Dependencies

Setting **Target workflow** to FPGA Turnkey enables the following tasks:

- “Set Target Interface” on page 21-9
- “Set Target Frequency” on page 21-10
- Tasks in the **Download to Target** folder

Selecting **Set Target Library (for floating-point synthesis support)** causes the **Set Target Library** task to appear on the left.

**See Also**

For information on the Set Target Library task, see “Set Target Library” on page 21-8.

## Set Target Library

**Target library:** The selected FPGA floating-point target library.

**Objective:** Choose to optimize your generated HDL code for **Speed** or **Area**.

**Block latencies:** Select the block latencies to use.

**Set Xilinx simulation path:** Select to enter the location of your pre-compiled Xilinx simulation library (`xilinxcorelib`). Do not select this option if you wish the coder to automatically detect the location of the simulation library. This option is available only if you selected a Xilinx synthesis tool in the **Set Target Device and Synthesis Tool** task. If the pre-compiled Xilinx simulation library is unavailable, the coder issues a warning.

**Absolute path:** Enter the location of the simulation library. This option is available if **Set Xilinx simulation path** is selected.

### Dependencies

This task appears when you select **Set Target Library (for floating-point synthesis support)** in the **Set Target Device and Synthesis Tool** task.

The **Set Xilinx simulation path** option is available when you select a Xilinx device in the **Set Target Device and Synthesis Tool** task.

### See Also

For more information on targeting FPGA floating-point library blocks, see “FPGA Target-Specific Floating-Point Library Mapping” on page 19-34.

## Set Target Interface

**Set Target Interface** displays properties of input and output ports on your model, and enables you to map these ports to I/O resources on the target device.

### Description

**Set Target Interface** displays the Target Platform Interface Table, which shows:

- The name, port type (input or output), and data type for each port on your model
- A pulldown menu listing the available I/O resources for the target device

These resources are device-specific. For detailed information on each resource, see the documentation for your FPGA development board.

### Dependency

This task appears when you set **Target workflow** to FPGA Turnkey.

## Set Target Frequency

Automatically generate clock module for FPGA Turnkey targets.

Leave entry unchanged if you wish to use the default value (same as input).

## Dependency

This task appears when you set **Target workflow** to FPGA Turnkey.

## Prepare Model For HDL Code Generation Overview

The tasks in the **Prepare Model For HDL Code Generation** folder check the model for compatibility with HDL code generation. If a check encounters a condition that would raise a code generation warning or error, the right pane of the HDL Workflow Advisor displays information about the condition and how to fix it. The **Prepare Model For HDL Code Generation** folder contains the following checks:

- **Check Global Settings:** Check model parameters for compatibility with HDL code generation.
- **Check Algebraic Loops:** Check the model for algebraic loops.
- **Check Block Compatibility:** Check that blocks in the model support HDL code generation.
- **Check Sample Times:** Check the solver options, tasking mode, and rate transition diagnostic settings, given the model's sample times.
- **Check FPGA-in-the-Loop Compatibility:** Check model compatibility with FPGA-in-the-Loop, specifically:
  - Not allowed: sink/source subsystems, single/double data types, zero sample time
  - Must be present: HDL Verifier license

This option is available only if you select **FPGA-in-the-Loop** for Target workflow.

- **Check USRP Compatibility:** The model must have 2 input ports and 2 output ports of signed 16-bit signals.

This option is available only if you select **Customization** for the **USRP(TM) Device for Target** workflow.

**See Also**

For summary information on each **Prepare Model For HDL Code Generation** task, select the task icon and then click the HDL Workflow Advisor **Help** button.

## Check Global Settings

**Check Global Settings** checks model-wide parameter settings for HDL code generation compatibility.

### Description

This check examines the model parameters for compatibility with HDL code generation and flags conditions that would raise an error or a warning during code generation. The HDL Workflow Advisor displays a table with the following information about each condition detected:

- *Block*: Hyperlink to the model configuration dialog page that contains the error or warning condition
- *Settings*: Name of the model parameter that caused the error or warning condition
- *Current*: Current value of the setting
- *Recommended*: Recommended value of the setting
- *Severity*: Severity level of the warning or error condition. Minimally, you should fix settings that are tagged as error.

### Tip

To set reported settings to their recommended values, click the **Modify All** button. You can then run the check again and proceed to the next check.



## **Check Algebraic Loops**

Detect algebraic loops in the model.

### **Description**

The coder does not support HDL code generation for models in which algebraic loop conditions exist. **Check Algebraic Loops** examines the model and fails the check if it detects an algebraic loop. You should eliminate algebraic loops from your model before proceeding with further HDL Workflow Advisor checks or code generation.

### **See Also**

For information about algebraic loops, see “Algebraic Loops” in the Simulink documentation.

## **Check Block Compatibility**

Check the DUT for unsupported blocks.

### **Description**

**Check Block Compatibility** checks blocks within the DUT for compatibility with HDL code generation. The check fails if it encounters blocks that the coder does not support. The HDL Workflow Advisor reports incompatible blocks, including the full path to each block.

### **See Also**

See “Blocks Supported for HDL Code Generation” on page 9-3 for a complete list of supported blocks and their implementations.

## Check Sample Times

Check the solver, sample times, and tasking mode settings for the model.

### Description

**Check Sample Times** checks the solver options, sample times, tasking mode, and rate transition diagnostics for HDL code generation compatibility. Solver options that the coder requires or recommends are:

- **Type:** Fixed-step. (The coder currently supports variable-step solvers under limited conditions. See `hdlsetup` for details.)
- **Solver:** Discrete (no continuous states). Other fixed-step solvers could be selected, but this option is usually the best one for simulating discrete systems.
- **Tasking mode:** `SingleTasking`. The coder does not currently support models that execute in multitasking mode. Do not set **Tasking mode** to `Auto`.
- **Multitask rate transition** and **Single task rate transition** diagnostic options: set to `Error`.

## **Check FPGA-in-the-Loop Compatibility**

HDL Verifier checks model for compatibility with FPGA-in-the-Loop processing.

### **See Also**

For HDL code and model compatibilities with FPGA-in-the-Loop processing, see “Design Considerations for FPGA-in-the-Loop” on page 19-55.

## HDL Code Generation Overview

The tasks in the **HDL Code Generation** folder enable you to:

- Set and validate HDL code and test bench generation parameters. Most parameters of the **HDL Code** pane of the Model Configuration Parameters dialog box and the Model Explorer are supported.
- Generate any or all of:
  - RTL code
  - RTL test bench
  - Cosimulation model

To run the tasks in the **HDL Code Generation** folder automatically, select the folder and click **Run to Failure**.

---

**Tip** After each task in this folder runs, the coder updates the Configuration Parameters dialog box and the Model Explorer.

---

## **Set Code Generation Options Overview**

The tasks in the **Set Code Generation Options** folder enable you to set and validate HDL code and test bench generation parameters. Each task of the **Set Code Generation Options** folder supports options of the **HDL Code** pane of the Model Configuration Parameters dialog box and the Model Explorer. The tasks are:

- **Set Basic Options:** Set parameters that affect overall code generation. See “HDL Code Generation Pane: General” on page 7-8 for information on each parameter.
- **Set Advanced Options:** Set parameters that specify detailed characteristics of the generated code, such as HDL element naming and whether certain optimizations apply. See “HDL Code Generation Pane: Global Settings” on page 7-21 for information on each parameter.
- **Set Testbench Options:** Set options that determine characteristics of generated test bench code. See “HDL Code Generation Pane: Test Bench” on page 7-72 for information on each parameter.

To run the tasks in the **Set Code Generation Options** folder automatically, select the folder and click **Run to Failure**.

## Set Basic Options

Set parameters that affect overall code generation.

### Description

The **Set Basic Options** task sets options that are fundamental to HDL code generation. These options include selecting the DUT and selecting the target language. The basic options are the same as those found in the top-level **HDL Code** pane of the Model Configuration Parameters dialog box, except that the **Code generation output** group is omitted.

### See Also

See also “HDL Code Generation Pane: General” on page 7-8.

### **Set Advanced Options**

Set parameters that specify detailed characteristics of the generated code.

#### **Description**

The advanced options are the same as those found in the **HDL Code Generation > Global Settings** pane of the Configuration Parameters dialog box and the Model Explorer.

#### **See Also**

See also “HDL Code Generation Pane: Global Settings” on page 7-21.



## Set Testbench Options

Set options that determine characteristics of generated test bench code.

### Description

The test bench options are the same as those found in the **HDL Code Generation > Test Bench** pane of the Configuration Parameters dialog box and the Model Explorer.

### See Also

See also “HDL Code Generation Pane: Test Bench” on page 7-72.

## Generate RTL Code and Testbench

Select and initiate generation of RTL code, RTL test bench, and cosimulation model.

### Description

The **Generate RTL Code and Testbench** task enables choosing what type of code or model that you want to generate. You can select any combination of the following:

- **Generate RTL code:** Generate RTL code in the target language.
- **Generate RTL testbench:** Generate an RTL test bench in the target language.
- **Generate cosimulation model** (requires HDL Verifier): Generate a cosimulation model. Selecting this check box enables the next option.
- **Cosimulation model for use with:** Select one of the following options from the menu:
  - **Mentor Graphics ModelSim:** This option is the default. If your installation includes HDL Verifier for use with Mentor Graphics ModelSim, the coder generates and opens a Simulink model that contains an HDL Cosimulation block for Mentor Graphics ModelSim.
  - **Cadence Incisive:** If your installation includes HDL Verifier for use with Cadence Incisive, the coder generates and opens a Simulink model that contains an HDL Cosimulation block for Cadence Incisive.
- **Generate validation model:** Generate a validation model that highlights generated delays and other differences between your original model and the generated cosimulation model. With a validation model, you can observe the effects of streaming, resource sharing, and delay balancing.

The validation model contains the DUT from the original model and the DUT from the generated cosimulation model. Using the validation model, you can verify that the output of the optimized DUT is bit-true to the results produced by the original DUT.

- **Generate FPGA top level wrapper:** Generate an HDL code wrapper and a constraint file that contains pin map information and clock constraints. When you select a specific target device in the **Set Target Device and Synthesis Tool** task, **Generate FPGA top level wrapper** is

automatically selected. Generating this wrapper enables generation of the corresponding programming file for the **Generate Programming File** task in the **Download to Target** folder.

When you select **Generate FPGA top level wrapper**, the task **Annotate Model with Synthesis Result** is not available in the **FPGA Synthesis and Analysis** folder. To perform back-annotation analysis, clear the check box for **Generate FPGA top level wrapper**.

### **See Also**

See also “Generating a Simulink Model for Cosimulation with an HDL Simulator”.

## **FPGA Synthesis and Analysis Overview**

Create projects for supported FPGA synthesis tools, perform FPGA synthesis, mapping, and place/route tasks, and annotate critical paths in the original model

### **Description**

The tasks in the **FPGA Synthesis and Analysis** folder enable you to:

- Create FPGA synthesis projects for supported FPGA synthesis tools.
- Launch supported FPGA synthesis tools, using the project files to perform synthesis, mapping, and place/route tasks.
- Annotate your original model with critical path information obtained from the synthesis tools.

For a list of supported third-party synthesis tools, see “Supported Third-Party Synthesis Tools”.

The tasks in the folder are:

- **Create Project**
- **Perform Synthesis and P/R**
- **Annotate Model with Synthesis Result**

### **See Also**

See also “FPGA Synthesis and Analysis” on page 19-40.

## Create Project

Create FPGA synthesis project for supported FPGA synthesis tool.

### Description

This task creates a synthesis project for the selected synthesis tool and loads the project with the HDL code generated for your model.

Specify additional files you want included in the new ISE project. You should include only file types supported by ISE. If an included file does not exist, the software cannot create the ISE project.

Tips:

- You may add files manually into the edit box or by using the browser.
- If you are adding the files manually, separate each file name with a carriage return (using the browser adds this hard return automatically).

When the project creation completes, the HDL Workflow Advisor displays a link to the project in the right pane. Click this link to view the project in the synthesis tool project window.

For a list of supported third-party synthesis tools, see “Supported Third-Party Synthesis Tools”.

### See Also

See also “Creating a Synthesis Project” on page 19-40.

## **Perform Synthesis and P/R Overview**

Launch supported FPGA synthesis tools to perform synthesis, mapping, and place/route tasks.

### **Description**

The tasks in the **Perform Synthesis and P/R** folder enable you to:

- **Perform Logic Synthesis:** Launch supported FPGA synthesis tool and synthesize the generated HDL code.
- **Perform Mapping:** Launch supported FPGA synthesis tool and perform mapping and timing analysis.
- **Perform Place and Route:** Launch supported FPGA synthesis tool and perform place and route functions.

For a list of supported third-party synthesis tools, see “Supported Third-Party Synthesis Tools”.

### **See Also**

See also “FPGA Synthesis and Analysis” on page 19-40

## Perform Logic Synthesis

Launch supported FPGA synthesis tool and synthesize the generated HDL code.

### Description

The **Perform Logic Synthesis** task:

- Launches the synthesis tool in the background.
- Opens the previously generated synthesis project, compiles HDL code, synthesizes the design, and emits netlists and related files.
- Displays a synthesis log in the **Result** subpane.

### See Also

See also “Performing Synthesis, Mapping, and Place and Route” on page 19-43.

## **Perform Mapping**

Launches supported FPGA synthesis tool and maps the synthesized logic design to the target FPGA

### **Description**

The **Perform Mapping** task:

- Launches the synthesis tool in the background.
- Runs a mapping process that maps the synthesized logic design to the target FPGA.
- Emits a circuit description file for use in the place and route phase.
- Also emits pre-routing timing information for use in critical path analysis and back annotation of your source model.
- Displays a log in the **Result** subpane.

### **See Also**

See also “Performing Synthesis, Mapping, and Place and Route” on page 19-43.



## Perform Place and Route

Launches the synthesis tool in the background and runs a Place and Route process.

### Description

The **Perform Place and Route** task:

- Launches the synthesis tool in the background.
- Runs a Place and Route process that takes the circuit description produced by the previous mapping process, and emits a circuit description suitable for programming an FPGA.
- Also emits post-routing timing information for use in critical path analysis and back annotation of your source model.
- Displays a log in the **Result** subpane.

### Tips

If you select **Skip this task**, the HDL Workflow Advisor executes the workflow, but omits the **Perform Place and Route** task, marking it **Passed**. You might want to select **Skip this task** if you prefer to do place and route work manually.

If **Perform Place and Route** fails, but you want to use the post-mapping timing results to find critical paths in your model, you can select **Ignore place and route errors** and continue to the **Annotate Model with Synthesis Result** task.

### See Also

See also “Performing Synthesis, Mapping, and Place and Route” on page 19-43.

## **Annotate Model with Synthesis Result**

Analyzes pre- or post-routing timing information and visually highlights critical paths in your model

### **Description**

The **Annotate Model with Synthesis Result** task helps you to identify critical paths in your model. At your option, the task analyzes pre- or post-routing timing information produced by the **Perform Place and Route** task, and visually highlights one or more critical paths in your model.

If **Generate FPGA top level wrapper** is selected in the **Generate RTL Code and Testbench** task, **Annotate Model with Synthesis Result** is not available. To perform back-annotation analysis, clear the check box for **Generate FPGA top level wrapper**.

### **Input Parameters**

#### **Critical path source**

Select pre-route or post-route.

#### **Critical path number**

You can annotate up to 3 critical paths. Select the number of paths you want to annotate.

#### **Show all paths**

Show critical paths, including duplicate paths.

#### **Show unique paths**

Show only the first instance of a path that is duplicated.

#### **Show delay data**

Annotate the cumulative timing delay on each path.

#### **Show ends only**

Show the endpoints of each path, but omit the connecting signal lines.

### **Results and Recommended Actions**

When the **Annotate Model with Synthesis Result** task runs to completion, the coder displays the DUT with critical path information highlighted.

**See Also**

“Annotating Your Model with Critical Path Information” on page 19-47

## Download to Target Overview

The **Download to Target** folder supports the following tasks:

- **Generate Programming File:** Generate an FPGA programming file.
- **Program Target Device:** Download generated programming file to the target development board.
- **Generate xPC Target Interface** (for Speedgoat target devices only):  
Generate a model that contains an xPC Target interface subsystem.

### See Also

For summary information on each **Download to Target** task, select the task icon and then click the HDL Workflow Advisor **Help** button.

## **Generate Programming File**

The **Generate Programming File** task generates an FPGA programming file that is compatible with the selected target device.

### **Program Target Device**

The **Program Target Device** task downloads the generated FPGA programming file to the selected target device.

Before executing the **Program Target Device** task, make sure that your host PC is properly connected to the target development board via the required programming cable.

## **Generate xPC Target Interface**

The **Generate xPC Target Interface** task generates a model containing an interface subsystem that you can plug in to an xPC Target model.

The naming convention for the generated model is:

`gm_fpgamodelname_xpc.mdl`

where `fpgamodelname` is the name of the original model.

## **Save and Restore HDL Workflow Advisor State**

You can save the current settings of the HDL Workflow Advisor to a named *restore point*. At a later time, you can restore the same settings by loading the restore point data into the HDL Workflow Advisor.

### **See Also**

For detailed information on how to create, save, and load a restore point, see “Save and Restore HDL Workflow Advisor State” on page 19-21.

## **FPGA-in-the-Loop Implementation**

Set FIL options and run FIL processing.

### **Set FIL Options**

Set board IP and MAC addresses and select additional files, if required.

#### **Board IP Address**

Use this option for setting the board’s IP address if it is not the default IP address (192.168.0.2).

#### **Board MAC Address**

Under most circumstances, you do not need to change the Board MAC address. You will need to do so if you connect more than one FPGA development board to a single computer (for which you must have a separate NIC for each board). You must change the Board MAC address for additional boards so that each address is unique.

#### **Additional Source Files**

Select additional source files for the HDL design that is to be verified on the FPGA board, if required. HDL Workflow Advisor will attempt to identify the file type; change the file type in the **File Type** column if it is incorrect.

### **Build FPGA-in-the-Loop**

During the build process, the following actions occur:



- FPGA-in-the-Loop generates a FIL block named after the top-level module and places it in a new model.
- After new model generation, FIL opens a command window. In this window, the FPGA design software performs synthesis, fit, place-and-route, timing analysis, and FPGA programming file generation. When the process completes, a message in the command window prompts you to close the window.
- FPGA-in-the-Loop builds a testbench model around the generated FIL block.

### **Check USRP® Compatibility**

The model must have 2 input ports and 2 output ports of signed 16-bit signals.

### **Generate FPGA Implementation**

This step initiates FPGA programming file creation. For Input Parameters, enter the path to the Ettus Research™ USRP® FPGA files you previously downloaded. If you have not yet downloaded these files, see the Communications with USRP® documentation for “Customizing the USRP® Device” for a complete set of instructions.

When this step completes, see the instructions for downloading the programming file to the FPGA and running the simulation in “Customizing the USRP® Device”.



# Code Generation Control Files

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- “READ THIS FIRST: Control File Compatibility and Conversion Issues” on page 22-2
- “Overview of Control Files” on page 22-4
- “Structure of a Control File” on page 22-7
- “Code Generation Control Objects and Methods” on page 22-8
- “Using Control Files in the Code Generation Process” on page 22-16
- “Specifying Block Implementations and Parameters in the Control File” on page 22-17
- “Generating Black Box Control Statements Using `hdlnewblackbox`” on page 22-23

## READ THIS FIRST: Control File Compatibility and Conversion Issues

### In this section...

“Conversion From Use of Control Files Recommended” on page 22-2

“Detaching Existing Models From Control Files” on page 22-2

“Applying Control File Settings” on page 22-3

“Backwards Compatibility” on page 22-3

### Conversion From Use of Control Files Recommended

As of release R2010b, the coder does not support the attachment of a control file to a new model. Instead, the coder now saves nondefault HDL-related model settings, block implementation selections and implementation parameter settings to the model itself. This eliminates the need to maintain a separate control file. Because the coder saves only the nondefault parameter settings, the loading and saving of models is more efficient. The recommended practice is to discontinue use of control files and convert existing models. This simple process is described in the next section.

### Detaching Existing Models From Control Files

If you have existing models with attached control files, you should convert them to the current format and remove control file linkage. To convert a model that has an attached control file:

- 1 Open the model. When the coder opens a model that has an attached control file, it loads and sets parameters as specified in the control file, and clears the control file linkage from the model. During this process, the coder displays the following messages:

```
Found HDL control file attached to the model 'test_model' ...
Loading control file 'test_model_control' ...
Successfully loaded control file 'test_model_control.m' ...
Please consider saving the model to make changes permanent ...
Detaching the HDL control file from the model...
```

- 2 Save the model. The model now preserves nondefault settings. The next time you open the model, the coder will not display control file status messages.

Note that although the model is now detached from the control file, the control file itself is preserved so that you can apply it to other models if you wish.

## **Applying Control File Settings**

The coder provides the `hdlapplycontrolfile` utility as a quick way to transfer HDL settings from existing models that have attached control files to other models. See `hdlapplycontrolfile` for further information.

## **Backwards Compatibility**

For backward compatibility, the coder continues to support models that have attached control files.

## Overview of Control Files

### In this section...

“What Is a Control File?” on page 22-4

“Selectable Block Implementations and Implementation Parameters” on page 22-5

“Implementation Mappings” on page 22-5

### What Is a Control File?

*Code generation control files* (referred to in this document as *control files*) let you

- Save your model’s HDL code generation options in a persistent form.
- Extend the HDL code generation process and direct its details.

You attach a control file to your model using either the `makehdl` command or the Configuration Parameters dialog box. You do not need to know internal details of the code generation process to use a control file.

Control files support the following statement types:

- *Selection/action* statements provide a general framework for the application of different types of transformations to selected model components. Selection/action statements *select* a group of blocks within your model, and specify an *action* to be executed when code is generated for each block in the selected group.

Selection criteria include block type and location within the model. For example, you might select all built-in Gain blocks at or below the level of a certain subsystem within your model.

A typical action applied to such a group of blocks is to direct the code generator to execute a specific *block implementation method* when generating HDL code for the selected blocks. For example, for Gain blocks, you might choose a method that generates code that is optimized for speed or chip area.

- *Property setting* statements let you

- Select the model or subsystem from which code is to be generated.
- Set the values of code generation properties to be passed to the code generator. The properties and syntax are the same as those used for the `makehdl` command.
- Set up default or template HDL code generation settings for your organization.

## Selectable Block Implementations and Implementation Parameters

Selection/action statements provide a general framework that lets you define how the coder acts upon selected model components. The current release supports one such action: execution of block implementation methods.

Block implementation methods are code generator components that emit HDL code for the blocks in a model. This document refers to block implementation methods as *block implementations* or simply *implementations*.

The coder provides at least one block implementation for every supported block. This is called the *default implementation*. In addition, the coder provides selectable alternate block implementations for certain block types. Each implementation is optimized for different characteristics, such as speed or chip area. For example, you can choose Gain block implementations that use canonic signed digit (CSD) techniques (reducing area), or use a default implementation that retains multipliers.

For many block implementations, you can set *implementation parameters* that provide a further level of control over how code is generated for a particular implementation. For example, most blocks support the 'OutputPipeline' implementation parameter. This parameter lets you specify the generation of output pipeline stages for selected blocks by passing in the required pipeline depth as the parameter value.

## Implementation Mappings

Control files let you specify one or more *implementation mappings* that control how HDL code is to be generated for a specified group of blocks within the model. An implementation mapping is an association between a selected block or set of blocks within the model and a block implementation.

To select the set of blocks to be mapped to a block implementation, you specify

- A `modelscope`: a Simulink block path (which could incorporate an entire model or sublevel of the model, or a specific subsystem or block)
- A `blocktype`: a Simulink block type that corresponds to the selected block implementation

During code generation, each defined `modelscope` is searched for instances of the associated `blocktype`. For each such block instance encountered, the code generator uses the selected block implementation.



## Structure of a Control File

The required elements for a code generation control file are as follows:

- A control file implements a single function, which is invoked during the code generation process.

The function must instantiate a *code generation control object*, set its properties, and return the object to the code generator.

Setting up a code generation control object requires the use of a small number of methods, as described in “Code Generation Control Objects and Methods” on page 22-8. You do not need to know internal details of the code generation control object or the class to which it belongs.

You construct the object using the `hdlnewcontrol` function. The argument to `hdlnewcontrol` is the name of the control file itself. Use the `mfilename` function to pass in the file name, as shown in the following example.

```
function c = dct8config
c = hdlnewcontrol(mfilename);

% Set target language for Verilog.
c.set('TargetLanguage','Verilog');

% Set top-level subsystem from which code is generated.
c.generateHDLFor('dct8_fixed/OneD_DCT8');
```

- Following the constructor call, your code will invoke methods of the code generation control object. The previous example calls the `set` and `generateHDLFor` methods. These and other public methods of the object are discussed in “Code Generation Control Objects and Methods” on page 22-8.
- Your control file must be attached to your model before code generation, as described in “Using Control Files in the Code Generation Process” on page 22-16. The interface between the code generator and your attached control file is automatic.
- A control file must be located in either the current working folder, or a folder that is in the MATLAB path.

However, your control files should not be located within the MATLAB tree because they could be overwritten by subsequent installations.

## Code Generation Control Objects and Methods

### In this section...

“Overview” on page 22-8

“hdlnewcontrol” on page 22-8

“forEach” on page 22-8

“forAll” on page 22-13

“set” on page 22-13

“generateHDLFor” on page 22-14

“hdlnewcontrolfile” on page 22-15

### Overview

Code generation control objects are instances of the class `slhdlcoder.ConfigurationContainer`. This section describes the public methods of that class that you can use in your control files. Other methods of this class are for MathWorks internal development use only. The methods are described in the following sections:

### hdlnewcontrol

The `hdlnewcontrol` function constructs a code generation control object. The syntax is

```
object = hdlnewcontrol(mfilename);
```

The argument to `hdlnewcontrol` is the name of the control file itself. Use the `mfilename` function to pass in the file name string.

### forEach

This method establishes an implementation mapping between an HDL block implementation and a selected block or set of blocks within the model. The syntax is

```
object.forEach({'modelscope'}, ...
```

```
'blocktype', {'block_parms'}, ...
'implementation', {'implementation_parms'})
```

The `forEach` method selects a set of blocks (modelscope) that is searched, during code generation, for instances of a specified type of block (`blocktype`). Code generation for each block instance encountered uses the HDL block implementation specified by the `implementation` parameter.

---

**Note** You can use the `hdlnewforeach` function to generate `forEach` method calls for insertion into your control files. See “Generating Selection/Action Statements with the `hdlnewforeach` Function” on page 22-18 for more information.

---

The following table summarizes the arguments to the `forEach` method.

Argument	Type	Description
<code>block_parms</code>	Cell array of strings	Reserved for future use. Pass in an empty cell array ({} ) as a placeholder.
<code>blocktype</code>	String	Block specification that identifies the type of block that is to be mapped to the HDL block implementation. Block specification syntax is the same as that used in the <code>add-block</code> command. For built-in blocks, the <code>blocktype</code> is of the form  'built-in/blockname'  For other blocks, <code>blocktype</code> must include the full path to the library containing the block, for example:  'dsparch4/Digital Filter'

Argument	Type	Description
implementation	String	<p>The <code>implementation</code> string represents an HDL block implementation to be used in code generation for blocks that meet the <code>modelscope</code> and <code>blocktype</code> search criteria. Every block has at least one implementation. “Blocks Supported for HDL Code Generation” on page 9-3 provides guidelines for specifying implementations, and lists supported blocks and their implementations.</p>
implementation_parms	Cell array of p/v pairs	<p>Cell array of property/value pairs that set code generation parameters for the block implementation specified by the <code>implementation</code> argument. Specify parameters as: <code>'Property', value</code> where <code>'Property'</code> is the name of the property and <code>value</code> is the value applied to the property. If the implementation does not have parameters, or you want to use default parameters, pass in an empty cell array (<code>{}</code>) .</p> <p>“Blocks Supported for HDL Code Generation” on page 9-3 describes the syntax of each parameter, and describes how the parameter affects generated code.</p> <p>“Blocks Supported for HDL Code Generation” on page 9-3 lists supported blocks and their implementations and parameters.</p> <p>You can use the <code>hdlnewforeach</code> function to obtain the parameter names for selected block(s) in a model. See “Specifying Block Implementations and Parameters in the Control File” on page 22-17.</p>

Argument	Type	Description
modelscope	String or cell array of strings	<p>Strings defining one or more Simulink paths:  <code>{'path1' 'path2' ... 'pathN'}</code></p> <p>Each path defines a modelscope: a set of blocks that participate in an implementation mapping. The set of blocks in a modelscope could include the entire model, blocks at a specified level of the model, or a specific block or subsystem. A path terminating in a wildcard ('*') includes blocks at or below the model level specified by the path. You can use the period (.) to represent the root-level model at the top of a modelscope, instead of explicitly coding the model name. For example: <code>./subsyslevel/block</code>. See also “Representation of the Root Model in modelscopes” on page 22-11 and “Resolution of modelscopes” on page 22-12. Syntax for modelscope paths is</p> <ul style="list-style-type: none"> <li>• <code>'model/*'</code>: all blocks in the model</li> <li>• <code>'model/subsyslevel/block'</code>: a specific block within a specific level of the model</li> <li>• <code>'model/subsyslevel/subsystem'</code>: a specific subsystem block within a specific level of the model</li> <li>• <code>'model/subsyslevel/*'</code>: any block within a specific model level</li> </ul>

### Representation of the Root Model in modelscopes

You can represent the root-level model at the top of a modelscope as:

- The full model name, as in the following listing:

```
cfg.forEach( 'aModel/Subsystem/MinMax', ...
    'built-in/MinMax', {}, ...
    'default');
```

If you explicitly code the model name in a modelscope, and then save the model under a different name, the control file becomes invalid because it

references the previous model name. It is then required that you edit the control file and change all such modelscopes to reference the new model.

- The period (.) character, representing the current model as an abstraction, as in the following listing:

```
cfg.forEach( './Subsystem/MinMax', ...
    'built-in/MinMax', {}, ...
    'Cascade');
```

If you represent the model in this way, and then save the model under a different name, the control file does not require a change. Using the period to represent the root-level model makes the modelscope independent of the model name, and therefore more portable.

When you save HDL code generation settings to a control file, the period is used to represent the root-level model.

## Resolution of modelscopes

A possible conflict exists in the `forEach` specifications in the following example:

```
% 1. Use default (multipliers) Gain block implementation
% for one specific Gain block within OneD_DCT8 subsystem
c.forEach('./OneD_DCT8/Gain14',...
    'built-in/Gain', {},...
    'default', {});
% 2. Use factored CSD Gain optimization
% for all Gain blocks at or below level of OneD_DCT8 subsystem.
c.forEach('./OneD_DCT8/*',...
    'built-in/Gain', {},...
    'default', {'ConstMultiplierOptimization','FCSD'});
```

The first `forEach` call defines an implementation mapping for a specific block within the subsystem `OneD_DCT8`. The second `forEach` call specifies a non-default implementation parameter ('`ConstMultiplierOptimization`') for all blocks within or below the subsystem `OneD_DCT8`.

The coder resolves such ambiguities by giving higher priority to the more specific modelscope. In the example, the first modelscope is the more specific.

Five levels of modelscope priority from most specific (1) to least specific (5) are defined:

- 1** A/B/C/block
- 2** A/B/C/\*
- 3** A/B/\*
- 4** \*
- 5** Unspecified. Use the default implementation.

## forall

This method is a shorthand form of `forEach`. Only one modelscope path is specified. The `modelscope` argument is specified as a string (not a cell array) and it is implicitly terminated with `'/*'`. The syntax is

```
object.forAll('modelscope', ...
             'blocktype', {'block_parms'}, ...
             'implementation', {'implementation_parms'})
```

Other arguments are the same as those described for “`forEach`” on page 22-8.

## set

The `set` method sets one or more code generation properties. The syntax is

```
object.set('PropertyName', PropertyValue,...)
```

The argument list specifies one or more code generation options as property/value pairs. You can set all the code generation properties *except* the `HDLControlFiles` property.

---

**Note** If you specify the same property in both your control file and your `makehdl` command, the property will be set to the value specified in the control file.

Likewise, when generating code via the GUI, if you specify the same property in both your control file and the **HDL Coder** options panes, the property will be set to the value specified in the control file.

---

## **generateHDLFor**

This method selects the model or subsystem from which code is to be generated. The syntax is

```
object.generateHDLFor('simulinkpath')
```

The argument is a string specifying the full path to the model or subsystem from which code is to be generated.

To make your control files more portable, you can represent the root-level model in the path as an abstraction, as in the following example:

```
function c = newforeachexamp
c = hdlnewcontrol(mfilename);

% Set top-level subsystem from which code is generated.
c.generateHDLFor('./symmetric_fir');
...
```

The above `generateHDLFor` call is valid for any model containing a subsystem named `symmetric_fir` at the root level.

Use of this method is optional. You can specify the same parameter in the **Generate HDL for** menu in the **HDL Coder** pane of the Configuration Parameters dialog box, or in a `makehdl` command.



## **hdlnewcontrolfile**

The coder provides the `hdlnewcontrolfile` utility to help you construct code generation control files. Given a selection of one or more blocks from your model, `hdlnewcontrolfile` generates a control file containing `forEach` statements and comments providing information about supported implementations and parameters, for the selected blocks. The generated control file is automatically opened in the MATLAB editor for further customization. See the `hdlnewcontrolfile` function reference page for details.

## Using Control Files in the Code Generation Process

In this section...
“Where to Locate Your Control Files” on page 22-16
“Making Your Control Files More Portable” on page 22-16

### Where to Locate Your Control Files

Before you create a control file or use a control file in code generation, be sure to observe the following requirements for the location of control files:

- A control file must be stored in a folder that is in the MATLAB path, or the current working folder.
- Do not locate a control file within the MATLAB tree, because it could be overwritten by subsequent MATLAB installations.

### Making Your Control Files More Portable

It can be advantageous to code your control files so that they are independent of a particular model name. To do this, use the period (.) to represent the root-level model at the beginning of all modelscope paths. For example:

```
cfg.forEach( './Subsystem/MinMax', ...  
    'built-in/MinMax', {}, ...  
    'Cascade');
```

If you code modelscopes in this way, all modelscopes are interpreted as references to the current model, rather than as references to an explicitly named model. Therefore, you can save your model under a different name, and references to the root-level model will be valid.

# Specifying Block Implementations and Parameters in the Control File

## In this section...

“Overview” on page 22-17

“Generating Selection/Action Statements with the `hdlnewforeach` Function” on page 22-18

## Overview

The coder provides a default HDL block implementation for supported blocks. In addition, the coder provides selectable alternate HDL block implementations for several block types. Using selection/action statements (`forEach` or `forall` method calls) in a control file, you can specify the block implementation to be applied to all blocks of a given type (within a specific `modelscope`) during code generation. For many implementations, you can also pass in implementation parameters that provide additional control over code generation details.

You select HDL block implementations by specifying the implementation name as a string. “Blocks Supported for HDL Code Generation” on page 9-3 summarizes the supported blocks, their implementation names, and implementation parameters. Pass in the implementation name and implementation parameters (if any) to the implementation argument of a `forEach` or `forall` call. The following example specifies the `Tree` implementation for all `Sum` blocks in a model, with 2 output pipeline stages.

```
config.forEach('*',...
    'built-in/Sum', {},...
    'Tree', {'OutputPipeline', 2});
```

Given the implementation name, the coder calls the corresponding code generation method. You do not need to know internal details of the implementation classes.

## Generating Selection/Action Statements with the `hdlnewforeach` Function

Determining the block path, type, implementation specification, and implementation parameters for a large number of blocks in a model can be time-consuming. Use the `hdlnewforeach` function to create selection/action statements in your control files. Given a selection of one or more blocks from your model, `hdlnewforeach` returns the following for each selected block, as string data in the MATLAB workspace:

- A `forEach` call coded with the `modelscope`, `blocktype`, and default implementation arguments for the block
- (Optional) A cell array of strings enumerating the available implementations for the block.
- (Optional) A cell array of strings enumerating the names of implementation parameters corresponding to the block implementations. `hdlnewforeach` does not list data types and other details of block implementation parameters. These details are described in “Block Implementation Parameters” on page 9-49.

Having generated this information, you can copy and paste the strings into your control file.

### `hdlnewforeach` Example

This example uses `hdlnewforeach` to construct a `forEach` call that specifies generation of two output pipeline stages after the output of a selected `Sum` block within the `sfir_fixed` example model. To create the control file:

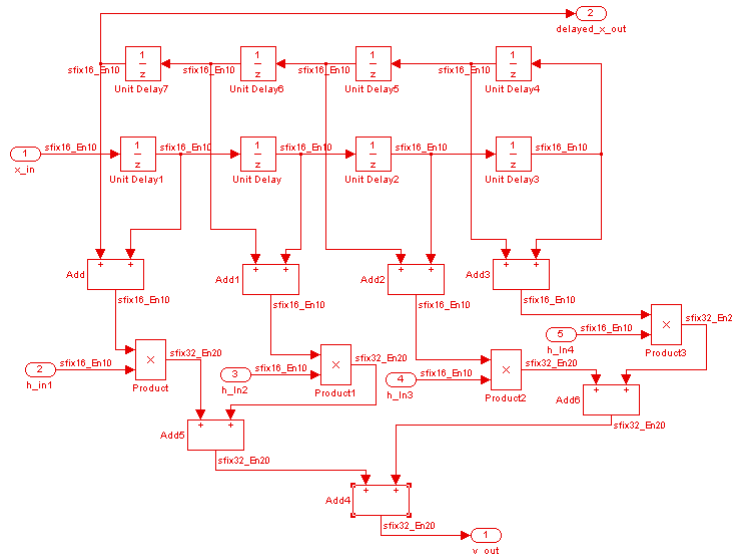
- 1** In the MATLAB Command Window, select **File > New > Blank M-File**. The MATLAB Editor opens an empty file.
- 2** Create a skeletal control file by entering the following code into the MATLAB Editor window:

```
function c = newforeachexamp
c = hdlnewcontrol(mfilename);

% Set top-level subsystem from which code is generated.
c.generateHDLFor('sfir_fixed/symmetric_fir');
```

```
% INSERT FOREACH CALL BELOW THIS LINE.
```

- 3** Save the file as `newforeachexamp.m`.
- 4** Open the `sfir_fixed` example model.
- 5** Close the `checkhdl` report window and activate the `sfir_fixed` model window.
- 6** In the `symmetric_fir` subsystem window, select the `Add4` block, as shown in the following figure.



Now you are ready to generate a `forEach` call for the selected block:

- 1** Type the following command at the MATLAB prompt.

```
[cmd,impl,parms] = hd1newforeach(gcb)
```

- 2** The command returns the following results:

```
c.forEach('./symmetric_fir/Add4',...
```

```
'built-in/Sum', {},...  
'default', {}); % Default architecture is 'Linear'
```

```
impl =  
  
    {3x1 cell}  
  
parms =  
  
    {1x2 cell}    {1x2 cell}    {1x2 cell}
```

The first return value, `cmd`, contains the generated `forEach` call. The `forEach` call specifies the default implementation for the Sum block, specified as `'default'`. Also by default, no parameters are passed in for this implementation.

- 3** The second return value, `impl`, is a cell array containing three strings representing the available implementations for the Sum block. The following example lists the contents of the `impl` array:

```
impl{1}  
  
ans =  
  
    'Linear'  
    'Cascade'  
    'Tree'
```

See the table Built-In/Sum on page 9-20 for information about these implementations.

- 4** The third return value, `parms`, is a cell array containing three strings that represent the available implementations parameters corresponding to the previously listed Sum block implementations. The following example lists the contents of the `parms` array:

```
parms{1:3}
```

```

ans =

    'InputPipeline'    'OutputPipeline'

ans =

    'InputPipeline'    'OutputPipeline'

ans =

    'InputPipeline'    'OutputPipeline'

```

This listing shows that each of the Sum block implementations has two parameters, 'InputPipeline' and 'OutputPipeline'. This indicates that parameter/value pairs of the form {'OutputPipeline', val} can be passed in with any of the Sum block implementations.

hdlnewforeach does not provide information about the data type, valid range, or other constraints on val. Some implementation parameters take numeric values, while others take strings. See “Block Implementation Parameters” on page 9-49 for details on implementation parameters.

- 5 Copy the three lines of foreach code from the MATLAB Command Window and paste them into the end of your newforeachexamp.m file:

```

% INSERT FOREACH CALL BELOW THIS LINE.
c.foreach('./symmetric_fir/Add4',...
    'built-in/Sum', {},...
    'default', {}); % Default architecture is 'Linear'

```

- 6 In this example, you will specify the default Sum block implementation for the Add4 block, but with generation of two output pipeline stages before the final output. To do this, pass in the 'OutputPipeline' parameter with a value of 2. Modify the final line of the foreach call in your control file:

```

% INSERT FOREACH CALL BELOW THIS LINE.
c.foreach('./symmetric_fir/Add4',...
    'built-in/Sum', {},...

```

```
'default', {'OutputPipeline', 2}); % Default architecture is 'Linear'
```

**7** Save the control file.

**8** The following code shows the complete control file:

```
function c = newforeachexamp
c = hdlnewcontrol(mfilename);

% Set top-level subsystem from which code is generated.
c.generateHDLFor('sfir_fixed/symmetric_fir');
% INSERT FOREACH CALLS HERE.
c.forEach('sfir_fixed/symmetric_fir/Add4',...
c.forEach('./symmetric_fir/Add4',...
'built-in/Sum', {},...
'default', {'OutputPipeline', 2}); % Default architecture is 'Linear'
```

---

**Note** For convenience, `hdlnewforeach` supports a more abbreviated syntax than that used in the previous example. See the `hdlnewforeach` reference page.

---



## Generating Black Box Control Statements Using `hdlnewblackbox`

The `hdlnewblackbox` function provides a simple way to create the control file statements that are required to generate black box interfaces for one or more subsystems. `hdlnewblackbox` is similar to `hdlnewforeach`).

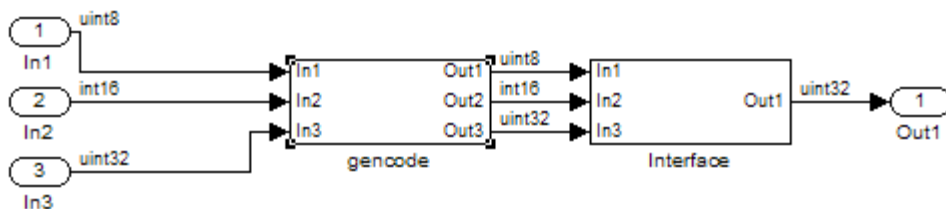
Given a selection of one or more subsystems from your model, `hdlnewblackbox` returns the following as string data in the MATLAB workspace for each selected subsystem:

- A `forEach` call coded with the `modelscope`, `blocktype`, and default implementation class (`SubsystemBlackBoxHDLInstantiation`) arguments for the block.
- (Optional) A cell array of strings enumerating the available implementations classes for the subsystem.
- (Optional) A cell array of cell arrays of strings enumerating the names of implementation parameters corresponding to the implementation classes. `hdlnewblackbox` does not list data types and other details of implementation parameters.

See `hdlnewblackbox` for the full syntax description of the function.

As an example, suppose that you want to generate black box control file statements for the subsystem `gencode` from the `subsystemst` model. Using `hdlnewblackbox`, you can do this as follows:

- 1** Activate the `subsystemst/top` subsystem window.
- 2** Select the subsystems for which you want to create control statements. In the following figure, `gencode` is selected.



**3** Deselect the subsystemst/top subsystem.

**4** Type the following command at the MATLAB prompt:

```
[cmd,impl,parms] = hdlnewblackbox
```

**5** The command returns the following results:

```
cmd =

c.forEach('subsystemst/top/gencode',...
'built-in/SubSystem', {},...
'BlackBox', {});

impl =

{4x1 cell}

parms =

{} {1x11 cell} {1x12 cell} {1x11 cell}
```

The first return value, `cmd`, contains the generated `forEach` call. The `forEach` call specifies the default back box implementation for the subsystem blocks: `BlackBox`. Also by default, no parameters are passed in for this implementation.

- 6** The second return value, `impl`, is a cell array containing three strings listing available implementations for the Subsystem block. The following example lists the contents of the `impl` array:

```
>> impl{1}

ans =

    'hdldefaults.NoHDL Emission'
    'hdldefaults.SubsystemBlackBoxHDLInstantiation'
    'hdldefaults.XilinxBlackBoxHDLInstantiation'
    'hdldefaults.AlteraDSPBuilderBlackBox'
```

- 7** The third return value, `parms`, is a cell array containing strings that represent the available implementations parameters corresponding to the previously listed Subsystem block implementations. The parameters of interest in this case are those available for `BlackBox`. These are enumerated in `parms{2}`, as shown in the following listing:

```
parms{1}

ans =

Columns 1 through 4

    'ClockInputPort' [1x20 char]    'ResetInputPort'    'AddClockPort'

Columns 5 through 9

    'AddClockEnablePort' 'AddResetPort'    [1x20 char]    [1x20 char]    'EntityName'

Columns 10 through 11

    'InputPipeline' 'OutputPipeline'
```

Implementation parameters for subsystems and other black box interface classes are described in “Customize the Generated Interface” on page 15-54.

- 8** Having generated this information, you can now copy and paste the strings into a control file.



# Properties — Alphabetical List

---

# BalanceDelays property

---

**Purpose** Enable delay balancing

**Settings** 'on' (default)  
Enable delay balancing.  
'off'  
Disable delay balancing.

**Usage Notes** A common problem is that optimizations can introduce delays along the critical path in a model, but equivalent delays are not introduced on other, parallel signal paths. This can introduce differences in numerics between the original model and the generated model and HDL code. Manual insertion of compensating delays along the other paths is possible, but is error-prone and does not scale well for very large models with many signal paths.

To help you solve this problem, the coder supports *delay balancing*. When you enable delay balancing, if the coder detects introduction of new delays along one path, it inserts matching delays on the other paths. When delay balancing is enabled, the generated model is functionally equivalent to the original model.

**See Also** “Delay Balancing” on page 13-34

# BlockGenerateLabel property

---

<b>Purpose</b>	Specify string to append to block labels used for HDL GENERATE statements
<b>Settings</b>	'string' Default: '_gen' Specify a postfix string to append to block labels used for HDL GENERATE statements.
<b>See Also</b>	InstanceGenerateLabel, OutputGenerateLabel

# CastBeforeSum property

---

<b>Purpose</b>	Enable or disable type casting of input values for addition and subtraction operations before execution of operation
<b>Settings</b>	'on' (default) <b>Selected</b> (default) Typecast input values in addition and subtraction operations to the result type before operating on the values. 'off' <b>Cleared</b> Preserve the types of input values during addition and subtraction operations and then convert the result to the result type.
<b>See Also</b>	InlineConfigurations, LoopUnrolling, SafeZeroConcat, UseAggregatesForConst, UseRisingEdge, UseVerilogTimescale



<b>Purpose</b>	Check model or subsystem for HDL code generation compatibility
<b>Settings</b>	<p>'on'</p> <p><b>Selected</b></p> <p>Check the model or subsystem for HDL compatibility before generating code, and report problems encountered. This is equivalent to executing the checkhdl function before calling makehdl.</p> <p>'off' (default)</p> <p><b>Cleared</b> (default)</p> <p>Do not check the model or subsystem for HDL compatibility before generating code.</p>
<b>See Also</b>	checkhdl, makehdl

# ClockEnableInputPort property

---

## Purpose

Name HDL port for model's clock enable input signals

## Settings

'string'

Default: 'clk\_enable'

The string specifies the name for the model's clock enable input port.

If you override the default with (for example) the string 'filter\_clock\_enable' for the generating subsystem `filter_subsys`, the generated entity declaration might look as follows:

```
ENTITY filter_subsys IS
    PORT( clk           : IN  std_logic;
          filter_clock_enable : IN  std_logic;
          reset         : IN  std_logic;
          filter_subsys_in  : IN  std_logic_vector (15 DOWNTO 0);
          filter_subsys_out : OUT std_logic_vector (15 DOWNTO 0);
    );
END filter_subsys;
```

If you specify a string that is a VHDL or Verilog reserved word, the code generator appends a reserved word postfix string to form a valid VHDL or Verilog identifier. For example, if you specify the reserved word `signal`, the resulting name string would be `signal_rsvd`. See `ReservedWordPostfix` for more information.

## Usage Notes

The clock enable signal is asserted active high (1). Thus, the input value must be high for the generated entity's registers to be updated.

## See Also

`ClockInputPort`, `InputType`, `OutputType`, `ResetInputPort`

# ClockEnableOutputPort property

---

**Purpose** Specify name of clock enable output port

**Settings** 'string'

Default: 'ce\_out'

The string specifies the name for the generated clock enable output port.

A clock enable output is generated when the design requires one.

# ClockHighTime property

---

**Purpose** Specify period, in nanoseconds, during which test bench drives clock input signals high (1)

**Settings** ns

Default: 5

The clock high time is expressed as a positive integer.

The `ClockHighTime` and `ClockLowTime` properties define the period and duty cycle for the clock signal. Using the defaults, the clock signal is a square wave (50% duty cycle) with a period of 10 ns.

**Usage Notes** The coder ignores this property if `ForceClock` is set to 'off'.

**See Also** `ClockLowTime`, `ForceClock`, `ForceClockEnable`, `ForceReset`, `HoldTime`

**Purpose**

Specify generation of single or multiple clock inputs

**Settings**

'Single' (Default)

Generates a single clock input for the DUT. If the DUT is multirate, the input clock is the master clock rate, and a timing controller is synthesized to generate additional clocks as required.

'Multiple'

Generates a unique clock for each Simulink rate in the DUT. The number of timing controllers generated depends on the contents of the DUT.

**Usage  
Notes**

The oversample factor must be 1 (default) to specify multiple clocks.

**Example**

The following example specifies the generation of multiple clocks.

```
makehdl(gcb, 'ClockInputs', 'Multiple');
```

# ClockInputPort property

---

**Purpose** Name HDL port for model's clock input signals

**Settings** 'string'

Default: 'clk'.

The string specifies the clock input port name.

If you override the default with (for example) the string 'filter\_clock' for the generated entity `my_filter`, the generated entity declaration might look as follows:

```
ENTITY my_filter IS
  PORT( filter_clock : IN std_logic;
        clk_enable   : IN std_logic;
        reset        : IN std_logic;
        my_filter_in : IN std_logic_vector (15 DOWNTO 0); -- sfix16_En15
        my_filter_out: OUT std_logic_vector (15 DOWNTO 0); -- sfix16_En15
        );
END my_filter;
```

If you specify a string that is a VHDL or Verilog reserved word, the code generator appends a reserved word postfix string to form a valid VHDL or Verilog identifier. For example, if you specify the reserved word `signal`, the resulting name string would be `signal_rsvd`. See `ReservedWordPostfix` for more information.

**See Also** `ClockEnableInputPort`, `InputType`, `OutputType`

**Purpose** Specify period, in nanoseconds, during which test bench drives clock input signals low (0)

**Settings** Default: 5

The clock low time is expressed as a positive integer.

The `ClockHighTime` and `ClockLowTime` properties define the period and duty cycle for the clock signal. Using the defaults, the clock signal is a square wave (50% duty cycle) with a period of 10 ns.

**Usage Notes** The coder ignores this property if `ForceClock` is set to 'off'.

**See Also** `ClockHighTime`, `ForceClock`, `ForceClockEnable`, `ForceReset`, `HoldTime`

# ClockProcessPostfix property

---

**Purpose** Specify string to append to HDL clock process names

**Settings** 'string'

Default: '\_process'.

The coder uses process blocks for register operations. The label for each of these blocks is derived from a register name and the postfix `_process`. For example, the coder derives the label `delay_pipeline_process` in the following block declaration from the register name `delay_pipeline` and the default postfix string `_process`:

```
delay_pipeline_process : PROCESS (clk, reset)
BEGIN
    .
    .
    .
```

**See Also** `PackagePostfix`, `ReservedWordPostfix`



# CodeGenerationOutput property

---

**Purpose** Control production of generated code and display of generated model

**Settings** 'string'  
Default: 'GenerateHDLCode'  
Generate code but do not display the generated model.  
'GenerateHDLCodeAndDisplayGeneratedModel'  
Generate both code and model, and display model when completed.  
'DisplayGeneratedModelOnly'  
Create and display generated model, but do not proceed to code generation.

**See Also** “Defaults and Options for Generated Models” on page 12-11

# ComplexImagPostfix property

---

**Purpose** Specify string to append to imaginary part of complex signal names

**Settings** 'string'  
Default: '\_im'.

**See Also** ComplexRealPostfix

# ComplexRealPostfix property

---

<b>Purpose</b>	Specify string to append to real part of complex signal names
<b>Settings</b>	'string' Default: '_re'.
<b>See Also</b>	ComplexImagPostfix

# DateComment property

---

**Purpose** Specify whether or not to include time/date information in the generated HDL file header

**Settings** 'on' (default)  
Include time/date information in the generated HDL file header.

```
-----  
--  
-- File Name:hdlsrc\symmetric_fir.vhd  
-- Created: 2011-02-14 07:21:36  
--
```

'off'

Omit time/date information in the generated HDL file header.

```
-----  
--  
-- File Name:hdlsrc\symmetric_fir.vhd  
--
```

By omitting the time/date information in the file header, you can more easily determine if two HDL files contain identical code. You can also avoid extraneous revisions of the same file when checking in HDL files to a source code management (SCM) system.

# EDAScriptGeneration property

---

**Purpose** Enable or disable generation of script files for third-party tools

**Settings** 'on' (default)  
Enable generation of script files.  
'off'  
Disable generation of script files.

**See Also** “Script Generation for EDA Tools” on page 18-2

# EnablePrefix property

---

**Purpose** Specify base name string for internal clock enables in generated code

**Settings** 'string'

Default: 'enb'

Specify the string used as the base name for internal clock enables and other flow control signals in generated code.

**Usage Notes** Where only a single clock enable is generated, `EnablePrefix` specifies the signal name for the internal clock enable signal.

In some cases multiple clock enables are generated (for example, when a cascade block implementation for certain blocks is specified). In such cases, `EnablePrefix` specifies a base signal name for the first clock enable that is generated. For other clock enable signals, numeric tags are appended to `EnablePrefix` to form unique signal names. For example, the following code fragment illustrates two clock enables that were generated when `EnablePrefix` was set to 'test\_clk\_enable' :

```
COMPONENT mysys_tc
  PORT( clk           : IN   std_logic;
        reset        : IN   std_logic;
        clk_enable   : IN   std_logic;
        test_clk_enable : OUT  std_logic;
        test_clk_enable_5_1_0 : OUT  std_logic
  );
END COMPONENT;
```

# EntityConflictPostfix property

---

## **Purpose**

Specify string to append to duplicate VHDL entity or Verilog module names

## **Settings**

'string'

Default: '\_block'

The specified postfix resolves duplicate VHDL entity or Verilog module names.

For example, if the coder detects two entities with the name `MyFilt`, the coder names the first entity `MyFilt` and the second instance `MyFilt_block`.

## **See Also**

`PackagePostfix`, `ReservedWordPostfix`

# ForceClock property

---

## **Purpose**

Specify whether test bench forces clock input signals

## **Settings**

'on' (default)

### **Selected** (default)

Specify that the test bench forces the clock input signals. When this option is set, the clock high and low time settings control the clock waveform.

'off'

### **Cleared**

Specify that a user-defined external source forces the clock input signals.

## **See Also**

ClockLowTime, ClockHighTime, ForceClockEnable, ForceReset, HoldTime



<b>Purpose</b>	Specify whether test bench forces clock enable input signals
<b>Settings</b>	<p>'on' (default)</p> <p><b>Selected</b> (default)</p> <p>Specify that the test bench forces the clock enable input signals to active high (1) or active low (0), depending on the setting of the clock enable input value.</p> <p>'off'</p> <p><b>Cleared</b></p> <p>Specify that a user-defined external source forces the clock enable input signals.</p>
<b>See Also</b>	ClockHighTime, ClockLowTime, ForceClock, HoldTime

# ForceReset property

---

**Purpose** Specify whether test bench forces reset input signals

**Settings** 'on' (default)

**Selected** (default)

Specify that the test bench forces the reset input signals. If you enable this option, you can also specify a hold time to control the timing of a reset.

'off'

**Cleared**

Specify that a user-defined external source forces the reset input signals.

**See Also** ClockHighTime, ClockLowTime, ForceClock, HoldTime

## Purpose

Generate HDL Cosimulation block(s) for use in testing DUT

## Settings

'on'

If your installation includes one or more of the following HDL simulation features, the coder generates an HDL Cosimulation block for each:

- HDL Verifier for use with Mentor Graphics ModelSim
- HDL Verifier for use with Cadence Incisive

The coder configures the generated HDL Cosimulation blocks to conform to the port and data type interface of the DUT selected for code generation. By connecting an HDL Cosimulation block to your model in place of the DUT, you can cosimulate your design with the desired simulator.

The coder appends the string specified by the `CosimLibPostfix` property to the names of the generated HDL Cosimulation blocks.

'off' (default)

Do not generate HDL Cosimulation blocks.

# GenerateCoSimModel property

---

<b>Purpose</b>	Generate model containing HDL Cosimulation block for use in testing DUT
<b>Settings</b>	<p>'ModelSim' (default)</p> <p>If your installation includes HDL Verifier for use with Mentor Graphics ModelSim, the coder generates and opens a Simulink model that contains an HDL Cosimulation block for Mentor Graphics ModelSim.</p> <p>'Incisive'</p> <p>If your installation includes HDL Verifier for use with Cadence Incisive, the coder generates and opens a Simulink model that contains an HDL Cosimulation block for Cadence Incisive.</p>
<b>See Also</b>	“Generate a Cosimulation Model” on page 15-31

# GeneratedModelName property

---

**Purpose** Specify name of generated model

**Settings** 'string'

By default, the name of a generated model is the same as that of the original model. Assign a string value to `GeneratedModelName` to override the default.

**See Also** “Defaults and Options for Generated Models” on page 12-11

## GeneratedModelNamePrefix property

---

<b>Purpose</b>	Specify prefix to name of generated model
<b>Settings</b>	'string' Default: 'gm_' The specified string is prepended to the name of the generated model.
<b>See Also</b>	“Defaults and Options for Generated Models” on page 12-11

<b>Purpose</b>	Generate HDL code
<b>Settings</b>	'on' (default) Generate HDL code. 'off' Do not generate HDL code.
<b>See Also</b>	“Generating HDL Code Using the GUI”

# GenerateValidationModel property

---

**Purpose** Generate validation model with HDL code

**Settings** 'on'

Generate a validation model that highlights generated delays and other differences between your original model and the generated model. With a validation model, you can observe the effects of streaming, resource sharing, and delay balancing.

'off' (default)

Do not generate a validation model.

## **Usage Notes**

If you enable generation of a validation model, also enable delay balancing to keep the generated DUT model synchronized with the original DUT model. Mismatches between delays in the original DUT model and delays in the generated DUT model cause validation to fail.

You can also generate a validation model by selecting one of the following check boxes:

- **Generate validation model** in the **HDL Code** pane of the Model Configuration Parameters dialog box
- **Generate validation model** in the **Generate RTL Code and Testbench** task of the HDL Workflow Advisor

**See Also** “Delay Balancing” on page 13-34



**Purpose**

Include model Web view in the code generation report

**Settings**

'on'

Include model Web view in the code generation report.

'off' (default)

Omit model Web view in the code generation report.

**Usage  
Notes**

With a model Web view, you can click a link in the generated code to highlight the corresponding block in the model.

**See Also**

# HandleAtomicSubsystem property

---

**Purpose** Enable reusable code generation for identical atomic subsystems

**Settings** 'on' (default)  
Generate reusable code for identical atomic subsystems.  
'off'  
Do not generate reusable code for identical atomic subsystems.

**See Also** “Generate Reusable Code for Atomic Subsystems” on page 15-8

<b>Purpose</b>	Specify string written to initialization section of compilation script
<b>Settings</b>	'string' Default: 'vlib work\n'.
<b>See Also</b>	“Script Generation for EDA Tools” on page 18-2

## HDLCompileTerm property

---

**Purpose** Specify string written to termination section of compilation script

**Settings** 'string'  
The default is the null string ('').

**See Also** “Script Generation for EDA Tools” on page 18-2

# HDLCompileFilePostfix property

---

## **Purpose**

Specify postfix string appended to file name for generated Mentor Graphics ModelSim compilation scripts

## **Settings**

'string'

Default: '\_compile.do'.

For example, if the name of the device under test or test bench is `my_design`, the coder adds the postfix `_compile.do` to form the name `my_design_compile.do`.

# HDLCompileVerilogCmd property

---

**Purpose** Specify command string written to compilation script for Verilog files

**Settings** 'string'

Default: 'vlog %s %s\n'.

The two arguments are the contents of the 'SimulatorFlags' property and the file name of the current module. To omit the flags, set 'SimulatorFlags' to '' (the default).

**See Also** “Script Generation for EDA Tools” on page 18-2

# HDLCompileVHDLCmd property

---

**Purpose** Specify command string written to compilation script for VHDL files

**Settings** 'string'

Default: 'vcom %s %s\n'.

The two arguments are the contents of the 'SimulatorFlags' property and the file name of the current entity. To omit the flags, set 'SimulatorFlags' to '' (the default).

**See Also** “Script Generation for EDA Tools” on page 18-2

# HDLControlFiles property

---

## Purpose

Attach code generation control file to model

## Settings

{'string'}

Pass in a cell array containing a string that specifies a control file to be attached to the current model. Defaults are

- File name extension: `.m`
- Location of file: the control file must be on the MATLAB path or in the current working folder. Therefore you need only specify the file name; do not specify path information.

The following example specifies a control file, using the default for the file name extension.

```
makehdl(gcb, 'HDLControlFiles', {'dct8config'});
```

Specify a control file that is on the MATLAB path, or in the current working folder. You may need to modify the MATLAB path so that the desired control file is on the path before generating code. Then attach the control file to the model.

---

**Note** The current release supports specification of a single control file.

---

## Usage Notes

To clear the property (so that control files are not invoked during code generation), pass in a cell array containing the null string, as in the following example:

```
makehdl(gcb, 'HDLControlFiles', {''});
```

## See Also

For a detailed description of the structure and use of control files, see “Code Generation Control Objects and Methods” on page 22-8.



# HDLMapFilePostfix property

---

**Purpose** Specify postfix string appended to file name for generated mapping file

**Settings** 'string'

Default: '\_map.txt'.

For example, if the name of the device under test is `my_design`, the coder adds the postfix `_map.txt` to form the name `my_design_map.txt`.

## HDLSimCmd property

---

**Purpose** Specify simulation command written to simulation script

**Settings** 'string'

Default: 'vsim -novopt work.%s\n'.

The implicit argument is the top-level module or entity name.

**See Also** “Script Generation for EDA Tools” on page 18-2

**Purpose** Specify string written to initialization section of simulation script

**Settings** 'string'  
The default string is  
`['onbreak resume\n',...  
'onerror resume\n']`

**See Also** “Script Generation for EDA Tools” on page 18-2

# HDLSimFilePostfix property

---

**Purpose** Specify postfix string appended to file name for generated Mentor Graphics ModelSim simulation scripts

**Settings** 'string'  
Default: `_sim.do`.  
For example, if the name of your test bench file is `my_design`, the coder adds the postfix `_sim.do` to form the name `my_design_tb_sim.do`.

**Purpose** Specify string written to termination section of simulation script

**Settings** 'string'  
Default: 'run -a11\n'.

**See Also** “Script Generation for EDA Tools” on page 18-2

# HDLSimViewWaveCmd property

---

**Purpose** Specify waveform viewing command written to simulation script

**Settings** 'string'

Default: 'add wave sim:%s\n'

The implicit argument is the top-level module or entity name.

**See Also** “Script Generation for EDA Tools” on page 18-2

**Purpose** Specify command written to synthesis script

**Settings** 'string'

Default: none.

Your choice of synthesis tool (see HDLSynthTool) sets the synthesis command string. The default string is a format string passed to `fprintf` to write the `Cmd` section of the synthesis script. The implicit argument is the top-level module or entity name. The content of the string is specific to the selected synthesis tool.

**See Also** HDLSynthTool, “Script Generation for EDA Tools” on page 18-2

# HDLSynthFilePostfix property

---

**Purpose** Specify postfix string appended to file name for generated synthesis scripts

**Settings** 'string'

Default: The value of HDLSynthFilePostfix normally defaults to a string that corresponds to the synthesis tool that HDLSynthTool specifies.

For example, if the value of HDLSynthTool is 'Synplify', HDLSynthFilePostfix defaults to the string '\_synplify.tcl'. Then, if the name of the device under test is my\_design, the coder adds the postfix \_synplify.tcl to form the synthesis script file name my\_design\_synplify.tcl.

**See Also** HDLSynthTool, “Script Generation for EDA Tools” on page 18-2



**Purpose** Specify string written to initialization section of synthesis script

**Settings** 'string'

Default: none

Your choice of synthesis tool (see HDLSynthTool) sets the synthesis initialization string. The default string is a format string passed to `fprintf` to write the `Init` section of the synthesis script. The default string is a synthesis project creation command. The implicit argument is the top-level module or entity name. The content of the string is specific to the selected synthesis tool.

**See Also** HDLSynthTool, “Script Generation for EDA Tools” on page 18-2

# HDLSynthTerm property

---

**Purpose** Specify string written to termination section of synthesis script

**Settings** 'string'

Default: none

Your choice of synthesis tool (see HDLSynthTool) sets the synthesis termination string. The default string is a format string passed to `fprintf` to write the Term section of the synthesis script. The Term section does not take arguments. The content of the string is specific to the selected synthesis tool.

**See Also** HDLSynthTool, “Script Generation for EDA Tools” on page 18-2

## Purpose

Select synthesis tool for which the coder generates scripts.

## Settings

'string'

Default: 'None'.

HDLSynthTool enables or disables generation of scripts for third-party synthesis tools. By default, the coder does not generate a synthesis script. To generate a script for one of the supported synthesis tools, set HDLSynthTool to one of the following strings:

---

**Tip** The value of HDLSynthTool also sets the postfix string (HDLSynthFilePostfix) that the coder appends to generated synthesis script file names.

---

Choice of HDLSynthTool Value...	Generates Script For...	Sets HDLSynthFilePostfix To...
'None'	N/A; script generation disabled	N/A
'ISE'	Xilinx ISE	'_ise.tcl'
'Precision'	Mentor Graphics Precision	'_precision.tcl'
'Quartus'	Altera Quartus II	'_quartus.tcl'
'Synplify'	Synopsys Synplify Pro	'_synplify.tcl'

## See Also

HDLSynthFilePostfix, “Script Generation for EDA Tools” on page 18-2

# HierarchicalDistPipelining property

---

**Purpose** Specify whether or not to apply retiming across a subsystem hierarchy

**Settings** 'on'

Enable retiming across a subsystem hierarchy. The coder applies retiming hierarchically down, until it reaches a subsystem where **DistributedPipelining** is off.

'off' (default)

Distribute pipelining only within a subsystem.

**See Also** “DistributedPipelining” on page 9-66

# HighlightAncestors property

---

<b>Purpose</b>	Highlight ancestors of blocks in generated model that differ from original model
<b>Settings</b>	'on' (default) Highlight blocks in a generated model that differ from the original model, and their ancestor (parent) blocks in the model hierarchy. 'off' Highlight only the blocks in a generated model that differ from the original model without highlighting their ancestor (parent) blocks in the model hierarchy.
<b>See Also</b>	“Defaults and Options for Generated Models” on page 12-11

# HighlightColor property

---

**Purpose** Specify color for highlighted blocks in generated model

**Settings** 'string'  
Default: 'cyan'.  
Specify the color as one of the following color string values:

- 'cyan'
- 'yellow'
- 'magenta'
- 'red'
- 'green'
- 'blue'
- 'white'
- 'black'

**See Also** “Defaults and Options for Generated Models” on page 12-11

# HoldInputDataBetweenSamples property

---

## Purpose

Specify how long subrate signal values are held in valid state

## Settings

'on' (default)

Data values for subrate signals are held in a valid state across N base-rate clock cycles, where N is the number of base-rate clock cycles that elapse per subrate sample period. (N is  $\geq 2$ .)

'off'

Data values for subrate signals are held in a valid state for only one base-rate clock cycle. For the subsequent base-rate cycles, data is in an unknown state (expressed as 'X') until leading edge of the next subrate sample period.

## Usage Notes

In most cases, the default ('on') is the best setting for this property. This setting matches the behavior of a Simulink simulation, in which subrate signals are held valid through each base-rate clock period.

In some cases (for example modeling memory or memory interfaces), it is desirable to set `HoldInputDataBetweenSamples` to 'off'. In this way you can obtain diagnostic information about when data is in an invalid ('X') state.

## See Also

`HoldTime`, “Code Generation from Multirate Models” on page 10-2

# HoldTime property

---

**Purpose** Specify hold time for input signals and forced reset input signals

**Settings** ns

Default: 2

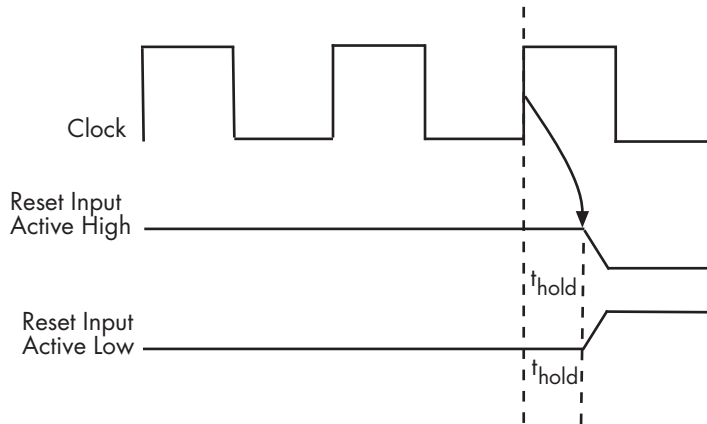
Specify the number of nanoseconds during which the model's data input signals and forced reset input signals are held past the clock rising edge.

The hold time is expressed as a positive integer.

This option applies to reset input signals only if forced resets are enabled.

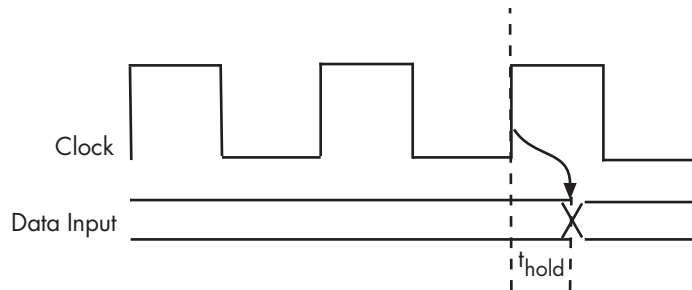
## Usage Notes

The hold time is the amount of time that reset input signals and input data are held past the clock rising edge. The following figures show the application of a hold time ( $t_{\text{hold}}$ ) for reset and data input signals when the signals are forced to active high and active low.



**Hold Time for Reset Input Signals**





## Hold Time for Data Input Signals

---

**Note** A reset signal is always asserted for two cycles plus  $t_{hold}$ .

---

## See Also

ClockHighTime, ClockLowTime, ForceClock

# IgnoreDataChecking property

---

<b>Purpose</b>	Specify number of samples during which output data checking is suppressed
<b>Settings</b>	<p>N</p> <p>Default: 0.</p> <p>N must be a positive integer.</p> <p>When <math>N &gt; 0</math>, the test bench suppresses output data checking for the first N output samples after the clock enable output (<code>ce_out</code>) is asserted.</p>
<b>Usage Notes</b>	<p>When using pipelined block implementations, output data may be in an invalid state for some number of samples. To avoid spurious test bench errors, determine this number and set <code>IgnoreDataChecking</code> accordingly.</p> <p>Be careful to specify N as a number of samples, not as a number of clock cycles. For a single-rate model, these are equivalent, but they are not equivalent for a multirate model.</p> <p>You should use <code>IgnoreDataChecking</code> in cases where there is a state (register) initial condition in the HDL code that does not match the Simulink state, including the following specific cases:</p> <ul style="list-style-type: none"><li>• When you specify the <code>'DistributedPipelining', 'on'</code> parameter for the MATLAB Function block (see “Distributed Pipeline Insertion for MATLAB Function Blocks” on page 17-42).</li><li>• When you specify the <code>'ResetType', 'None'</code> parameter (see “ResetType” on page 9-92 ) for the following block types:<ul style="list-style-type: none"><li>▪ <code>commcnvtrlv2/Convolutional Deinterleaver</code></li><li>▪ <code>commcnvtrlv2/Convolutional Interleaver</code></li><li>▪ <code>commcnvtrlv2/General Multiplexed Deinterleaver</code></li><li>▪ <code>commcnvtrlv2/General Multiplexed Interleaver</code></li><li>▪ <code>dspsigops/Delay</code></li></ul></li></ul>

- simulink/Additional Math & Discrete/Additional Discrete/Unit Delay Enabled
- simulink/Commonly Used Blocks/Unit Delay
- simulink/Discrete/Delay
- simulink/Discrete/Memory
- simulink/Discrete/Tapped Delay
- simulink/User-Defined Functions/MATLAB Function
- sflib/Chart
- sflib/Truth Table
- When generating a black box interface to existing manually-written HDL code.

# InitializeBlockRAM property

---

**Purpose** Enable or suppress generation of initial signal value for RAM blocks

**Settings** 'on' (default)

For RAM blocks, generate initial values of '0' for both the RAM signal and the output temporary signal.

'off'

For RAM blocks, do not generate initial values for either the RAM signal or the output temporary signal.

**Usage Notes** This property applies to RAM blocks in the `hdlDemoLib` library (see also “RAM Blocks” on page 11-3). The library provides three type of RAM blocks:

- Dual Port RAM
- Simple Dual Port RAM
- Single Port RAM

**See Also**

`IgnoreDataChecking`

# InitializeTestBenchInputs property

---

**Purpose** Specify initial value driven on test bench inputs before data is asserted to DUT

**Settings**

- 'on'
- Initial value driven on test bench inputs is '0'.
- 'off' (default)
- Initial value driven on test bench inputs is 'X' (unknown).

# InlineConfigurations property

---

**Purpose** Specify whether generated VHDL code includes inline configurations

**Settings** 'on' (default)

**Selected** (default)

Include VHDL configurations in files that instantiate a component.

'off'

**Cleared**

Suppress the generation of configurations and require user-supplied external configurations. Use this setting if you are creating your own VHDL configuration files.

**Usage Notes** VHDL configurations can be either inline with the rest of the VHDL code for an entity or external in separate VHDL source files. By default, the coder includes configurations for a model within the generated VHDL code. If you are creating your own VHDL configuration files, you should suppress the generation of inline configurations.

**See Also** LoopUnrolling, SafeZeroConcat, UseAggregatesForConst, UseRisingEdge

**Purpose**

Inline HDL code for MATLAB Function blocks

**Settings**

'on'

Inline HDL code for MATLAB Function blocks to avoid instantiation of code for custom blocks.

'off' (default)

Instantiate HDL code for MATLAB Function blocks and do not inline.

**Examples**

Enable inlining of HDL code:

```
mdl = 'my_custom_block_model';  
hdlset_param(mdl, 'InlineMATLABBlockCode', 'on');
```

Enable instantiation of HDL code:

```
mdl = 'my_custom_block_model';  
hdlset_param(mdl, 'InlineMATLABBlockCode', 'off');
```

# InputType property

---

## **Purpose**

Specify HDL data type for model's input ports

## **Settings**

Default (for VHDL): 'std\_logic\_vector'

Default (for VHDL): **std\_logic\_vector**

Specifies VHDL type STD\_LOGIC\_VECTOR for the model's input ports.

'signed/unsigned'

**signed/unsigned**

Specifies VHDL type SIGNED or UNSIGNED for the model's input ports.

'wire' (Verilog)

**wire** (Verilog)

If the target language is Verilog, the data type for all ports is wire. This property is not modifiable in this case.

## **See Also**

ClockEnableInputPort, OutputType



# InstanceGenerateLabel property

---

**Purpose** Specify string to append to instance section labels in VHDL GENERATE statements

**Settings** 'string'  
Default: '\_gen'  
Specify a postfix string to append to instance section labels in VHDL GENERATE statements.

**See Also** BlockGenerateLabel, OutputGenerateLabel

# InstancePostfix property

---

**Purpose** Specify string appended to generated component instance names

**Settings** 'string'  
Default: '' (no postfix appended)  
Specify a string to be appended to component instance names in generated code.

**Purpose** Specify string prefixed to generated component instance names

**Settings** 'string'  
Default: 'u\_'  
Specify a string to be prefixed to component instance names in generated code.

# LoopUnrolling property

---

<b>Purpose</b>	Specify whether VHDL FOR and GENERATE loops are unrolled and omitted from generated VHDL code
<b>Settings</b>	<p>'on'</p> <p><b>Selected</b></p> <p>Unroll and omit FOR and GENERATE loops from the generated VHDL code.</p> <p>In Verilog code, loops are always unrolled.</p> <p>If you are using an electronic design automation (EDA) tool that does not support GENERATE loops, you can enable this option to omit loops from your generated VHDL code.</p> <p>'off' (default)</p> <p><b>Cleared</b> (default)</p> <p>Include FOR and GENERATE loops in the generated VHDL code.</p>
<b>Usage Notes</b>	The setting of this option does not affect results obtained from simulation or synthesis of generated VHDL code.
<b>See Also</b>	InlineConfigurations, SafeZeroConcat, UseAggregatesForConst, UseRisingEdge

# MaskParameterAsGeneric property

---

## Purpose

Generate reusable HDL code for subsystems with identical mask parameters that differ only in value

## Settings

'on'

Generate one HDL file for multiple masked subsystems with different values for tunable mask parameters. The coder automatically detects atomic subsystems with tunable mask parameters that are sharable.

Inside the subsystem, you can use the mask parameter only in the following blocks and parameters:

Block	Parameter	Limitation
Constant	<b>Constant value</b> on the Main tab of the dialog box	None
Gain	<b>Gain</b> on the Main tab of the dialog box	<b>Parameter data type</b> should be the same for all Gain blocks.

'off' (default)

Generate a separate HDL file for each masked subsystem.

# RAMArchitecture property

---

**Purpose** Select RAM architecture with clock enable, or without clock enable, for all RAMs in DUT subsystem

**Settings** 'WithClockEnable' (default)  
Generate RAMs with clock enable.  
'WithoutClockEnable'  
Generate RAMs without clock enable.

# MinimizeClockEnables property

## Purpose

Omit generation of clock enable logic for single-rate designs

## Settings

'on'

Omit generation of clock enable logic for single-rate designs, wherever possible (see “Usage Notes” on page 23-67). The following VHDL code example does not define or examine a clock enable signal. When the clock signal (clk) goes high, the current signal value is output.

```
Unit_Delay_process : PROCESS (clk, reset)
BEGIN
    IF reset = '1' THEN
        Unit_Delay_out1 <= to_signed(0, 32);
    ELSIF clk'EVENT AND clk = '1' THEN
        Unit_Delay_out1 <= In1_signed;
    END IF;
END PROCESS Unit_Delay_process;
```

'off' (default)

Generate clock enable logic. The following VHDL code extract represents a register with a clock enable (enb)

```
Unit_Delay_process : PROCESS (clk, reset)
BEGIN
    IF reset = '1' THEN
        Unit_Delay_out1 <= to_signed(0, 32);
    ELSIF clk'EVENT AND clk = '1' THEN
        IF enb = '1' THEN
            Unit_Delay_out1 <= In1_signed;
        END IF;
    END IF;
END PROCESS Unit_Delay_process;
```

## Usage Notes

In some cases, the coder emits clock enables even when MinimizeClockEnables is 'on'. These cases are:

- Registers inside Enabled, State-Enabled, and Triggered subsystems.

# MinimizeClockEnables property

---

- Multirate models.
- The coder emits clock enables for the following blocks:
  - commseqgen2/PN Sequence Generator
  - dspsigops/NCO
  - dspsrcs4/Sine Wave
  - hlldemolib/HDL FFT
  - built-in/DiscreteFir
  - dspmlti4/CIC Decimation
  - dspmlti4/CIC Interpolation
  - dspmlti4/FIR Decimation
  - dspmlti4/FIR Interpolation
  - dspadpt3/LMS Filter
  - dsparch4/Biquad Filter
  - dsparch4/Digital Filter



# MinimizeIntermediateSignals property

---

## Purpose

Specify whether to optimize HDL code for debuggability or code coverage

## Settings

'on'

Optimize for code coverage by minimizing intermediate signals. For example, suppose that the generated code with this setting *off* is:

```
const3 <= to_signed(24, 7);
subtractor_sub_cast <= resize(const3, 8);
subtractor_sub_cast_1 <= resize(delayout, 8);
subtractor_sub_temp <= subtractor_sub_cast - subtractor_sub_cast_1;
```

With this setting *on*, the output code is optimized to:

```
subtractor_sub_temp <= 24 - (resize(delayout, 8));
```

The intermediate signals `const3`, `subtractor_sub_cast`, and `subtractor_sub_cast_1` are removed.

'off' (default)

Optimize for debuggability by preserving intermediate signals.

# MulticyclePathInfo property

---

**Purpose** Generate text file that reports multicycle path constraint information, for use with synthesis tools.

**Settings** 'on'

**Selected**

Generate a multicycle path information file.

'off' (default)

Do not generate a multicycle path information file.

**Usage  
Notes**

The file name for the multicycle path information file derives from the name of the DUT and the postfix string '\_constraints', as follows:

*DUTname\_constraints.txt*

For example, if the DUT name is `symmetric_fir`, the name of the multicycle path information file is `symmetric_fir_constraints.txt`.

**See Also** “Generate Multicycle Path Information Files” on page 10-16

## Purpose

Divide generated test bench into helper functions, data, and HDL test bench code files

## Settings

'on'

Write separate files for test bench code, helper functions, and test bench data. The file names are derived from the name of the DUT, the TestBenchPostfix property, and the TestBenchDataPostfix property as follows:

*DUTname\_TestBenchPostfix\_TestBenchDataPostfix*

For example, if the DUT name is `symmetric_fir`, and the target language is VHDL, the default test bench file names are:

- `symmetric_fir_tb.vhd`: test bench code
- `symmetric_fir_tb_pkg.vhd`: helper functions package
- `symmetric_fir_tb_data.vhd`: data package

If the DUT name is `symmetric_fir` and the target language is Verilog, the default test bench file names are:

- `symmetric_fir_tb.v`: test bench code
- `symmetric_fir_tb_pkg.v`: helper functions package
- `symmetric_fir_tb_data.v`: test bench data

'off' (default)

Write a single test bench file containing the HDL test bench code and helper functions and test bench data.

## See Also

TestBenchPostFix, TestBenchDataPostFix

# OptimizationReport property

---

<b>Purpose</b>	Display HTML optimization report
<b>Settings</b>	'on ' Create and display an HTML optimization report. 'off ' (default) Do not create an HTML optimization report.
<b>See Also</b>	“Create and Use Code Generation Reports” on page 14-2

# OptimizeTimingController property

---

## Purpose

Optimize timing controller entity for speed and code size by implementing separate counters per rate

## Settings

'on' (default)

A timing controller code file is generated if required by the design, for example:

- When code is generated for a multirate model.
- When a cascade block implementation for certain blocks is specified.

This file contains a module defining timing signals (clock, reset, external clock enable inputs and clock enable output) in a separate entity or module. In a multirate model, the timing controller entity generates the required rates from a single master clock using one or more counters and multiple clock enables.

When `OptimizeTimingController` is set 'on' (the default), the coder generates multiple counters (one counter for each rate in the model). The benefit of this optimization is that it generates faster logic, and the size of the generated code is usually much smaller.

'off'

When `OptimizeTimingController` is set 'off', the timing controller uses one counter to generate the rates in the model.

## See Also

“Code Generation from Multirate Models” on page 10-2, `EnablePrefix`, `TimingControllerPostfix`

# OutputGenerateLabel property

---

**Purpose** Specify string that labels output assignment block for VHDL GENERATE statements

**Settings** 'string'  
Default: 'outputgen'  
Specify a postfix string to append to output assignment block labels in VHDL GENERATE statements.

**See Also** BlockGenerateLabel, OutputGenerateLabel

**Purpose**

Specify HDL data type for model's output ports

**Settings**

'Same as input data type' (VHDL default)

**Same as input data type** (VHDL default)

Output ports have the same type as the specified input port type.

'std\_logic\_vector'

**std\_logic\_vector**

Output ports have VHDL type STD\_LOGIC\_VECTOR.

'signed/unsigned'

**signed/unsigned**

Output ports have type SIGNED or UNSIGNED.

'wire' (Verilog)

**wire** (Verilog)

If the target language is Verilog, the data type for all ports is wire. This property is not modifiable in this case.

**See Also**

ClockEnableInputPort, InputType

# Oversampling property

---

**Purpose** Specify frequency of global oversampling clock as a multiple of the model's base rate

**Settings** N

Default: 1.

N must be an integer greater than or equal to 0.

Oversampling specifies N, the *oversampling factor* of a global oversampling clock. The oversampling factor expresses the global oversampling clock rate as a multiple of your model's base rate.

When you specify an oversampling factor greater than 1, the coder generates the global oversampling clock and derives the required timing signals from the clock signal. By default, the coder does not generate a global oversampling clock.

Generation of the global oversampling clock affects only generated HDL code. The clock does not affect the simulation behavior of your model.

If you want to generate a global oversampling clock:

- The oversampling factor must be an integer greater than or equal to 1.
- In a multirate DUT, the other rates in the DUT must divide evenly into the global oversampling rate.

**See Also** "Generate a Global Oversampling Clock" on page 10-9



**Purpose** Specify string to append to specified model or subsystem name to form name of package file

**Settings** 'string'  
Default: '\_pkg'  
The coder applies this option only if a package file is required for the design.

**See Also** ClockProcessPostfix, EntityConflictPostfix,  
ReservedWordPostfix

# PipelinePostfix property

---

**Purpose** Specify string to append to names of input or output pipeline registers generated for pipelined block implementations

**Settings** 'string'

Default: '\_pipe'

When you specify a generation of input and/or output pipeline registers for selected blocks, the coder appends the string specified by the PipelinePostfix property when generating code for such pipeline registers.

For example, suppose you specify a pipelined output implementation for a Product block in a model, as in the following code:

```
hdlset_param('sfir_fixed/symmetric_fir/Product','OutputPipeline', 2')
```

The following makehdl command specifies that the coder appends 'testpipe' to generated pipeline register names.

```
makehdl(gcs, 'PipelinePostfix', 'testpipe');
```

The following excerpt from generated VHDL code shows process the PROCESS code, with postfixed identifiers, that implements two pipeline stages:

```
Product_outtestpipe_process : PROCESS (clk, reset)
BEGIN
    IF reset = '1' THEN
        Product_outtestpipe_reg <= (OTHERS => to_signed(0, 33));
    ELSIF clk'EVENT AND clk = '1' THEN
        IF enb = '1' THEN
            Product_outtestpipe_reg(0) <= Product_out1;
            Product_outtestpipe_reg(1) <= Product_outtestpipe_reg(0);
        END IF;
    END IF;
END PROCESS Product_outtestpipe_process;
```

**See Also**

“Block Implementation Parameters” on page 9-49, “InputPipeline” on page 9-78, “OutputPipeline” on page 9-85

# RAMMappingThreshold property

---

**Purpose** Specify the minimum RAM size required for mapping to RAMs instead of registers

**Settings** N

Default: 256.

N must be an integer greater than or equal to 0.

RAMMappingThreshold defines the minimum RAM size required for mapping to RAMs instead of registers. This threshold applies to:

- Delay blocks
- Persistent variables in MATLAB Function blocks

## Example

To change the RAM mapping threshold for a model, use the `hdlset_param` function. For example:

```
hdlset_param('sfir_fixed', 'RAMMappingThreshold', 1024);
```

That command sets the threshold for the `sfir_fixed` model to 1024 bits.

## See Also

- “UseRAM” on page 9-96 in the HDL Coder documentation
- “MapPersistentVarsToRAM” on page 9-81 in the HDL Coder documentation

# RequirementComments property

---

<b>Purpose</b>	Enable or disable generation of hyperlinked requirements comments in HTML code generation reports
<b>Settings</b>	<p>'on' (default)</p> <p>If the model includes requirements comments, generate hyperlinked requirements comments within the HTML code generation report. The comments link to the corresponding requirements documents.</p> <p>'off'</p> <p>When generating an HTML code generation report, render requirements as comments within the generated code</p>
<b>See Also</b>	“Create and Use Code Generation Reports” on page 14-2, “Generate Code with Annotations or Comments” on page 14-27, Traceability

# ReservedWordPostfix property

---

**Purpose** Specify string appended to identifiers for entities, signals, constants, or other model elements that conflict with VHDL or Verilog reserved words

**Settings** 'string'  
Default: '\_rsvd'.  
The reserved word postfix is applied identifiers (for entities, signals, constants, or other model elements) that conflict with VHDL or Verilog reserved words. For example, if your generating model contains a signal named `mod`, the coder adds the postfix `_rsvd` to form the name `mod_rsvd`.

**See Also** `ClockProcessPostfix`, `EntityConflictPostfix`,  
`ReservedWordPostfix`

## Purpose

Specify asserted (active) level of reset input signal

## Settings

'active-high' (default)

### Active-high (default)

Specify that the reset input signal must be driven high (1) to reset registers in the model. For example, the following code fragment checks whether reset is active high before populating the delay\_pipeline register:

```
Delay_Pipeline_Process : PROCESS (clk, reset)
BEGIN
    IF reset = '1' THEN
        delay_pipeline(0 TO 50) <= (OTHERS => (OTHERS => '0'));
    .
    .
    .
```

'active-low'

### Active-low

Specify that the reset input signal must be driven low (0) to reset registers in the model. For example, the following code fragment checks whether reset is active low before populating the delay\_pipeline register:

```
Delay_Pipeline_Process : PROCESS (clk, reset)
BEGIN
    IF reset = '0' THEN
        delay_pipeline(0 TO 50) <= (OTHERS => (OTHERS => '0'));
    .
    .
    .
```

## See Also

ResetType

# ResetInputPort property

---

**Purpose** Name HDL port for model's reset input

**Settings** 'string'

Default: 'reset'.

The string specifies the name for the model's reset input port. If you override the default with (for example) the string 'chip\_reset' for the generating system `myfilter`, the generated entity declaration might look as follows:

```
ENTITY myfilter IS
  PORT( clk          : IN  std_logic;
        clk_enable   : IN  std_logic;
        chip_reset    : IN  std_logic;
        myfilter_in   : IN  std_logic_vector (15 DOWNTO 0);
        myfilter_out  : OUT std_logic_vector (15 DOWNTO 0);
        );
END myfilter;
```

If you specify a string that is a VHDL or Verilog reserved word, the code generator appends a reserved word postfix string to form a valid VHDL or Verilog identifier. For example, if you specify the reserved word `signal`, the resulting name string would be `signal_rsvd`. See `ReservedWordPostfix` for more information.

## Usage Notes

If the reset asserted level is set to active high, the reset input signal is asserted active high (1) and the input value must be high (1) for the entity's registers to be reset. If the reset asserted level is set to active low, the reset input signal is asserted active low (0) and the input value must be low (0) for the entity's registers to be reset.

**See Also** `ClockEnableInputPort`, `InputType`, `OutputType`



## Purpose

Define length of time (in clock cycles) during which reset is asserted

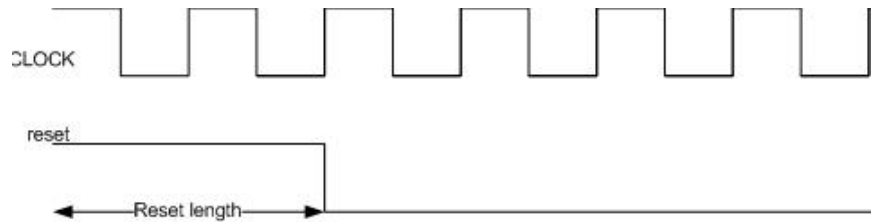
## Settings

N

Default: 2.

N must be an integer greater than or equal to 0.

Resetlength defines N, the number of clock cycles during which reset is asserted. The following figure illustrates the default case, in which the reset signal (active-high) is asserted for 2 clock cycles.



# ResetType property

---

## Purpose

Specify whether to use asynchronous or synchronous reset logic when generating HDL code for registers

## Settings

'async' (default)

### Asynchronous (default)

Use asynchronous reset logic. The following process block, generated by a Unit Delay block, illustrates the use of asynchronous resets. When the reset signal is asserted, the process block performs a reset, without checking for a clock event.

```
Unit_Delay1_process : PROCESS (clk, reset)
BEGIN
    IF reset = '1' THEN
        Unit_Delay1_out1 <= (OTHERS => '0');
    ELSIF clk'event AND clk = '1' THEN
        IF clk_enable = '1' THEN
            Unit_Delay1_out1 <= signed(x_in);
        END IF;
    END IF;
END PROCESS Unit_Delay1_process;
```

'sync'

### Synchronous

Use synchronous reset logic. Code for a synchronous reset follows. The following process block, generated by a Unit Delay block, checks for a clock event, the rising edge, before performing a reset:

```
Unit_Delay1_process : PROCESS (clk)
BEGIN
    IF rising_edge(clk) THEN
        IF reset = '1' THEN
            Unit_Delay1_out1 <= (OTHERS => '0');
        ELSIF clk_enable = '1' THEN
```

```
        Unit_Delay1_out1 <= signed(x_in);  
    END IF;  
END IF;  
END PROCESS Unit_Delay1_process;
```

**See Also**      [ResetAssertedLevel](#)

# ResourceReport property

---

<b>Purpose</b>	Display HTML resource utilization report
<b>Settings</b>	'on' Create and display an HTML resource utilization report (bill of materials). 'off' (default) Do not create an HTML resource utilization report.
<b>See Also</b>	“Create and Use Code Generation Reports” on page 14-2

<b>Purpose</b>	Specify syntax for concatenated zeros in generated VHDL code
<b>Settings</b>	'on' (default) <b>Selected</b> (default) Use the type-safe syntax, '0' & '0', for concatenated zeros. Typically, this syntax is preferred. 'off' <b>Cleared</b> Use the syntax "000000..." for concatenated zeros. This syntax can be easier to read and is more compact, but it can lead to ambiguous types.
<b>See Also</b>	LoopUnrolling, UseAggregatesForConst, UseRisingEdge

# ScalarizePorts property

## Purpose

Flatten vector ports into structure of scalar ports in VHDL code

## Settings

'on'

When generating code for a vector port, generate a structure of scalar ports

'off' (default)

Do not generate a structure of scalar ports for a vector port.

## Usage Notes

The ScalarizePorts property lets you control how the coder generates VHDL code for vector ports.

For example, consider the subsystem `vsum` in the following figure.



By default, `ScalarizePorts` is 'off'. The coder generates a type definition and port declaration for the vector port `In1` like the following:

```
PACKAGE simplevectorsum_pkg IS
  TYPE vector_of_std_logic_vector16 IS ARRAY (NATURAL RANGE <>)
    OF std_logic_vector(15 DOWNT0 0);
  TYPE vector_of_signed16 IS ARRAY (NATURAL RANGE <>) OF signed(15 DOWNT0 0);
END simplevectorsum_pkg;
.
.
.
ENTITY vsum IS
  PORT( In1      : IN    vector_of_std_logic_vector16(0 TO 9); -- int16 [10]
        Out1     : OUT   std_logic_vector(19 DOWNT0 0)  -- sfix20
```

```
);  
END vsum;
```

Under VHDL typing rules two types declared in this manner are not compatible across design units. This may cause problems if you need to interface two or more generated VHDL code modules.

You can flatten such a vector port into a structure of scalar ports by enabling `ScalarizePorts` in your `makehdl` command, as in the following example.

```
makehdl(gcs, 'ScalarizePorts', 'on')
```

The listing below shows the generated ports.

```
ENTITY vsum IS  
  PORT( In1_0      : IN   std_logic_vector(15 DOWNT0 0); -- int16  
        In1_1      : IN   std_logic_vector(15 DOWNT0 0); -- int16  
        In1_2      : IN   std_logic_vector(15 DOWNT0 0); -- int16  
        In1_3      : IN   std_logic_vector(15 DOWNT0 0); -- int16  
        In1_4      : IN   std_logic_vector(15 DOWNT0 0); -- int16  
        In1_5      : IN   std_logic_vector(15 DOWNT0 0); -- int16  
        In1_6      : IN   std_logic_vector(15 DOWNT0 0); -- int16  
        In1_7      : IN   std_logic_vector(15 DOWNT0 0); -- int16  
        In1_8      : IN   std_logic_vector(15 DOWNT0 0); -- int16  
        In1_9      : IN   std_logic_vector(15 DOWNT0 0); -- int16  
        Out1       : OUT  std_logic_vector(19 DOWNT0 0) -- sfix20  
  );  
END vsum;
```

## See Also

“Generate Interfaces for Referenced Models” on page 15-17

# SimulatorFlags property

---

<b>Purpose</b>	Specify simulator flags to apply to generated compilation scripts
<b>Settings</b>	'string' Default: '' Specify options that are specific to your application and the simulator you are using. For example, if you must use the 1076–1993 VHDL compiler, specify the flag <code>-93</code> .
<b>Usage Notes</b>	The flags you specify with this option are added to the compilation command in generated compilation scripts. The simulation command string is specified by the <code>HDLCCompileVHDLCmd</code> or <code>HDLCCompileVerilogCmd</code> properties.



# SplitArchFilePostfix property

---

<b>Purpose</b>	Specify string to append to specified name to form name of file containing model's VHDL architecture
<b>Settings</b>	'string' Default: '_arch'. This option applies only if you direct the coder to place the generated VHDL entity and architecture code in separate files.
<b>Usage Notes</b>	The option applies only if you direct the coder to place the filter's entity and architecture in separate files.
<b>See Also</b>	SplitEntityArch, SplitEntityFilePostfix

# SplitEntityArch property

---

**Purpose** Specify whether generated VHDL entity and architecture code is written to single VHDL file or to separate files

**Settings** 'on'

**Selected**

Write the generated VHDL code to a single file.

'off' (default)

**Cleared** (default)

Write the code for the generated VHDL entity and architecture to separate files.

The names of the entity and architecture files derive from the base file name (as specified by the generating model or subsystem name). By default, postfix strings identifying the file as an entity (`_entity`) or architecture (`_arch`) are appended to the base file name. You can override the default and specify your own postfix string.

For example, instead of all generated code residing in `MyFIR.vhd`, you can specify that the code reside in `MyFIR_entity.vhd` and `MyFIR_arch.vhd`.

---

**Note** This property is specific to VHDL code generation. It does not apply to Verilog code generation and should not be enabled when generating Verilog code.

---

**See Also** `SplitArchFilePostfix`, `SplitEntityFilePostfix`

# SplitEntityFilePostfix property

---

**Purpose**

Specify string to append to specified model name to form name of generated VHDL entity file

**Settings**

'string'

Default: '\_entity'

This option applies only if you direct the coder to place the generated VHDL entity and architecture code in separate files.

**See Also**

SplitArchFilePostfix, SplitEntityArch

# TargetDirectory property

---

**Purpose** Identify folder into which the coder writes generated output files.

**Settings** 'string'  
Default: 'hdlsrc'  
Specify a subfolder under the current working folder into which the coder writes generated files. The string can specify a complete path name.  
If the target folder does not exist, the coder creates it.

**See Also** VerilogFileExtension, VHDLFileExtension

**Purpose**

Specify HDL language to use for generated code

**Settings**

'VHDL' (default)

**VHDL** (default)

Generate VHDL code.

'verilog'

**Verilog**

Generate Verilog code.

The generated HDL code complies with the following standards:

- VHDL-1993 (IEEE® 1076-1993) or later
- Verilog-2001 (IEEE 1364-2001) or later

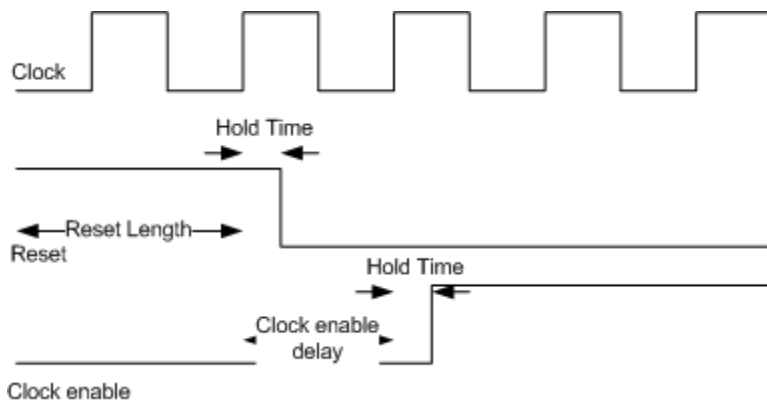
# TestBenchClockEnableDelay property

**Purpose** Define elapsed time (in clock cycles) between deassertion of reset and assertion of clock enable

**Settings** N (integer number of clock cycles) Default: 1

The TestBenchClockEnableDelay property specifies a delay time N, expressed in base-rate clock cycles ( the default value is 1) elapsed between the time the reset signal is deasserted and the time the clock enable signal is first asserted. TestBenchClockEnableDelay works in conjunction with the HoldTime property; After deassertion of reset, the clock enable goes high after a delay of N base-rate clock cycles plus the delay specified by HoldTime.

In the figure below, the reset signal (active-high) deasserts after the interval labelled Hold Time. The clock enable asserts after a further interval labelled Clock enable delay.



**See Also** HoldTime, ResetLength

# TestBenchDataPostFix property

---

## Purpose

Specify suffix added to test bench data file name when generating multi-file test bench

## Settings

'string'

Default: '\_data'.

The coder applies `TestBenchDataPostFix` only when generating a multi-file test bench (i.e. when `MultifileTestBench` is set 'on').

For example, if the name of your DUT is `my_test`, and `TestBenchPostFix` has the default value `_tb`, the coder adds the postfix `_data` to form the test bench data file name `my_test_tb_data`.

## See Also

`MultifileTestBench`, `TestBenchPostFix`

## TestBenchPostFix property

---

**Purpose** Specify suffix to test bench name

**Settings** 'string'

Default: '\_tb'.

For example, if the name of your DUT is `my_test`, the coder adds the postfix `_tb` to form the name `my_test_tb`.

**See Also** `MultifileTestBench`, `TestBenchDataPostFix`



# TimingControllerPostfix property

---

## Purpose

Specify suffix appended to DUT name to form timing controller name

## Settings

'string'

Default: '\_tc'.

A timing controller code file is generated if required by the design, for example:

- When code is generated for a multirate model.
- When a cascade block implementation for certain blocks is specified.

The timing controller name derives from the name of the subsystem that is selected for code generation (the DUT) as `DUTname+TimingControllerPostfix`. For example, if the name of your DUT is `my_test`, in the default case the coder adds the postfix `_tc` to form the timing controller name `my_test_tc`.

## See Also

`OptimizeTimingController`, “Code Generation from Multirate Models” on page 10-2

# TestBenchReferencePostFix property

---

**Purpose** Specify string appended to names of reference signals generated in test bench code

**Settings** 'string'  
Default: '\_ref'.  
Reference signal data is represented as arrays in the generated test bench code. The string specified by TestBenchReferencePostFix is appended to the generated signal names.

<b>Purpose</b>	Enable or disable creation of HTML code generation report with code-to-model and model-to-code hyperlinks
<b>Settings</b>	'on' Create and display an HTML code generation report. 'off' (default) Do not create an HTML code generation report.
<b>Usage Notes</b>	You can use the RequirementComments property to generate hyperlinked requirements comments within the HTML code generation report. The requirements comments link to the corresponding requirements documents for your model.
<b>See Also</b>	“Create and Use Code Generation Reports” on page 14-2, “Generate Code with Annotations or Comments” on page 14-27 , RequirementComments

# UseAggregatesForConst property

---

**Purpose** Specify whether constants are represented by aggregates, including constants that are less than 32 bits

**Settings** 'on'

**Selected**

Specify that constants, including constants that are less than 32 bits, be represented by aggregates. The following VHDL code show a scalar less than 32 bits represented as an aggregate:

```
GainFactor_gainparam <= (14 => '1', OTHERS => '0');
```

'off' (default)

**Cleared**(default)

Specify that the coder represent constants less than 32 bits as scalars and constants greater than or equal to 32 bits as aggregates. The following VHDL code was generated by default for a value less than 32 bits:

```
GainFactor_gainparam <= to_signed(16384, 16);
```

**See Also** [LoopUnrolling](#), [SafeZeroConcat](#), [UseRisingEdge](#)

## Purpose

Specify comment line in header of generated HDL and test bench files

## Settings

'string'

The comment is generated in each of the generated code and test bench files. The code generator adds leading comment characters for the target language. When newlines or line feeds are included in the string, the code generator emits single-line comments for each newline.

For example, the following `makehdl` command adds two comment lines to the header in a generated VHDL file.

```
makehdl(gcb,'UserComment','This is a comment line.\nThis is a second line.')
```

The resulting header comment block for subsystem `symmetric_fir` would appear as follows:

```
-----  
--  
-- Module: symmetric_fir  
-- Simulink Path: sfir_fixed/symmetric_fir  
-- Created: 2006-11-20 15:55:25  
-- Hierarchy Level: 0  
--  
-- This is a comment line.  
-- This is a second line.  
--  
-- Simulink model description for sfir_fixed:  
-- This model shows how to use HDL Coder to check, generate,  
-- and verify HDL for a fixed-point symmetric FIR filter.  
--  
-----
```

# UseRisingEdge property

---

## Purpose

Specify VHDL coding style used to check for rising edges when operating on registers

## Settings

'on'

### Selected

Use the VHDL `rising_edge` function to check for rising edges when operating on registers. The following code, generated from a Unit Delay block, tests `rising_edge` as shown in the following PROCESS block:

```
Unit_Delay1_process : PROCESS (clk, reset)
BEGIN
    IF reset = '1' THEN
        Unit_Delay1_out1 <= (OTHERS => '0');
    ELSIF rising_edge(clk) THEN
        IF clk_enable = '1' THEN
            Unit_Delay1_out1 <= signed(x_in);
        END IF;
    END IF;
END PROCESS Unit_Delay1_process;
```

'off' (default)

### Cleared(default)

Check for clock events when operating on registers. The following code, generated from a Unit Delay block, checks for a clock event as shown in the ELSIF statement of the following PROCESS block:

```
Unit_Delay1_process : PROCESS (clk, reset)
BEGIN
    IF reset = '1' THEN
        Unit_Delay1_out1 <= (OTHERS => '0');
    ELSIF clk'event AND clk = '1' THEN
        IF clk_enable = '1' THEN
```

```
        Unit_Delay1_out1 <= signed(x_in);  
    END IF;  
END IF;  
END PROCESS Unit_Delay1_process;
```

## Usage Notes

The two coding styles have different simulation behavior when the clock transitions from 'X' to '1'.

## See Also

LoopUnrolling, SafeZeroConcat, UseAggregatesForConst

# UseVerilogTimescale property

---

<b>Purpose</b>	Use compiler <code>`timescale</code> directives in generated Verilog code
<b>Settings</b>	<code>'on'</code> (default) <b>Selected</b> (default) Use compiler <code>`timescale</code> directives in generated Verilog code. <code>'off'</code> <b>Cleared</b> Suppress the use of compiler <code>`timescale</code> directives in generated Verilog code.
<b>Usage Notes</b>	The <code>`timescale</code> directive provides a way of specifying different delay values for multiple modules in a Verilog file. This setting does not affect the generated test bench.
<b>See Also</b>	LoopUnrolling, SafeZeroConcat, UseAggregatesForConst, UseRisingEdge



**Purpose**

Specify string prefixed to vector names in generated code

**Settings**

'string'

Default: 'vector\_of\_'

Specify a string to be prefixed to vector names in generated code.

# Verbosity property

---

**Purpose** Specify level of detail for messages displayed during code generation

**Settings** Default: 1  
0  
When `Verbosity` is set to 0, no code generation progress messages are displayed as code generation proceeds. When `Verbosity` is set to 1, more detailed progress messages are displayed.

# VerilogFileExtension property

---

**Purpose** Specify file type extension for generated Verilog files

**Settings** 'string'

The default file type extension for generated Verilog files is .v.

**See Also** TargetLanguage

# VHDLArchitectureName property

---

**Purpose** Specify architecture name for generated HDL code

**Settings** 'string'  
The default architecture name is 'rtl'.

# VHDLFileExtension property

---

**Purpose** Specify file type extension for generated VHDL files

**Settings** 'string'  
The default file type extension for generated VHDL files is .vhd.

**See Also** TargetLanguage

## VHDLlibraryName property

---

**Purpose** Specify name of target library for generated HDL code

**Settings** 'string'  
The default target library name is 'work'.

**See Also** HDLCompileInit

# Property Reference

---

Language Selection Properties (p. 24-2)	Properties for selecting language of generated HDL code
File Naming and Location Properties (p. 24-3)	Properties that name and specify location of generated files
Reset Properties (p. 24-4)	Properties that specify reset signals in generated code
Header Comment and General Naming Properties (p. 24-5)	Properties affecting generation of header comments and process, module, component instance, and other name strings
Script Generation Properties (p. 24-7)	Properties affecting generation of script files for simulation and synthesis tools
Port Properties (p. 24-9)	Properties that specify port characteristics in generated code
Advanced Coding Properties (p. 24-10)	Advanced HDL coding properties
Test Bench Properties (p. 24-12)	Properties that specify generated test bench code
Generated Model Properties (p. 24-14)	Properties for controlling naming and appearance of generated models

## Language Selection Properties

TargetLanguage

Specify HDL language to use for generated code



## File Naming and Location Properties

HDLMapFilePostfix	Specify postfix string appended to file name for generated mapping file
TargetDirectory	Identify folder into which the coder writes generated output files.
VerilogFileExtension	Specify file type extension for generated Verilog files
VHDLFileExtension	Specify file type extension for generated VHDL files

## Reset Properties

Oversampling	Specify frequency of global oversampling clock as a multiple of the model's base rate
ResetAssertedLevel	Specify asserted (active) level of reset input signal
ResetLength	Define length of time (in clock cycles) during which reset is asserted
ResetType	Specify whether to use asynchronous or synchronous reset logic when generating HDL code for registers

## Header Comment and General Naming Properties

<code>ClockProcessPostfix</code>	Specify string to append to HDL clock process names
<code>ComplexImagPostfix</code>	Specify string to append to imaginary part of complex signal names
<code>ComplexRealPostfix</code>	Specify string to append to real part of complex signal names
<code>EntityConflictPostfix</code>	Specify string to append to duplicate VHDL entity or Verilog module names
<code>InstancePostfix</code>	Specify string appended to generated component instance names
<code>InstancePrefix</code>	Specify string prefixed to generated component instance names
<code>PackagePostfix</code>	Specify string to append to specified model or subsystem name to form name of package file
<code>ReservedWordPostfix</code>	Specify string appended to identifiers for entities, signals, constants, or other model elements that conflict with VHDL or Verilog reserved words
<code>SplitArchFilePostfix</code>	Specify string to append to specified name to form name of file containing model's VHDL architecture
<code>SplitEntityArch</code>	Specify whether generated VHDL entity and architecture code is written to single VHDL file or to separate files
<code>SplitEntityFilePostfix</code>	Specify string to append to specified model name to form name of generated VHDL entity file

<code>TimingControllerPostfix</code>	Specify suffix appended to DUT name to form timing controller name
<code>VectorPrefix</code>	Specify string prefixed to vector names in generated code
<code>VHDLArchitectureName</code>	Specify architecture name for generated HDL code
<code>VHDLLibraryName</code>	Specify name of target library for generated HDL code

## Script Generation Properties

EDAScriptGeneration	Enable or disable generation of script files for third-party tools
HDLCompileFilePostfix	Specify postfix string appended to file name for generated Mentor Graphics ModelSim compilation scripts
HDLCompileInit	Specify string written to initialization section of compilation script
HDLCompileTerm	Specify string written to termination section of compilation script
HDLCompileVerilogCmd	Specify command string written to compilation script for Verilog files
HDLCompileVHDLCmd	Specify command string written to compilation script for VHDL files
HDLSimCmd	Specify simulation command written to simulation script
HDLSimFilePostfix	Specify postfix string appended to file name for generated Mentor Graphics ModelSim simulation scripts
HDLSimInit	Specify string written to initialization section of simulation script
HDLSimTerm	Specify string written to termination section of simulation script
HDLSimViewWaveCmd	Specify waveform viewing command written to simulation script
HDLSynthCmd	Specify command written to synthesis script

<code>HDLSynthFilePostfix</code>	Specify postfix string appended to file name for generated synthesis scripts
<code>HDLSynthInit</code>	Specify string written to initialization section of synthesis script
<code>HDLSynthTerm</code>	Specify string written to termination section of synthesis script
<code>HDLSynthTool</code>	Select synthesis tool for which the coder generates scripts.

## Port Properties

<code>ClockEnableInputPort</code>	Name HDL port for model's clock enable input signals
<code>ClockEnableOutputPort</code>	Specify name of clock enable output port
<code>ClockInputPort</code>	Name HDL port for model's clock input signals
<code>ClockInputs</code>	Specify generation of single or multiple clock inputs
<code>EnablePrefix</code>	Specify base name string for internal clock enables in generated code
<code>InputType</code>	Specify HDL data type for model's input ports
<code>OutputType</code>	Specify HDL data type for model's output ports
<code>ResetInputPort</code>	Name HDL port for model's reset input
<code>ScalarizePorts</code>	Flatten vector ports into structure of scalar ports in VHDL code

## Advanced Coding Properties

<code>BlockGenerateLabel</code>	Specify string to append to block labels used for HDL GENERATE statements
<code>CheckHDL</code>	Check model or subsystem for HDL code generation compatibility
<code>GenerateHDLCode</code>	Generate HDL code
<code>GenerateValidationModel</code>	Generate validation model with HDL code
<code>GenerateWebview</code>	Include model Web view in the code generation report
<code>HandleAtomicSubsystem</code>	Enable reusable code generation for identical atomic subsystems
<code>HDLControlFiles</code>	Attach code generation control file to model
<code>InitializeBlockRAM</code>	Enable or suppress generation of initial signal value for RAM blocks
<code>InlineMATLABBlockCode</code>	Inline HDL code for MATLAB Function blocks
<code>InstanceGenerateLabel</code>	Specify string to append to instance section labels in VHDL GENERATE statements
<code>MaskParameterAsGeneric</code>	Generate reusable HDL code for subsystems with identical mask parameters that differ only in value
<code>MulticyclePathInfo</code>	Generate text file that reports multicycle path constraint information, for use with synthesis tools.
<code>OptimizationReport</code>	Display HTML optimization report



---

OutputGenerateLabel	Specify string that labels output assignment block for VHDL GENERATE statements
PipelinePostfix	Specify string to append to names of input or output pipeline registers generated for pipelined block implementations
RAMArchitecture	Select RAM architecture with clock enable, or without clock enable, for all RAMs in DUT subsystem
ResourceReport	Display HTML resource utilization report
Traceability	Enable or disable creation of HTML code generation report with code-to-model and model-to-code hyperlinks
UserComment	Specify comment line in header of generated HDL and test bench files
Verbosity	Specify level of detail for messages displayed during code generation

## Test Bench Properties

<code>ClockHighTime</code>	Specify period, in nanoseconds, during which test bench drives clock input signals high (1)
<code>ClockLowTime</code>	Specify period, in nanoseconds, during which test bench drives clock input signals low (0)
<code>ForceClock</code>	Specify whether test bench forces clock input signals
<code>ForceClockEnable</code>	Specify whether test bench forces clock enable input signals
<code>ForceReset</code>	Specify whether test bench forces reset input signals
<code>GenerateCoSimBlock</code>	Generate HDL Cosimulation block(s) for use in testing DUT
<code>GenerateCoSimModel</code>	Generate model containing HDL Cosimulation block for use in testing DUT
<code>HoldInputDataBetweenSamples</code>	Specify how long substrate signal values are held in valid state
<code>HoldTime</code>	Specify hold time for input signals and forced reset input signals
<code>IgnoreDataChecking</code>	Specify number of samples during which output data checking is suppressed
<code>InitializeTestBenchInputs</code>	Specify initial value driven on test bench inputs before data is asserted to DUT
<code>MultifileTestBench</code>	Divide generated test bench into helper functions, data, and HDL test bench code files
<code>SimulatorFlags</code>	Specify simulator flags to apply to generated compilation scripts

<code>TestBenchClockEnableDelay</code>	Define elapsed time (in clock cycles) between deassertion of reset and assertion of clock enable
<code>TestBenchDataPostFix</code>	Specify suffix added to test bench data file name when generating multi-file test bench
<code>TestBenchPostFix</code>	Specify suffix to test bench name
<code>TestBenchReferencePostFix</code>	Specify string appended to names of reference signals generated in test bench code

## Generated Model Properties

<code>CodeGenerationOutput</code>	Control production of generated code and display of generated model
<code>GeneratedModelName</code>	Specify name of generated model
<code>GeneratedModelNamePrefix</code>	Specify prefix to name of generated model
<code>HighlightAncestors</code>	Highlight ancestors of blocks in generated model that differ from original model
<code>HighlightColor</code>	Specify color for highlighted blocks in generated model

# Functions — Alphabetical List

---

# checkhdl

---

**Purpose** Check subsystem or model for HDL code generation compatibility

**Syntax**

```
checkhdl(bdroot)
checkhdl('modelName')
checkhdl('subsysname')
checkhdl(gcb)
output = checkhdl('system')
```

**Description** `checkhdl` generates an HDL Code Generation Check Report, saves the report to the target folder, and displays the report in a new window. Before generating HDL code, use `checkhdl` to check your subsystems or models.

The report lists compatibility errors with a link to each block or subsystem that caused a problem. To highlight and display incompatible blocks, click each link in the report while keeping the model open.

The report file name is `system_report.html`. `system` is the name of the subsystem or model passed in to `checkhdl`.

When a model or subsystem passes `checkhdl`, that does not imply code generation will complete. `checkhdl` does not verify all block parameters.

`checkhdl(bdroot)` examines the current model for HDL code generation compatibility.

`checkhdl('modelName')` examines the specified model, `modelName`.

`checkhdl('subsysname')` examines a subsystem. `subsysname` is the full block path for a subsystem at any level of the model hierarchy.

`checkhdl(gcb)` examines the currently selected subsystem.

`output = checkhdl('system')`

does not generate a report. Instead, it returns a 1xN struct array with one entry for each error, warning, or message. `system` specifies a model or the full block path for a subsystem at any level of the model hierarchy.

`checkhdl` reports three levels of compatibility problems:

- *Errors*: cause the code generation process to terminate. The report must not contain errors to continue with HDL code generation.
- *Warnings*: indicate problems in the generated code, but allow HDL code generation to continue. For example, the presence of an unsupported block in the model raises a warning. In this case, the coder attempts to proceed as if the block were not present in the design. This might lead to errors later on in the code generation process.
- *Messages*: indication that some data types have special treatment. For example, the coder automatically converts single-precision floating-point data types to double-precision because VHDL and Verilog do not support single-precision data types.

## Examples

Check the subsystem `symmetric_fir` within the model `sfir_fixed` for HDL code generation compatibility and generate a compatibility report.

```
checkhdl('sfir_fixed/symmetric_fir')
```

Check the subsystem `symmetric_fir_err` within the model `sfir_fixed_err` for HDL code generation compatibility, and return information on problems encountered in the struct output.

```
output = checkhdl('sfir_fixed_err/symmetric_fir_err')
### Starting HDL Check.
...
### HDL Check Complete with 4 errors, warnings and messages.
```

The following MATLAB commands display the top-level structure of the struct output, and its first cell.

```
output =

1x4 struct array with fields:
    path
    type
    message
    level
```

# checkhdl

---

```
output(1)

ans =

    path: 'sfir_fixed_err/symmetric_fir_err/Product'
    type: 'block'
    message: 'Unhandled mixed double and non-double datatypes at ports of block'
    level: 'Error'
```

## See Also

makehdl

## Tutorials

- “Selecting and Checking a Subsystem for HDL Compatibility”



**Purpose** Display HDL Workflow Advisor

**Syntax**  
`hdladvisor(gcb)`  
`hdladvisor(subsystem)`  
`hdladvisor(model, 'SystemSelector')`

**Description** `hdladvisor(gcb)` starts the HDL Workflow Advisor, passing the currently selected subsystem within the current model as the DUT to be checked.

`hdladvisor(subsystem)` starts the HDL Workflow Advisor, passing in the path to a specified subsystem within the model.

`hdladvisor(model, 'SystemSelector')` opens a System Selector window that lets you select a subsystem to be opened into the HDL Workflow Advisor as the device under test (DUT) to be checked.

**Examples** Open the subsystem `symmetric_fir` within the model `sfir_fixed` into the HDL Workflow Advisor.

```
hdladvisor('sfir_fixed/symmetric_fir')
```

---

Open a System Selector window to select a subsystem within the current model. Then open the selected subsystem into the HDL Workflow Advisor.

```
hdladvisor(gcs, 'SystemSelector')
```

**Alternatives** You can also open the HDL Workflow Advisor from the your model window by selecting → **Tools** **HDL Coder** > **HDL Workflow Advisor**.

**See Also** “What Is the HDL Workflow Advisor?” on page 19-2 | “Using the HDL Workflow Advisor Window” on page 19-6 | “Selecting and Running HDL Workflow Advisor Tasks” on page 19-9

# hdlapplycontrolfile

---

**Purpose** Apply control file settings to model

**Syntax** `hdlapplycontrolfile(modelname, controlfilename)`  
`hdlapplycontrolfile(dutname, controlfilename)`

**Description** `hdlapplycontrolfile(modelname, controlfilename)` applies the settings in the specified control file to the specified model.

`hdlapplycontrolfile(dutname, controlfilename)` applies the settings in the specified control file to a specified subsystem (the device under test, or DUT) within the current model.

**Tips**

- As of release R2010b, use of control files is not recommended, and the coder does not support the attachment of a control file to a new model. Instead, the coder now saves non-default block implementation and implementation parameter settings to the model itself. This eliminates the need to load and save a separate control file. The coder provides the `hdlapplycontrolfile` utility as a quick way to transfer HDL settings from existing models that have attached control files to other models.

- After you apply control file settings to a model, be sure to save the model.

- If you have existing models with attached control files, you should convert them to the current format. To do this, simply open the model and save it. Saving a model clears its attachment to its control file, but the control file itself is preserved so that you can apply it to other models if you wish.

For backward compatibility, the coder continues to support models that have attached control files. See “READ THIS FIRST: Control File Compatibility and Conversion Issues” on page 22-2 for further information.

- Some control files are designed to be generic, and do not specify the DUT using `generateHDLFor`. To apply settings from such a control file, you must supply a full path to the desired DUT using the `dutname` argument.

## Input Arguments

### **modelName**

Name of the target model, to which control file settings are applied.

**Default:** None

### **controlfilename**

Name of the control file containing hdl settings to be applied

**Default:** None

### **dutname**

Full path to the top-level subsystem (the device under test or DUT) within the target model.

**Default:** None

## Examples

Apply settings from `sfir_fixed_control.m` to the open model `sfir_fixed_newVersion`.

```
hdlapplycontrolfile('sfir_fixed_newVersion','sfir_fixed_control.m')  
Successfully loaded control file 'sfir_fixed_control.m' ...
```

---

Apply settings from `sfir_fixed_control.m` to the subsystem `symmetric_fir` within the open model `sfir_fixed_newVersion`.

```
hdlapplycontrolfile('sfir_fixed_newVersion/symmetric_fir','sfir_fixed_control.m')  
Successfully loaded control file 'sfir_fixed_control.m' ...
```

## See Also

| “READ THIS FIRST: Control File Compatibility and Conversion Issues” on page 22-2

# hdlispblkparams

---

**Purpose** Display HDL block parameters that have nondefault values

**Syntax** `hdlispblkparams(path)`  
`hdlispblkparams(path, 'all')`

**Description** `hdlispblkparams(path)` displays, for the specified block, the names and values of HDL parameters that have nondefault values.  
`hdlispblkparams(path, 'all')` displays, for the specified block, the names and values of all HDL block parameters.

**Input Arguments** **path**  
Path to a block or subsystem in the current model.

**Default:** None

**'all'**

If you pass in the string 'all', `hdlispblkparams` displays the names and values of all HDL properties of the specified block.

**Examples** The following example displays nondefault HDL block parameter settings for a Sum of Elements block).

```
hdlispblkparams('simplevectorsum/vsum/Sum of Elements')
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%  
HDL Block Parameters ('simplevectorsum/vsum/Sum of Elements')  
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
Implementation
```

```
Architecture : Linear
```

```
Implementation Parameters
```

```
InputPipeline : 1
```

The following example displays HDL block parameters and values for the currently selected block, (a Sum of Elements block).

```
hdlispblkparams(gcb, 'all')

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
HDL Block Parameters ('simplevectorsum/vsum/Sum of
Elements')
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

Implementation

Architecture : Linear

Implementation Parameters

InputPipeline : 0
OutputPipeline : 0
```

## See Also

“Set and View HDL Block Parameters” on page 8-2

# hdldispmdlparams

---

**Purpose** Display HDL model parameters that have nondefault values

**Syntax** `hdldispmdlparams(model)`  
`hdldispmdlparams(model, 'all')`

**Description** `hdldispmdlparams(model)` displays, for the specified model, the names and values of HDL parameters that have nondefault values.  
`hdldispmdlparams(model, 'all')` displays the names and values of all HDL parameters for the specified model.

**Input Arguments** **model**  
Name of an open model.

**Default:** None

**'all'**

If you pass in the string 'all' , `hdldispmdlparams` displays the names and values of all HDL properties of the specified model.

**Examples** The following example displays HDL properties of the current model that have nondefault values.

```
hdldispmdlparams(bdroot)

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
HDL CodeGen Parameters (non-default)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

CodeGenerationOutput      : 'GenerateHDLCodeAndDisplayGeneratedModel'
HDLSubsystem              : 'simplevectorsum_2atomics/Subsystem'
OptimizationReport        : 'on'
ResetInputPort            : 'rst'
ResetType                  : 'Synchronous'
```

---

The following example displays HDL properties and values of the current model.

```
hdlispmdlparams(bdroot, 'all')

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
HDL CodeGen Parameters
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

AddPipelineRegisters           : 'off'
Backannotation                 : 'on'
BlockGenerateLabel            : '_gen'
CheckHDL                      : 'off'
ClockEnableInputPort          : 'clk_enable'
.
.
.
VerilogFileExtension           : '.v'
```

## See Also

“View HDL Model Parameters” on page 8-7

# hdlget\_param

---

**Purpose** Return value of specified HDL block-level parameter for specified block

**Syntax** `p = hdlget_param(block_path,prop)`

**Description** `p = hdlget_param(block_path,prop)` gets the value of a specified HDL property of a block or subsystem, and returns the value to the output variable.

**Tips**

- Use `hdlget_param` only to obtain the value of HDL block parameters (see “Blocks Supported for HDL Code Generation” on page 9-3 for a complete listing of block implementations and their parameters). To obtain the value of general model parameters, use the `set_param` function.

## Input Arguments

### **block\_path**

Path to a block or subsystem in the current model.

**Default:** None

### **prop**

A string designating one of the following:

- The name of an HDL block property of the block or subsystem specified by `block_path`.
- 'all' : If `prop` is set to 'all', `hdlget_param` returns Name, Value pairs for HDL properties of the specified block.

**Default:** None

## Output Arguments

### **p**

`p` receives the value of the HDL block property specified by `prop`. The data type and dimensions of `p` depend on the data type and dimensions of the value returned. If `prop` is set to 'all', `p` is a cell array.



## Examples

In the following example `hdlget_param` returns the value of the HDL block parameter `OutputPipeline` to the variable `p`.

```
p = hdlget_param(gcb, 'OutputPipeline')  
  
p =  
  
    3
```

---

In the following example `hdlget_param` returns HDL block parameters and values for the current block to the cell array `p`.

```
p = hdlget_param(gcb, 'all')  
  
p =  
  
    'Architecture'    'Linear'    'InputPipeline'    [0]    'OutputPipeline'    [0]
```

## See Also

`hdlset_param`

# hdlLib

---

**Purpose** Create library of blocks that support HDL code generation

**Syntax** `hdlLib`

**Description** `hdlLib` creates a library of blocks that are compatible with HDL code generation. The library affords quick access to supported blocks. Use blocks from this library to build models that are compatible with the coder.

The default name for the library is `hdlSupported`. After you generate the library, save it to a folder of your choice.

`hdlLib` loads many block libraries during the creation of the `hdlSupported` library. (Loading libraries causes a license checkout.) When `hdlLib` completes generation of the library, it does not unload block libraries.

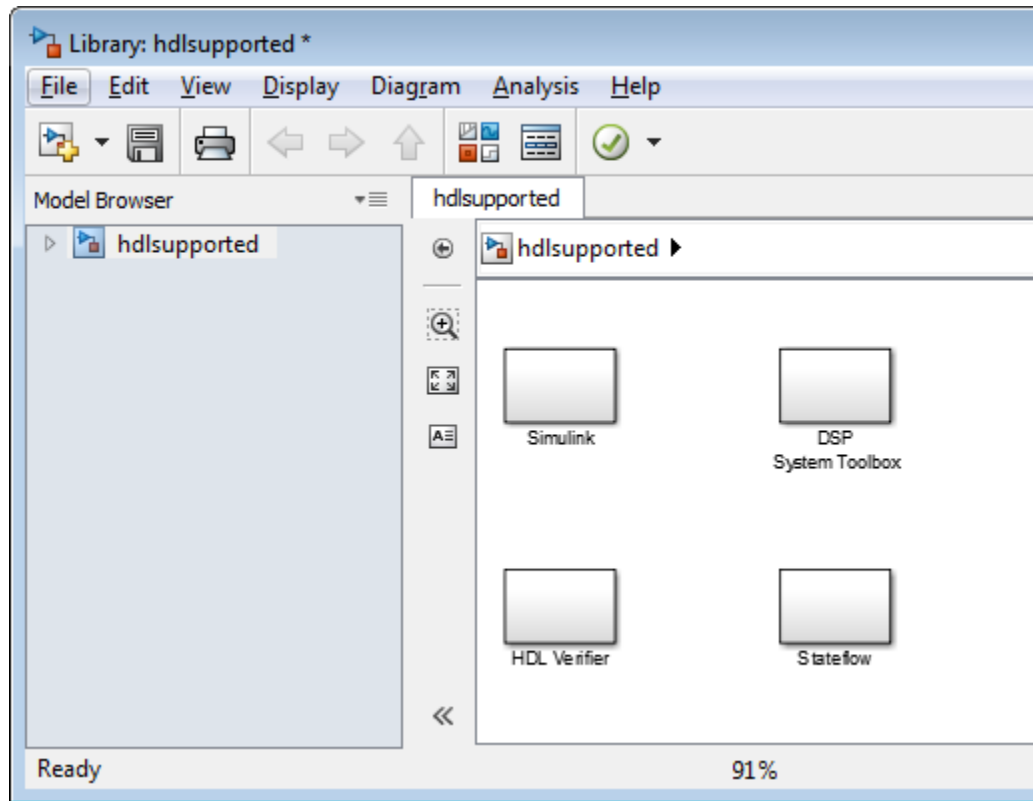
Parameter settings for some blocks in the `hdlSupported` library differ from corresponding blocks in other libraries.

The set of supported blocks will change in future releases of the coder. To keep the `hdlSupported` current, rebuild the library each time you install a new release.

**Examples** Build a library of HDL-compatible blocks.

```
hdlLib
```

The following figure shows the top-level view of the `hdlSupported` library.



**See Also**

“Create a Supported Blocks Library” on page 14-34

# hdlnewblackbox

---

**Purpose** Generate customizable control file from selected subsystem or blocks

**Syntax**

```
hdlnewblackbox
hdlnewblackbox('blockpath')
hdlnewblackbox({'blockpath1','blockpath2',... 'blockpathN'})
[cmd, impl] = hdlnewblackbox
[cmd, impl] = hdlnewblackbox('blockpath')
[cmd, impl] = hdlnewblackbox({'blockpath1','blockpath2',
    ... 'blockpathN'})
[cmd, impl, params] = hdlnewblackbox
[cmd, impl, params] = hdlnewblackbox('blockpath')
[cmd, impl, params] = hdlnewblackbox({'blockpath1',
    'blockpath2',... 'blockpathN'})
```

**Description** The `hdlnewblackbox` utility helps you construct `forEach` calls for use in code generation control files when generating black box interfaces. Given a selection of one or more blocks from your model, `hdlnewblackbox` returns the following as string data in the MATLAB workspace for each selected block:

- A `forEach` call coded with the `modelscope`, `blocktype`, and default implementation class (`SubsystemBlackBoxHDLInstantiation`) arguments for the block.
- (Optional) a cell array of strings enumerating the available implementations classes for the subsystem.
- (Optional) A cell array of cell arrays of strings enumerating the names of implementation parameters corresponding to the implementation classes. `hdlnewblackbox` does not list data types and other details of implementation parameters.

`hdlnewblackbox` returns a `forEach` call for each selected block in the model.

`hdlnewblackbox('blockpath')` returns a `forEach` call for the block specified by the `'blockpath'` argument. The `'blockpath'` argument is a string specifying the full Simulink path to the desired block.

`hdlnewblackbox({'blockpath1','blockpath2',... 'blockpathN'})` returns a `forEach` call for the blocks specified by the `{'blockpath1','blockpath2',... 'blockpathN'}` arguments. The `{'blockpath1','blockpath2',... 'blockpathN'}` arguments are passed as a cell array of strings, each string specifying the full Simulink path to a desired block.

`[cmd, impl] = hdlnewblackbox` returns a `forEach` call for each selected block in the model to the string variable `cmd`. The call also returns `impl`, a cell array of cell arrays of strings enumerating the available implementations for the block.

`[cmd, impl] = hdlnewblackbox('blockpath')` returns a `forEach` call for the block specified by the `'blockpath'` argument to the string variable `cmd`. The call also returns `impl`, a cell array of cell arrays of strings enumerating the available implementations for the block. The `'blockpath'` argument is a string specifying the full Simulink path to the desired block.

`[cmd, impl] = hdlnewblackbox({'blockpath1','blockpath2',... 'blockpathN'})` returns a `forEach` call for the blocks specified by the `{'blockpath1','blockpath2',... 'blockpathN'}` arguments to the string variable `cmd`. The call also returns `impl`, a cell array of cell arrays of strings enumerating the available implementations for the block. The `{'blockpath1','blockpath2',... 'blockpathN'}` arguments are passed as a cell array of strings, each string specifying the full Simulink path to a desired block.

`[cmd, impl, params] = hdlnewblackbox` returns a `forEach` call for each selected block in the model to the string variable `cmd`. The call also returns:

- `impl`, a cell array of cell arrays of strings enumerating the available implementations for the block.
- `params`, a cell array of cell arrays of strings enumerating the available implementation parameters corresponding to each implementation.

# hdlnewblackbox

---

`[cmd, impl, params] = hdlnewblackbox('blockpath')` returns a `forEach` call for the block specified by the `'blockpath'` argument to the string variable `cmd`. The call also returns:

- `impl`, a cell array of cell arrays of strings enumerating the available implementations for the block.
- `params`, a cell array of cell arrays of strings enumerating the available implementation parameters corresponding to each implementation.

The `'blockpath'` argument is a string specifying the full Simulink path to the desired block.

`[cmd, impl, params] = hdlnewblackbox({'blockpath1', 'blockpath2', ... 'blockpathN'})` returns a `forEach` call for the blocks specified by the `{'blockpath1', 'blockpath2', ... 'blockpathN'}` arguments to the string variable `cmd`. The call also returns:

- `impl`, a cell array of cell arrays of strings enumerating the available implementations for the block.
- `params`, a cell array of cell arrays of strings enumerating the available implementation parameters corresponding to each implementation.

The `{'blockpath1', 'blockpath2', ... 'blockpathN'}` arguments are passed as a cell array of strings, each string specifying the full Simulink path to a desired block.

## Tips

After invoking `hdlnewblackbox`, you will generally want to insert the `forEach` calls returned by the function into a control file, and use the implementation information returned to specify a nondefault block implementation.

## Examples

```
% Return a forEach call for a specific subsystem to the MATLAB workspace
hdlnewblackbox('sfir_fixed/symmetric_fir');
%
% Return forEach calls for all currently selected blocks to the MATLAB workspace
hdlnewblackbox;
%
```

```
% Return forEach calls, implementation names, and implementation parameter names
% for all currently selected blocks to string variables
[cmd,impl,parms] = hdlnewblackbox;
```

# hdlnewcontrol

---

**Purpose** Construct code generation control object for use in control file

**Syntax** `object = hdlnewcontrol(mfilename)`

**Description** `object = hdlnewcontrol(mfilename)` constructs and returns a control generation control object (`object`) that is linked to a code generation control file.

The argument to `hdlnewcontrol` is the name of the control file itself. Use the `mfilename` function to pass in the file name string.

---

**Tip** The `hdlnewcontrol` function constructs an instance of the class `slhdlcoder.ConfigurationContainer`. `hdlnewcontrol` is a wrapper function provided to let you instantiate such objects. You should not directly call the constructor of the class.

In your control files, use only the public methods of the class `slhdlcoder.ConfigurationContainer`. Public methods are described in this document. Other methods of this class are for MathWorks internal development use only.

---

## See also

- “READ THIS FIRST: Control File Compatibility and Conversion Issues” on page 22-2



**Purpose** Generate customizable control file from selected subsystem or blocks

**Syntax**

```
hdlnewcontrolfile
hdlnewcontrolfile('blockpath')
hdlnewcontrolfile({'blockpath1','blockpath2',
    ...'blockpathN'})
t = hdlnewcontrolfile(...)
```

**Description** The coder provides the `hdlnewcontrolfile` utility to help you construct code generation control files. Given a selection of one or more blocks from your model, `hdlnewcontrolfile` generates a control file containing:

- A `c.generateHDLFor` call specifying the full path to the currently selected block or subsystem from which code is to be generated.
- `c.forEach` calls for the selected blocks that have HDL implementations.
- Comments providing information about supported implementations and parameters for selected blocks that have HDL implementations.
- `c.set` calls for global HDL Coder options that are set to nondefault values.

Generated control files are automatically opened as untitled files in the MATLAB editor for further customization. The file naming sequence for successively generated control files is `Untitled1`, `Untitled2`, ... `UntitledN`.

`hdlnewcontrolfile` returns a control file containing a `forEach` statement and comments for each selected block in the model.

`hdlnewcontrolfile('blockpath')` returns a control file containing a `forEach` statement and comments for the block specified by the `'blockpath'` argument. The `'blockpath'` argument is a string specifying the full Simulink path to the desired block.

`hdlnewcontrolfile({'blockpath1','blockpath2',... 'blockpathN'})` returns a control file containing a `forEach` statement and comments for the blocks specified by the

# hdlnewcontrolfile

---

{'blockpath1','blockpath2',... 'blockpathN'} arguments. The {'blockpath1','blockpath2',... 'blockpathN'} arguments are passed as a cell array of strings, each string specifying the full Simulink path to a desired block.

t = hdlnewcontrolfile(...) returns control statements as text in the string variable t, instead of returning a control file.

## Tips

You can use the generated control file as:

- A starting point for development of a customized control file.
- A source of information or documentation of the HDL code generation parameter settings in the model.

## Examples

```
% Generate control file for a specific block
hdlnewcontrolfile('sfir_fixed/symmetric_fir/Product1');
%
% Generate a control file for all currently selected blocks
hdlnewcontrolfile;
%
% Generate a control file for two specific blocks
hdlnewcontrolfile({'sfir_fixed/symmetric_fir/Add1',...
'sfir_fixed/symmetric_fir/Product2'});
```

**Purpose** Generate forEach calls for insertion into code generation control files

**Syntax**

```
hdlnewforeach
hdlnewforeach('blockpath')
hdlnewforeach({'blockpath1','blockpath2',...})
[cmd, impl] = hdlnewforeach
[cmd, impl] = hdlnewforeach('blockpath')
[cmd, impl] = hdlnewforeach({'blockpath1','blockpath2',...})
[cmd, impl, parms] = hdlnewforeach
[cmd, impl, parms] = hdlnewforeach('blockpath')
[cmd, impl, parms] = hdlnewforeach({'blockpath1','blockpath2',
...})
```

**Description** The coder provides the hdlnewforeach utility to help you construct forEach calls for use in code generation control files. Given a selection of one or more blocks from your model, hdlnewforeach returns the following for each selected block, as string data in the MATLAB workspace:

- A forEach call coded with the modelscope, blocktype, and default implementation arguments for the block.
- (Optional) A cell array of cell arrays of strings enumerating the available implementations for the block.
- (Optional) A cell array of cell arrays of strings enumerating the names of implementation parameters corresponding to the block implementations. See “Block Implementation Parameters” on page 9-49 for that data types and other details of block implementation parameters.

hdlnewforeach returns a forEach call for each selected block in the model. Each call is returned as a string.

hdlnewforeach('blockpath') returns a forEach call for a specified block in the model. The call is returned as a string.

The 'blockpath' argument is a string specifying the full path to the desired block.

# hdlnewforeach

---

`hdlnewforeach({'blockpath1','blockpath2',...})` returns a `forEach` call for each specified block in the model. Each call is returned as a string.

The `{'blockpath1','blockpath2',...}` argument is a cell array of strings, each of which specifies the full path to a desired block.

`[cmd, impl] = hdlnewforeach` returns a `forEach` call for each selected block in the model to the string variable `cmd`. In addition, the call returns a cell array of cell arrays of strings (`impl`) enumerating the available implementations for the block.

`[cmd, impl] = hdlnewforeach('blockpath')` returns a `forEach` call for a specified block in the model to the string variable `cmd`. In addition, the call returns a cell array of cell arrays of strings (`impl`) enumerating the available implementations for the block.

The `'blockpath'` argument is a string specifying the full path to the desired block.

`[cmd, impl] = hdlnewforeach({'blockpath1','blockpath2',...})` returns a `forEach` call for each specified block in the model to the string variable `cmd`. In addition, the call returns a cell array of cell arrays of strings (`impl`) enumerating the available implementations for the block.

The `{'blockpath1','blockpath2',...}` argument is a cell array of strings, each of which specifies the full path to a desired block.

`[cmd, impl, parms] = hdlnewforeach` returns a `forEach` call for each selected block in the model to the string variable `cmd`. In addition, the call returns:

- A cell array of cell arrays of strings (`impl`) enumerating the available implementations for the block.
- A cell array of cell arrays of strings (`parms`) enumerating the available implementation parameters corresponding to each implementation.

`[cmd, impl, parms] = hdlnewforeach('blockpath')` returns a `forEach` call for a specified block in the model to the string variable `cmd`. In addition, the call returns:

- A cell array of cell arrays of strings (`impl`) enumerating the available implementations for the block.
- A cell array of cell arrays of strings (`parms`) enumerating the available implementation parameters corresponding to each implementation.

The `'blockpath'` argument is a string specifying the full path to the desired block.

```
[cmd, impl, parms] =  
hdlnewforeach({'blockpath1', 'blockpath2', ...}) returns a  
forEach call for each specified block in the model to the string variable  
cmd. In addition, the call returns:
```

- A cell array of cell arrays of strings (`impl`) enumerating the available implementations for the block.
- A cell array of cell arrays of strings (`parms`) enumerating the available implementation parameters corresponding to each implementation.

The `{'blockpath1', 'blockpath2', ...}` argument is a cell array of strings, each of which specifies the full path to a desired block.

## Tips

`hdlnewforeach` returns an empty string for blocks that do not have an HDL implementation. `hdlnewforeach` also returns an empty string for subsystems, which are a special case. Subsystems do not have a default implementation class, but special-purpose subsystems implementations are provided (see “External Component Interfaces”).

After invoking `hdlnewforeach`, you will generally want to insert the `forEach` calls returned by the function into a control file, and use the implementation and parameter information returned to specify a nondefault block implementation. See “Generating Selection/Action Statements with the `hdlnewforeach` Function” on page 22-18 for a worked example.

## Examples

The following example generates `forEach` commands for two explicitly specified blocks.

```
hdlnewforeach({'sfir_fixed/symmetric_fir/Add4', ...  
'sfir_fixed/symmetric_fir/Product2'})
```

```
ans =

c.foreach('./symmetric_fir/Add4',...
'built-in/Sum', {},...
'default', {}); % Default architecture is 'Linear'

c.foreach('./symmetric_fir/Product2',...
'built-in/Product', {},...
'default', {}); % Default architecture is 'Linear'
```

The following example generates a `foreach` command for an explicitly specified `Sum` block. The implementation and parameters information returned is listed after the `foreach` command.

```
c.foreach('./symmetric_fir/Add4',...
'built-in/Sum', {},...
'default', {}); % Default architecture is 'Linear'

impl =

    {3x1 cell}

parms =

    {1x2 cell}    {1x2 cell}    {1x2 cell} >> parms{1:4}

>> impl{1}

ans =

    'Linear'
    'Cascade'
```

```
'Tree'ans =  
  
>> parms{1:3}  
  
ans =  
  
    'InputPipeline'    'OutputPipeline'  
  
ans =  
  
    'InputPipeline'    'OutputPipeline'  
  
ans =  
  
    'InputPipeline'    'OutputPipeline'
```

# hdlrestoreparams

---

<b>Purpose</b>	Restore block- and model-level HDL parameters to model
<b>Syntax</b>	<code>hdlrestoreparams(subsys)</code> <code>hdlrestoreparams(subsys,filename)</code>
<b>Description</b>	<p><code>hdlrestoreparams(subsys)</code> restores to the specified model the default block- and model-level HDL settings.</p> <p><code>hdlrestoreparams(subsys,filename)</code> restores to the specified model the block- and model-level HDL settings from a previously saved file.</p>
<b>Input Arguments</b>	<p><b>subsys - Subsystem name</b> string Subsystem name, specified as a string, with full hierarchical path. <b>Example:</b> 'modelName/subsysTarget' <b>Example:</b> 'modelName/subsysA/subsysB/subsysTarget'</p> <p><b>filename - Name of file</b> string Name of file containing previously saved HDL model parameters. <b>Example:</b> 'mymodel_saved_params.m'</p>
<b>Examples</b>	<p><b>Reset and Restore HDL-Related Model Parameters</b></p> <p>Open the model.</p> <pre>sfir_fixed</pre> <p>Verify that model parameters have default values.</p> <pre>hdlsaveparams('sfir_fixed/symmetric_fir')</pre> <pre>hdlset_param('sfir_fixed', 'HDLSubsystem', 'sfir_fixed');</pre>



Set HDL-related model parameters for the `symmetric_fir` subsystem.

```
hdlset_param('sfir_fixed/symmetric_fir', 'SharingFactor', 3)
hdlset_param('sfir_fixed/symmetric_fir/Product',
             'InputPipeline', 5)
```

Verify that model parameters are set.

```
hdlsaveparams('sfir_fixed/symmetric_fir')

hdlset_param('sfir_fixed', 'HDLSubsystem',
             'sfir_fixed/symmetric_fir');
hdlset_param('sfir_fixed/symmetric_fir', 'SharingFactor', 3);
hdlset_param('sfir_fixed/symmetric_fir/Product',
             'InputPipeline', 5);
```

Save the model parameters to a MATLAB script, `sfir_saved_params.m`.

```
hdlsaveparams('sfir_fixed/symmetric_fir',
             'sfir_saved_params.m')
```

Reset all HDL-related model parameters to default values.

```
hdlrestoreparams('sfir_fixed/symmetric_fir')
```

Verify that model parameters have default values.

```
hdlsaveparams('sfir_fixed/symmetric_fir')

hdlset_param('sfir_fixed', 'HDLSubsystem',
             'sfir_fixed');
```

Restore the saved model parameters from `sfir_saved_params.m`.

```
hdlrestoreparams('sfir_fixed/symmetric_fir',
             'sfir_saved_params.m')
```

Verify that the saved model parameters are restored.

```
hdlsaveparams('sfir_fixed/symmetric_fir')
```

# hdlrestoreparams

---

```
hdlset_param('sfir_fixed', 'HDLSubsystem',  
            'sfir_fixed/symmetric_fir');  
hdlset_param('sfir_fixed/symmetric_fir', 'SharingFactor', 3);  
hdlset_param('sfir_fixed/symmetric_fir/Product',  
            'InputPipeline', 5);
```

**See Also** [hdlsaveparams](#)

<b>Purpose</b>	Save nondefault block- and model-level HDL parameters
<b>Syntax</b>	<code>hdlsaveparams(subsys)</code> <code>hdlsaveparams(subsys,filename)</code>
<b>Description</b>	<p><code>hdlsaveparams(subsys)</code> displays nondefault block- and model-level HDL parameters.</p> <p><code>hdlsaveparams(subsys,filename)</code> saves nondefault block- and model-level HDL parameters to a MATLAB script.</p>
<b>Input Arguments</b>	<p><b>subsys - Subsystem name</b> string Subsystem name, specified as a string, with full hierarchical path. <b>Example:</b> 'modelName/subsysTarget' <b>Example:</b> 'modelName/subsysA/subsysB/subsysTarget'</p> <p><b>filename - Name of file</b> string Name of file to which you are saving model parameters, specified as a string. <b>Example:</b> 'mymodel_saved_params.m'</p>
<b>Examples</b>	<p><b>Display HDL-Related Nondefault Model Parameters</b></p> <p>Open the model.</p> <pre>sfir_fixed</pre> <p>Set HDL-related model parameters for the <code>symmetric_fir</code> subsystem.</p> <pre>hdlset_param('sfir_fixed/symmetric_fir', 'SharingFactor', 3) hdlset_param('sfir_fixed/symmetric_fir/Product', 'InputPipeline', 5)</pre>

# hdlsaveparams

---

Display HDL-related nondefault model parameters for the `symmetric_fir` subsystem.

```
hdlsaveparams('sfir_fixed/symmetric_fir')
```

```
hdlset_param('sfir_fixed', 'HDLSubsystem', 'sfir_fixed/symmetric_fir');  
hdlset_param('sfir_fixed/symmetric_fir', 'SharingFactor', 3);  
hdlset_param('sfir_fixed/symmetric_fir/Product', 'InputPipeline', 5);
```

The output identifies the subsystem and displays its HDL-related parameter values.

## Save and Restore HDL-Related Model Parameters

Open the model.

```
sfir_fixed
```

Verify that model parameters have default values.

```
hdlsaveparams('sfir_fixed/symmetric_fir')
```

```
hdlset_param('sfir_fixed', 'HDLSubsystem', 'sfir_fixed');
```

Set HDL-related model parameters for the `symmetric_fir` subsystem.

```
hdlset_param('sfir_fixed/symmetric_fir', 'SharingFactor', 3)  
hdlset_param('sfir_fixed/symmetric_fir/Product',  
             'InputPipeline', 5)
```

Verify that model parameters are set.

```
hdlsaveparams('sfir_fixed/symmetric_fir')
```

```
hdlset_param('sfir_fixed', 'HDLSubsystem',  
             'sfir_fixed/symmetric_fir');  
hdlset_param('sfir_fixed/symmetric_fir', 'SharingFactor', 3);  
hdlset_param('sfir_fixed/symmetric_fir/Product',  
             'InputPipeline', 5);
```

Save the model parameters to a MATLAB script, `sfir_saved_params.m`.

```
hdlsaveparams('sfir_fixed/symmetric_fir',  
             'sfir_saved_params.m')
```

Reset all HDL-related model parameters to default values.

```
hdlrestoreparams('sfir_fixed/symmetric_fir')
```

Verify that model parameters have default values.

```
hdlsaveparams('sfir_fixed/symmetric_fir')
```

```
hdlset_param('sfir_fixed', 'HDLSubsystem',  
            'sfir_fixed');
```

Restore the saved model parameters from `sfir_saved_params.m`.

```
hdlrestoreparams('sfir_fixed/symmetric_fir',  
                'sfir_saved_params.m')
```

Verify that the saved model parameters are restored.

```
hdlsaveparams('sfir_fixed/symmetric_fir')
```

```
hdlset_param('sfir_fixed', 'HDLSubsystem',  
            'sfir_fixed/symmetric_fir');  
hdlset_param('sfir_fixed/symmetric_fir', 'SharingFactor', 3);  
hdlset_param('sfir_fixed/symmetric_fir/Product',  
            'InputPipeline', 5);
```

**See Also** `hdlrestoreparams`

# hdlset\_param

---

**Purpose** Set HDL-related parameters at model or block level

**Syntax** `hdlset_param(path,Name,Value)`

**Description** `hdlset_param(path,Name,Value)` sets HDL-related parameters in the block or model referenced by `path`. The parameters to be set, and their values, are specified by one or more `Name,Value` pair arguments. You can specify several name and value pair arguments in any order as `Name1,Value1, ...,NameN,ValueN`.

- Tips**
- When you set multiple parameters on the same model or block, use a single `hdlset_param` command with multiple pairs of arguments, rather than multiple `hdlset_param` commands. This technique is more efficient because using a single call requires evaluating parameters only once.
  - To set HDL block parameters for multiple blocks, use the `find_system` function to locate the blocks of interest. Then, use a loop to iterate over the blocks and call `hdlset_param` to set the desired parameters.

## Input Arguments

### **path**

Path to the model or block for which `hdlset_param` is to set one or more parameter values.

**Default:** None

### **Name-Value Pair Arguments**

Specify optional comma-separated pairs of `Name,Value` arguments, where `Name` is the argument name and `Value` is the corresponding value. `Name` must appear inside single quotes (' '). You can specify several name and value pair arguments in any order as `Name1,Value1, ...,NameN,ValueN`.

### **Name**

`Name` is a string specifying the name of one of the following:

- A model-level HDL-related property. See Properties — Alphabetical List for a complete listing and definitions of properties, their data types and their default values.
- An HDL block property, such as an implementation name or an implementation parameter. See “Blocks Supported for HDL Code Generation” on page 9-3 for a complete listing of block implementations and their parameters.

**Default:** None

## Value

Value is a value to be applied to the corresponding property in a Name, Value argument.

**Default:** Default value is dependent on the property.

## Examples

The following example uses the `sfir_fixed` model to demonstrate how to locate a group of blocks in a subsystem and specify the same output pipeline depth for each of the blocks.

```
open sfir_fixed;
prodblocks = find_system('sfir_fixed/symmetric_fir', 'BlockType', 'Product');
for ii=1:length(prodblocks), hdlset_param(prodblocks{ii}, 'OutputPipeline', 2), end;
```

## How To

- “Set and View HDL Block Parameters” on page 8-2
- “Set HDL Block Parameters for Multiple Blocks” on page 8-5

# hdlsetup

---

**Purpose** Set up model parameters for HDL code generation

**Syntax** `hdlsetup('modelName')`

**Description** `hdlsetup('modelName')` sets the parameters of the model specified by *modelName* to common default values for HDL code generation. After using `hdlsetup`, you can use `set_param` to modify these default settings.

Open the model before you invoke the `hdlsetup` command.

To see which model parameters are affected by `hdlsetup`, open `hdlsetup.m`.

## How hdlsetup Configures Solver Options

`hdlsetup` configures **Solver** options used by the coder. These options are:

- **Type:** Fixed-step. This is the recommended solver type for most HDL applications.

The coder also supports variable-step solvers under the following conditions:

- The device under test (DUT) is single-rate.
  - The sample times of all signals driving the DUT are greater than 0.
- **Solver:** Discrete (no continuous states). You can use other fixed-step solvers, but this option is usually best for simulating discrete systems.
  - **Tasking mode:** SingleTasking. The coder does not support multitasking mode.

Do not set **Tasking mode** to Auto.



---

<b>Purpose</b>	Generate HDL RTL code from model or subsystem
<b>Syntax</b>	<code>makehdl(model)</code> <code>makehdl(model,Name,Value)</code>
<b>Description</b>	<p><code>makehdl(model)</code> generates HDL code from the specified model.</p> <p><code>makehdl(model,Name,Value)</code> generates HDL code from the specified model with options specified by one or more name-value pair arguments.</p>
<b>Input Arguments</b>	<p><b>model - Model or subsystem name</b> string</p> <p>Model or subsystem name, specified as top-level model name or subsystem name with full hierarchical path.</p> <p><b>Example:</b> <code>'top_level_name'</code></p> <p><b>Example:</b> <code>'top_level_name/subsysA/subsysB/codegen_subsys_name'</code></p> <p><b>Name-Value Pair Arguments</b></p> <p>Specify optional comma-separated pairs of <code>Name,Value</code> arguments, where <code>Name</code> is the argument name and <code>Value</code> is the corresponding value. <code>Name</code> must appear inside single quotes ( <code>' '</code> ). You can specify several name and value pair arguments in any order as <code>Name1,Value1,...,NameN,ValueN</code>.</p> <p><b>Example:</b> <code>'TargetLanguage','Verilog'</code></p> <p><b>Basic Options</b></p> <p><b>TargetLanguage - Target language</b> <code>'VHDL'</code> (default)   <code>'Verilog'</code></p> <p>For more information, see <code>TargetLanguage</code>.</p> <p><b>TargetDirectory - Output directory</b></p>

'hdlsrc' (default) | string

For more information, see TargetDirectory.

## **CheckHDL - Check HDL code generation compatibility**

'off' (default) | 'on'

For more information, see CheckHDL.

## **GenerateHDLCode - Generate HDL code**

'on' (default) | 'off'

For more information, see GenerateHDLCode.

## **SplitEntityArch - Split VHDL entity and architecture into separate files**

'off' (default) | 'on'

For more information, see SplitEntityArch.

## **Verbosity - Level of message detail**

1 (default) | 0

For more information, see Verbosity.

## **Report Generation**

### **Traceability - Generate report with mapping links between HDL and model**

'off' (default) | 'on'

For more information, see Traceability.

### **ResourceReport - Resource utilization report generation**

'off' (default) | 'on'

For more information, see ResourceReport.

### **OptimizationReport - Optimization report generation**

'off' (default) | 'on'

For more information, see OptimizationReport.

### **GenerateWebview - Include model Web view**

'on' (default) | 'off'

For more information, see GenerateWebview.

## **Speed and Area Optimization**

### **BalanceDelays - Delay balancing**

'on' (default) | 'off'

For more information, see BalanceDelays.

### **HierarchicalDistPipelining - Hierarchical distributed pipelining**

'off' (default) | 'on'

For more information, see HierarchicalDistPipelining.

### **OptimizeTimingController - Timing controller speed and area optimization**

'on' (default) | 'off'

For more information, see OptimizeTimingController.

### **MinimizeClockEnables - Omit clock enable logic for single-rate designs**

'off' (default) | 'on'

For more information, see MinimizeClockEnables.

### **RAMMappingThreshold - Minimum RAM size for mapping to RAMs instead of registers**

256 (default) | positive integer

The minimum RAM size required for mapping to RAMs instead of registers, specified in bits.

For more information, see RAMMappingThreshold.

## Coding Style

### **UserComment - HDL file header comment**

string

For more information, see UserComment.

### **UseAggregatesForConst - Represent constant values with aggregates**

'off' (default) | 'on'

For more information, see UseAggregatesForConst.

### **UseRisingEdge - Use VHDL rising\_edge function to clock registers**

'off' (default) | 'on'

For more information, see UseRisingEdge.

### **LoopUnrolling - Unroll VHDL FOR and GENERATE loops**

'off' (default) | 'on'

For more information, see LoopUnrolling.

### **CastBeforeSum - Input value type casting for addition and subtraction**

'on' (default) | 'off'

For more information, see CastBeforeSum.

### **UseVerilogTimescale - Generate 'timescale compiler directives**

'on' (default) | 'off'

For more information, see UseVerilogTimescale.

### **InlineConfigurations - Include VHDL configurations**

'on' (default) | 'off'

For more information, see InlineConfigurations.

### **SafeZeroConcat - Type-safe syntax for concatenated zeros**

'on' (default) | 'off'

For more information, see SafeZeroConcat.

### **DateComment - Include time stamp in header**

'on' (default) | 'off'

For more information, see DateComment.

### **ScalarizePorts - Flatten vector ports into scalar ports**

'off' (default) | 'on'

For more information, see ScalarizePorts.

### **MinimizeIntermediateSignals - Minimize intermediate signals**

'off' (default) | 'on'

For more information, see MinimizeIntermediateSignals.

### **RequirementComments - Link from code generation reports to requirement documents**

'on' (default) | 'off'

For more information, see RequirementComments.

### **InlineMATLABBlockCode - Inline HDL code for MATLAB Function blocks**

'off' (default) | 'on'

For more information, see InlineMATLABBlockCode.

### **MaskParameterAsGeneric - Reusable code generation for subsystems with identical mask parameters**

'off' (default) | 'on'

For more information, see MaskParameterAsGeneric.

### **InitializeBlockRAM - Initial signal value generation for RAM blocks**

'on' (default) | 'off'

For more information, see InitializeBlockRAM.

## **RAMArchitecture - RAM architecture**

'WithClockEnable' (default) | 'WithoutClockEnable'

For more information, see RAMArchitecture.

## **HandleAtomicSubsystem - Reusable code generation for identical atomic subsystems**

'on' (default) | 'off'

For more information, see HandleAtomicSubsystem.

## **Clocks and Reset**

### **Oversampling - Oversampling factor for global clock**

1 (default) | integer greater than or equal to 0

Frequency of global oversampling clock, specified as an integer multiple of the model's base rate.

For more information, see Oversampling.

### **ResetAssertedLevel - Asserted (active) level of reset**

'active-high' (default) | 'active-low'

For more information, see ResetAssertedLevel.

### **ResetType - Reset type**

'async' (default) | 'sync'

For more information, see ResetType.

## **Test Bench**

### **Verbosity - Level of message detail**

0 (default) | n

For more information, see Verbosity.

**GenerateCoSimBlock - Generate HDL Cosimulation block**`'off' (default) | 'on'`

Generate an HDL Cosimulation block so you can simulate the DUT in Simulink with an HDL simulator.

For more information, see `GenerateCoSimBlock`.

**GenerateCoSimModel - Generate HDL Cosimulation model**`'ModelSim' (default) | 'Incisive'`

Generate a model containing an HDL Cosimulation block for the specified HDL simulator.

For more information, see `GenerateCoSimModel`.

**GenerateValidationModel - Generate validation model**`'off' (default) | 'on'`

For more information, see `GenerateValidationModel`.

**SimulatorFlags - Options for generated compilation scripts**`string`

For more information, see `SimulatorFlags`.

**TestBenchReferencePostFix - Suffix for test bench reference signals**`'_ref' (default) | string`

For more information, see `TestBenchReferencePostFix`.

**Script Generation****EDAScriptGeneration - Enable or disable script generation for third-party tools**`'on' (default) | 'off'`

For more information, see `EDAScriptGeneration`.

**HDLCompileInit - Compilation script initialization string**`'vlib work\n' (default) | string`

For more information, see HDLCompileInit.

## **HDLCompileTerm - Compilation script termination string**

' ' (default) | string

For more information, see HDLCompileTerm.

## **HDLCompileFilePostfix - Postfix for compilation script file name**

'\_compile.do' (default) | string

For more information, see HDLCompileFilePostfix.

## **HDLCompileVerilogCmd - Verilog compilation command**

'vlog %s %s\n' (default) | string

Verilog compilation command, specified as a string. The SimulatorFlags name-value pair specifies the first argument, and the module name specifies the second argument.

For more information, see HDLCompileVerilogCmd.

## **HDLCompileVHDLCmd - VHDL compilation command**

'vcom %s %s\n' (default) | string

VHDL compilation command, specified as a string. The SimulatorFlags name-value pair specifies the first argument, and the entity name specifies the second argument.

For more information, see HDLCompileVerilogCmd.

## **HDLSynthTool - Synthesis tool**

'None' (default) | 'ISE' | 'Precision' | 'Quartus' | 'Synplify'

HDL synthesis tool, specified as a string.

For more information, see HDLSynthTool.

## **HDLSynthCmd - HDL synthesis command**

string



HDL synthesis command, specified as a string. The default is derived from the HDLSynthTool name-value pair.

For more information, see HDLSynthCmd.

### **HDLSynthFilePostfix - Postfix for synthesis script file name**

string

HDL synthesis script file name postfix, specified as a string. The default is derived from the HDLSynthTool name-value pair.

For more information, see HDLSynthFilePostfix.

### **HDLSynthInit - Synthesis script initialization string**

string

Initialization for the HDL synthesis script, specified as a string. The default is derived from the HDLSynthTool name-value pair.

For more information, see HDLSynthInit.

### **HDLSynthTerm - Synthesis script termination string**

string

Termination string for the HDL synthesis script. The default is derived from the HDLSynthTool name-value pair.

For more information, see HDLSynthTerm.

## **Generated Model**

### **CodeGenerationOutput - Display and generation of generated model**

'GenerateHDLCode' (default) |  
'GenerateHDLCodeAndDisplayGeneratedModel' |  
'DisplayGeneratedModelOnly'

For more information, see CodeGenerationOutput.

### **GeneratedModelName - Generated model name**

same as original model name (default) | string

For more information, see `GeneratedModelName`.

## **GeneratedModelNamePrefix - Prefix for generated model name**

'gm\_' (default) | string

For more information, see `GeneratedModelNamePrefix`.

## **HighlightAncestors - Highlight parent blocks of generated model blocks differing from original model**

'on' (default) | 'off'

For more information, see `HighlightAncestors`.

## **HighlightColor - Color of highlighted blocks in generated model**

'cyan' (default) | 'yellow' | 'magenta' | 'red' | 'green' | 'blue'  
| 'white' | 'magenta' | 'black'

For more information, see `HighlightColor`.

## **Synthesis**

### **MulticyclePathInfo - Multicycle path constraint file generation**

'off' (default) | 'on'

For more information, see `MulticyclePathInfo`.

## **Port Names and Types**

### **ClockEnableInputPort - Clock enable input port name**

'clk\_enable' (default) | string

Clock enable input port name, specified as a string.

For more information, see `ClockEnableInputPort`.

### **ClockEnableOutputPort - Clock enable output port name**

'ce\_out' (default) | string

Clock enable output port name, specified as a string.

For more information, see `ClockEnableOutputPort`.

**ClockInputPort - Clock input port name**

'clk' (default) | string

Clock input port name, specified as a string.

For more information, see ClockInputPort.

**ClockInputs - Single or multiple clock inputs**

'Single' (default) | 'Multiple'

Single or multiple clock inputs, specified as a string.

For more information, see ClockInputs.

**EnablePrefix - Prefix for internal enable signals**

'enb' (default) | string

Prefix for internal clock enable and control flow enable signals, specified as a string.

For more information, see EnablePrefix.

**InputType - HDL data type for input ports**

'std\_logic\_vector' (default) | 'signed/unsigned' | 'wire' (default)

HDL data type for input ports, specified as a string.

VHDL inputs can have 'std\_logic\_vector' or 'signed/unsigned' data type. Verilog inputs must be 'wire'.

For more information, see InputType.

**OutputType - HDL data type for output ports**

'Same as input data type' (default) | 'std\_logic\_vector' | 'signed/unsigned' | 'wire' (default)

HDL data type for output ports, specified as a string.

VHDL output can be 'Same as input data type', 'std\_logic\_vector' or 'signed/unsigned'. Verilog output must be 'wire'.

For more information, see OutputType.

## **ResetInputPort - Reset input port name**

'reset' (default) | string

Reset input port name, specified as a string.

For more information, see ResetInputPort.

## **File and Variable Names**

### **VerilogFileExtension - Verilog file extension**

'.v' (default) | string

For more information, see VerilogFileExtension.

### **VHDLFileExtension - VHDL file extension**

'.vhd' (default) | string

For more information, see VHDLFileExtension.

### **VHDLArchitectureName - VHDL architecture name**

'rtl' (default) | string

For more information, see VHDLArchitectureName.

### **VHDLLibraryName - VHDL library name**

'work' (default) | string

For more information, see VHDLLibraryName.

### **SplitEntityFilePostfix - Postfix for VHDL entity file names**

'\_entity' (default) | string

For more information, see SplitEntityFilePostfix.

### **SplitArchFilePostfix - Postfix for VHDL architecture file names**

'\_arch' (default) | string

For more information, see SplitArchFilePostfix.

### **PackagePostfix - Postfix for package file name**

'\_pkg' (default) | string

For more information, see `PackagePostfix`.

### **HDLMapFilePostfix - Postfix for mapping file**

'\_map.txt' (default) | string

For more information, see `HDLMapFilePostfix`.

### **BlockGenerateLabel - Block label postfix for VHDL GENERATE statements**

'\_gen' (default) | string

For more information, see `BlockGenerateLabel`.

### **ClockProcessPostfix - Postfix for clock process names**

'\_process' (default) | string

For more information, see `ClockProcessPostfix`.

### **ComplexImagPostfix - Postfix for imaginary part of complex signal**

'\_im' (default) | string

For more information, see `ComplexImagPostfix`.

### **ComplexRealPostfix - Postfix for imaginary part of complex signal names**

'\_re' (default) | string

For more information, see `ComplexRealPostfix`.

### **EntityConflictPostfix - Postfix for duplicate VHDL entity or Verilog module names**

'\_block' (default) | string

For more information, see `EntityConflictPostfix`.

### **InstanceGenerateLabel - Instance section label postfix for VHDL GENERATE statements**

'\_gen' (default) | string

For more information, see InstanceGenerateLabel.

**InstancePostfix - Postfix for generated component instance names**

' ' (default) | string

For more information, see InstancePostfix.

**InstancePrefix - Prefix for generated component instance names**

'u\_' (default) | string

For more information, see InstancePrefix.

**OutputGenerateLabel - Output assignment label postfix for VHDL GENERATE statements**

'outputgen' (default) | string

For more information, see OutputGenerateLabel.

**PipelinePostfix - Postfix for input and output pipeline register names**

'\_pipe' (default) | string

For more information, see PipelinePostfix.

**ReservedWordPostfix - Postfix for names conflicting with VHDL or Verilog reserved words**

'\_rsvd' (default) | string

For more information, see ReservedWordPostfix.

**TimingControllerPostfix - Postfix for timing controller name**

'\_tc' (default) | string

For more information, see TimingControllerPostfix.

**VectorPrefix - Prefix for vector names**

'vector\_of\_' (default) | string

For more information, see VectorPrefix.

## Examples

### Generate VHDL for the Current Model

Generate VHDL code for the current model.

Generate HDL code for the current model with code generation options set to default values.

```
makehdl(bdroot)
```

The generated VHDL code is saved in the hdlsrc folder.

### Generate Verilog for a Subsystem Within a Model

Generate Verilog for the subsystem `symmetric_fir` within the model `sfir_fixed`.

Open the `sfir_fixed` model.

```
sfir_fixed;
```

The model opens in a new Simulink window.

Generate Verilog for the `symmetric_fir` subsystem.

```
makehdl('sfir_fixed/symmetric_fir','TargetLanguage','Verilog')
```

```
### Generating HDL for 'sfir_fixed/symmetric_fir'  
### Starting HDL Check.  
### HDL Check Complete with 0 errors, 0 warnings and 0 messages.
```

```
### Begin Verilog Code Generation  
### Working on sfir_fixed/symmetric_fir as hdlsrc\symmetric_fir.v  
### HDL Code Generation Complete.
```

The generated Verilog code for the `symmetric_fir` subsystem is saved in `hdlsrc\symmetric_fir.v`.

Close the model.

```
bdclose('sfir_fixed');
```

## **Check Subsystem for Compatibility with HDL Code Generation**

Check that the subsystem `symmetric_fir` is compatible with HDL code generation, then generate HDL.

Open the `sfir_fixed` model.

```
sfir_fixed;
```

The model opens in a new Simulink window.

Check the `symmetric_fir` subsystem for compatibility with HDL code generation. Generate code with code generation options set to default values.

```
makehdl('sfir_fixed/symmetric_fir','CheckHDL','on')
```

The generated VHDL code for the `symmetric_fir` subsystem is saved in `hdlsrc\symmetric_fir.v`. For more information on the HDL compatibility checker, see `checkhdl`.

Close the model.

```
bdclose('sfir_fixed');
```

## **See Also**

```
makehdltb | checkhdl
```



---

<b>Purpose</b>	Generate HDL test bench from model or subsystem
<b>Syntax</b>	<code>makehdltb(subsys)</code> <code>makehdltb(subsys,Name,Value)</code>
<b>Description</b>	<p><code>makehdltb(subsys)</code> generates an HDL test bench from the specified subsystem.</p> <p><code>makehdltb(subsys,Name,Value)</code> generates an HDL test bench from the specified subsystem with options specified by one or more name-value pair arguments.</p>
<b>Input Arguments</b>	<p><b>subsys - Subsystem name</b> string</p> <p>Subsystem name, specified as a string, with full hierarchical path.</p> <p><b>Example:</b> <code>'modelName/subsysTarget'</code></p> <p><b>Example:</b> <code>'modelName/subsysA/subsysB/subsysTarget'</code></p> <p><b>Name-Value Pair Arguments</b></p> <p>Specify optional comma-separated pairs of <code>Name,Value</code> arguments, where <code>Name</code> is the argument name and <code>Value</code> is the corresponding value. <code>Name</code> must appear inside single quotes ( <code>' '</code>). You can specify several name and value pair arguments in any order as <code>Name1,Value1,...,NameN,ValueN</code>.</p> <p><b>Example:</b> <code>`TargetLanguage','Verilog'</code></p> <p><b>Basic Options</b></p> <p><b>TargetLanguage - Target language</b> <code>'VHDL'</code> (default)   <code>'Verilog'</code></p> <p>For more information, see <code>TargetLanguage</code>.</p> <p><b>TargetDirectory - Output directory</b></p>

'hdlsrc' (default) | string

For more information, see TargetDirectory.

## **SplitEntityArch - Split VHDL entity and architecture into separate files**

'off' (default) | 'on'

For more information, see SplitEntityArch.

## **Test Bench**

### **ForceClock - Force clock input**

'on' (default) | 'off'

Specify that the generated test bench drives the clock enable input based on ClockLowTime and ClockHighTime.

For more information, see ForceClock.

### **ClockHighTime - Clock high time**

5 (default) | positive integer

Clock high time during a clock period, specified in nanoseconds.

For more information, see ClockHighTime.

### **ClockLowTime - Clock low time**

5 (default) | positive integer

Clock low time during a clock period, specified in nanoseconds.

For more information, see ClockLowTime.

### **ForceClockEnable - Force clock enable input**

'on' (default) | 'off'

Specify that the generated test bench drives the clock enable input.

For more information, see ForceClockEnable.

### **ForceReset - Force reset input**

'on' (default) | 'off'

Specify that the generated test bench drives the reset input.

For more information, see ForceReset.

### **ResetLength - Reset asserted time length**

2 (default) | integer greater than or equal to 0

Length of time that reset is asserted, specified as the number of clock cycles.

For more information, see ResetLength.

### **ResetAssertedLevel - Asserted (active) level of reset**

'active-high' (default) | 'active-low'

For more information, see ResetAssertedLevel.

### **HoldInputDataBetweenSamples - Hold valid data for signals clocked at slower rate**

'on' (default) | 'off'

For more information, see HoldInputDataBetweenSamples.

### **HoldTime - Hold time for inputs and forced reset**

2 (default) | positive integer

Hold time for inputs and forced reset, specified in nanoseconds.

For more information, see HoldTime.

### **IgnoreDataChecking - Time to wait after clock enable before checking output data**

0 (default) | positive integer

Time after clock enable is asserted before starting output data checks, specified in number of samples.

For more information, see IgnoreDataChecking.

### **InitializeTestBenchInputs - Initialize test bench inputs to '0'**

'off' (default) | 'on'

For more information, see InitializeTestBenchInputs.

### **MultifileTestBench - Divide generated test bench into helper functions, data, and HDL test bench files**

'off' (default) | 'on'

For more information, see MultifileTestBench.

### **TestBenchClockEnableDelay - Number of clock cycles between deassertion of reset and assertion of clock enable**

1 (default) | positive integer

For more information, see TestBenchClockEnableDelay.

### **TestBenchDataPostFix - Postfix for test bench data file name**

'\_data' (default) | string

For more information, see TestBenchDataPostFix.

### **TestBenchPostFix - Suffix for test bench name**

'\_tb' (default) | string

For more information, see TestBenchPostFix.

### **GenerateCoSimBlock - Generate HDL Cosimulation block**

'off' (default) | 'on'

Generate an HDL Cosimulation block so you can simulate the DUT in Simulink with an HDL simulator.

For more information, see GenerateCoSimBlock.

### **GenerateCoSimModel - Generate HDL Cosimulation model**

'ModelSim' (default) | 'Incisive'

Generate a model containing an HDL Cosimulation block for the specified HDL simulator.

For more information, see GenerateCoSimModel.

## Coding Style

### **UseVerilogTimescale - Generate 'timescale compiler directives**

'on' (default) | 'off'

For more information, see UseVerilogTimescale.

### **DateComment - Include time stamp in header**

'on' (default) | 'off'

For more information, see DateComment.

### **InlineConfigurations - Include VHDL configurations**

'on' (default) | 'off'

For more information, see InlineConfigurations.

### **ScalarizePorts - Flatten vector ports into scalar ports**

'off' (default) | 'on'

For more information, see ScalarizePorts.

## Script Generation

### **HDLCompileInit - Compilation script initialization string**

'vlib work\n' (default) | string

For more information, see HDLCompileInit.

### **HDLCompileTerm - Compilation script termination string**

' ' (default) | string

For more information, see HDLCompileTerm.

### **HDLCompileFilePostfix - Postfix for compilation script file name**

'\_compile.do' (default) | string

For more information, see HDLCompileFilePostfix.

### **HDLCompileVerilogCmd - Verilog compilation command**

`'vlog %s %s\n'` (default) | string

Verilog compilation command, specified as a string. The `SimulatorFlags` name-value pair specifies the first argument, and the module name specifies the second argument.

For more information, see `HDLCompileVerilogCmd`.

### **HDLCompileVHDLCmd - VHDL compilation command**

`'vcom %s %s\n'` (default) | string

VHDL compilation command, specified as a string. The `SimulatorFlags` name-value pair specifies the first argument, and the entity name specifies the second argument.

For more information, see `HDLCompileVerilogCmd`.

### **HDLSimCmd - HDL simulation command**

`'vsim -novopt work.%s\n'` (default) | string

The HDL simulation command, specified as a string. Your top-level module or entity name is automatically used as the argument.

For more information, see `HDLSimCmd`.

### **HDLSimInit - HDL simulation script initialization string**

`['onbreak resume\n', 'onerror resume\n']` (default) | string

Initialization for the HDL simulation script, specified as a string.

For more information, see `HDLSimInit`.

### **HDLSimTerm - HDL simulation script termination string**

`'run -all'` (default) | string

The termination string for the HDL simulation command.

For more information, see `HDLSimTerm`.

### **HDLSimFilePostfix - Postscript for HDL simulation script**

`'_sim.do'` (default) | string

For more information, see `HDLsimFilePostfix`.

### **HDLsimViewWaveCmd - HDL simulation waveform viewing command**

`'add wave sim:%s\n'` (default) | string

Waveform viewing command, specified as a string. The top-level module or entity name specifies the argument.

For more information, see `HDLsimViewWaveCmd`.

### **Port Names and Types**

#### **ClockEnableInputPort - Clock enable input port name**

`'clk_enable'` (default) | string

Clock enable input port name, specified as a string.

For more information, see `ClockEnableInputPort`.

#### **ClockEnableOutputPort - Clock enable output port name**

`'ce_out'` (default) | string

Clock enable output port name, specified as a string.

For more information, see `ClockEnableOutputPort`.

#### **ClockInputPort - Clock input port name**

`'clk'` (default) | string

Clock input port name, specified as a string.

For more information, see `ClockInputPort`.

#### **ClockInputs - Single or multiple clock inputs**

`'Single'` (default) | `'Multiple'`

Single or multiple clock inputs, specified as a string.

For more information, see `ClockInputs`.

#### **EnablePrefix - Prefix for internal enable signals**

'enb' (default) | string

Prefix for internal clock enable and control flow enable signals, specified as a string.

For more information, see `EnablePrefix`.

### **ResetInputPort - Reset input port name**

'reset' (default) | string

Reset input port name, specified as a string.

For more information, see `ResetInputPort`.

## **File and Variable Names**

### **VerilogFileExtension - Verilog file extension**

'.v' (default) | string

For more information, see `VerilogFileExtension`.

### **VHDLFileExtension - VHDL file extension**

'.vhd' (default) | string

For more information, see `VHDLFileExtension`.

### **VHDLArchitectureName - VHDL architecture name**

'rtl' (default) | string

For more information, see `VHDLArchitectureName`.

### **VHDLLibraryName - VHDL library name**

'work' (default) | string

For more information, see `VHDLLibraryName`.

### **SplitEntityFilePostfix - Postfix for VHDL entity file names**

'\_entity' (default) | string

For more information, see `SplitEntityFilePostfix`.



**SplitArchFilePostfix - Postfix for VHDL architecture file names**

'\_arch' (default) | string

For more information, see SplitArchFilePostfix.

**PackagePostfix - Postfix for package file name**

'\_pkg' (default) | string

For more information, see PackagePostfix.

**ComplexImagPostfix - Postfix for imaginary part of complex signal**

'\_im' (default) | string

For more information, see ComplexImagPostfix.

**ComplexRealPostfix - Postfix for imaginary part of complex signal names**

'\_re' (default) | string

For more information, see ComplexRealPostfix.

**Examples****Generate VHDL Test Bench**

Generate VHDL DUT and test bench for a subsystem.

Use makehdl to generate VHDL code for the subsystem symmetric\_fir.

```
makehdl('sfir_fixed/symmetric_fir')
```

```
### Applying HDL Code Generation Control Statements
```

```
### Begin VHDL Code Generation
### Working on sfir_fixed/symmetric_fir
    as hdlsrc\symmetric_fir.vhd
### HDL Code Generation Complete.
```

After makehdl is complete, use makehdltb to generate a VHDL test bench for the same subsystem.

```
makehdltb('sfir_fixed/symmetric_fir')

### Begin TestBench Generation
### Generating Test bench:
   hdlsrc\symmetric_fir_tb.vhd
### Please wait ...

### HDL TestBench Generation Complete.
```

The generated VHDL test bench code is saved in the hdlsrc folder.

## Generate Verilog Test Bench

Generate Verilog DUT and test bench for a subsystem.

Use makehdl to generate Verilog code for the subsystem symmetric\_fir.

```
makehdl('sfir_fixed/symmetric_fir','TargetLanguage','Verilog')

### Generating HDL for 'sfir_fixed/symmetric_fir'.
### Starting HDL check.
### HDL check complete with 0 errors, 0 warnings and 0 messages.
### Begin Verilog Code Generation
### Working on sfir_fixed/symmetric_fir as hdlsrc\symmetric_fir.v
### HDL code generation complete.
```

After makehdl is complete, use makehdltb to generate a Verilog test bench for the same subsystem.

```
makehdltb('sfir_fixed/symmetric_fir','TargetLanguage','Verilog')

### Begin TestBench generation.
### Generating HDL TestBench for 'sfir_fixed/symmetric_fir'.
### Begin simulation of the model 'gm_sfir_fixed'...
### Collecting data...
### Generating test bench: hdlsrc\symmetric_fir_tb.v
### Creating stimulus vectors...
### HDL TestBench generation complete.
```

The generated Verilog test bench code is saved in the hdlsrc folder.

**See Also** `makehd1`



# Function Reference

---

## Code Generation Functions

`makehdl`

Generate HDL RTL code from model or subsystem

`makehdltb`

Generate HDL test bench from model or subsystem

## HDL Block and Model Parameter Utilities

<code>hdldispblkparams</code>	Display HDL block parameters that have nondefault values
<code>hdldispmdlparams</code>	Display HDL model parameters that have nondefault values
<code>hdlget_param</code>	Return value of specified HDL block-level parameter for specified block
<code>hdlset_param</code>	Set HDL-related parameters at model or block level

## Utility Functions

<code>checkhdl</code>	Check subsystem or model for HDL code generation compatibility
<code>hdladvisor</code>	Display HDL Workflow Advisor
<code>hdllib</code>	Create library of blocks that support HDL code generation
<code>hdlsetup</code>	Set up model parameters for HDL code generation



## Control File Utilities

<code>hdlapplycontrolfile</code>	Apply control file settings to model
<code>hdlnewblackbox</code>	Generate customizable control file from selected subsystem or blocks
<code>hdlnewcontrol</code>	Construct code generation control object for use in control file
<code>hdlnewcontrolfile</code>	Generate customizable control file from selected subsystem or blocks
<code>hdlnewforeach</code>	Generate <code>forEach</code> calls for insertion into code generation control files



# Examples

---

Use this list to find examples in the documentation.

## **Specifying Inputs**

“Specifying Properties of Primary Inputs by Example at the Command Line” on page 2-14

“Specifying Properties of Primary Fixed-Point Inputs by Example at the Command Line” on page 2-15

“Specifying a Structure as a Constant Input” on page 2-17

“Specifying a Variable-Size Vector Input” on page 2-18

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